2GHz High Performance Double Edge Triggered D-Flip Flop Based Shift Registers In 32NM CMOS Technology

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Abstract

This paper provides an efficient design and analysis of Serial In Serial Out (SISO), Serial In Parallel Out (SIPO), Parallel In Serial Out (PISO) and Parallel In Parallel Out (PIPO) shift registers using High Performance Double Edge Triggered D-Flip flop (DETFF). Double Edge Triggered Flip Flops stores data on both the rising edge and falling edge of a clock signal. Although the clock frequency is determined by the system specifications, the usage of DET flip-flops can reduce the clock frequency to half of its original value for the same data throughput. As a result, power consumption is reduced, making DET flip-flops desirable for low power applications. The DETFF based shift registers are simulated with different clock frequencies and the performance of the shift registers are evaluated by observing the average power, delay and PDP.

Keywords— *DETFF, delay, PDP, performance, power consumption, throughput.*

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1. Introduction

In the past, the major concerns of the very large scale integrated (VLSI) engineers were area, performance, cost and reliability; power considerations were mostly of only secondary importance. Currently, several VLSI design implementations are described in CMOS technology. Power consumption of VLSI chips is becoming an increasingly critical problem as modern VLSI circuits continue to grow and technologies evolve. In portable systems, very low power consumption is desired in order to increase battery life.

The total clock related power consumption in synchronous VLSI circuits can be divided into three major factors: power consumption in the clock network, power consumption in the clock buffers, and power consumption in the flip-flops. Therefore, the improvement of such circuits without weakening the characteristics is of prime importance to the VLSI industry. Today's focus on low power is not only because of the recent growing demands of mobile applications. Even before the mobile era, power consumption has been a fundamental problem. To solve the power dissipation problem, many researchers have proposed different ideas from the device level to the architectural level and above. However, there is no universal way to avoid tradeoffs between power, delay and area, and thus designers are required to choose appropriate techniques that satisfy application and product needs.

Currently, several designs are described in CMOS technology. CMOS flip-flops are widely used in building many systems including portable systems, personal computers, servers, etc. Flip-flops appear in several configurations, such as D flip-flops, T flip-flops and J-K flip-flops where the D flip-flop is the most common. In order to reduce the complexity of circuit design, a large proportion of digital circuits are designed to be synchronous circuits; that is, they operate based on a clock signal. D-type flip-flop (DFF) is one of the most fundamental building block in modern VLSI systems and it contributes a significant part of the total power dissipation of the system.

The 32 nanometer (32 nm) node is the step following the 45 nanometer process in CMOS semiconductor device fabrication. Intel and AMD both produced commercial microchips using the 32 nanometer process in the early 2010s. IBM and the Common Platform also developed a 32 nm high-k metal gate process. Intel began selling its 32 nm processors as Core i3, Core i5, and the dual-core mobile Core i7. In this paper, DETFF and shift registers are designed in 32nm technology.

This paper is organized as follows: Section 2 & 3 explains the basics of DETFF and shift registers. The nominal simulations along with analysis are discussed in Section 4. Performance for newly designed shift registers is compared in terms of average power, delay and PDP in Section 5. Paper ends in Section 6 with the conclusion.

2. Double Edge Triggered D-Flip Flop

High performance flip-flops are crucial when the device dimensions shrunk down to sub-32nm technology. The common approach for improving the performance is to increase the clock frequency. However, use of high clock frequency has a number of disadvantages. Power consumption of the clock system dramatically increases and clock uncertainties take significant part of the clock cycle. Other problems include degradation of the clock waveform due to the non-ideal clock distribution, power supply noise and cross-talk. An alternative clocking strategy relies on the use of storage elements capable of capturing data on both clock edges (rising edge and falling edge). Such storage elements are referred to as Double-Edge Triggered clocked Storage Elements (DETSE).

In this case, the same data throughput can be achieved with half of the clock frequency. In other words double edge clocking can be used to save half of the power on the clock distribution network. Double edge triggered flip-flops are edge sensitive devices which latch data in each clock period on rising and falling edge of the clock signal. Several flip-flops have been proposed in the literature. The main attention has been in improving the performance of the circuits.

Though several contributions have been made to the art of DET flip-flops, a need evidently occurs for a design that further improves the relative power consumption of DET flip-flops. One such high performance DETFF is shown in Fig 1.

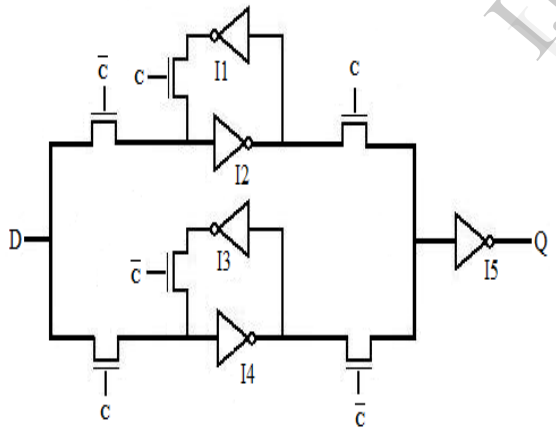

FIGURE 1: HIGH PERFORMANCE DETFF [1]

The high performance DETFF in Fig. 1 is free from threshold voltage loss problem of pass transistors. Thus the high performance Double Edge Triggered Flip-Flop (DETFF) in Fig. 1 is more efficient in terms of area, power and speed which claim for better performance than conventional designs. The high performance DETFF shown in Fig 1 has less average power and lowest PDP than conventional designs. Such DETFF is very well suited for high performance applications.

3. Shift Registers

In digital circuits, Shift register is a group of flip-flops used to shift or transfer data from flip-flop to flip-flop. It's a group of D flip-flops connected in a chain and the clock of the flip-flops is connected in a synchronous manner. Shift register has 2 basic functions such as; data storage and data movement. Shift register has 4 classifications namely; Serial In Serial Out (SISO), Serial In Parallel Out (SIPO), Parallel In Serial Out (PISO) and Parallel In Parallel Out (PIPO).

3.1 Serial In Serial Out (SISO) Shift Register

The Serial In Serial Out (SISO) shift register accepts data serially (one bit at a time on a single line). It produces the stored information on its output also in serial form. And the basic Serial In Serial Out (SISO) shift register is shown in Fig 2.

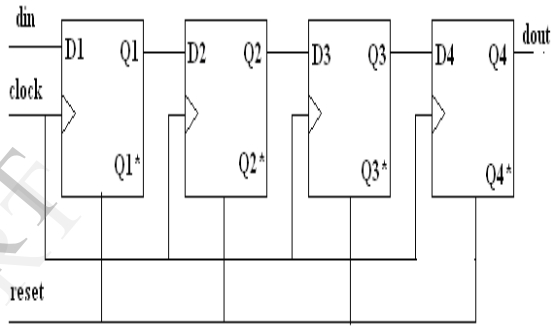

FIGURE 2: SISO SHIFT REGISTER

3.2 Serial In Parallel Out (SIPO) Shift Register

This configuration allows conversion from serial to parallel format. Data input is given serially, as described in the SISO section above. Once the data are stored, each bit appears on its respective output line, and all bits are available simultaneously. And the basic Serial In Parallel Out (SIPO) shift register is shown in Fig 3.

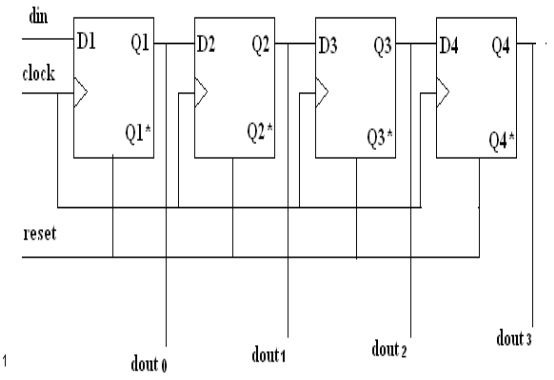

FIGURE 3: SIPO SHIFT REGISTER

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3.3 Parallel In Serial Out (PISO) Shift Register

This configuration has the data input on lines D1 through D4 in parallel format. To write the data to the register, the Write/Shift control line must be held LOW. To shift the data, the W/S control line is brought HIGH and the registers are clocked. The arrangement now acts as a PISO shift register, with D1 as the Data Input. However, as long as the number of clock cycles is not more than the length of the data-string, the Data Output, Q, will be the parallel data read off in order. And the Parallel In Serial Out is shown in Fig 4.

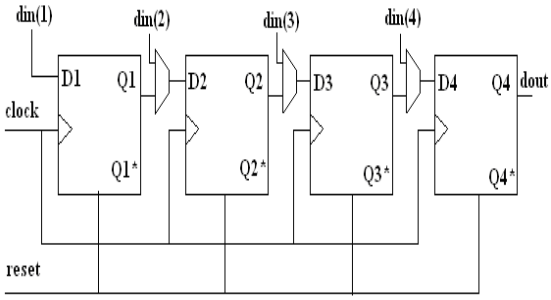

FIGURE 4: PISO SHIFT REGISTER

3.4 Parallel In Parallel (PIPO) Shift Register

For parallel in - parallel out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits. The following circuit is a four-bit Parallel In Parallel Out shift register constructed by D flip-flops and shown in Fig 5. The D's are the parallel inputs and the Q's are the parallel outputs. Once the register is clocked, all the data at the D inputs appear at the corresponding Q outputs simultaneously.

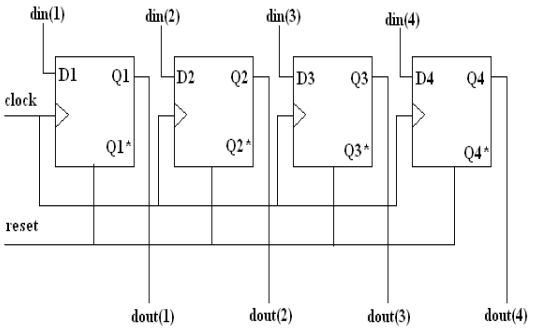

FIGURE 5: PIPO SHIFT REGISTER

4. Simulation Results

To evaluate the performance, high performance DETFF and all the shift registers are designed using 32nm CMOS technology. All simulations are carried out using HSPICE simulation tool at nominal conditions with operating frequencies of 1GHz and 2GHz. The simulated waveforms of DETFF and shift registers are shown in Fig. 6, 7, 8, 9 & 10. These waveforms show that the DETFF based shift register is storing the data in both rising edge and falling edge of the clock signal.

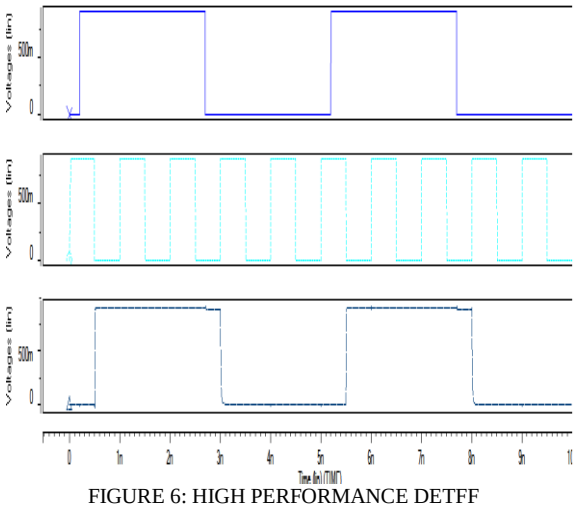

FIGURE 6: HIGH PERFORMANCE DETFF

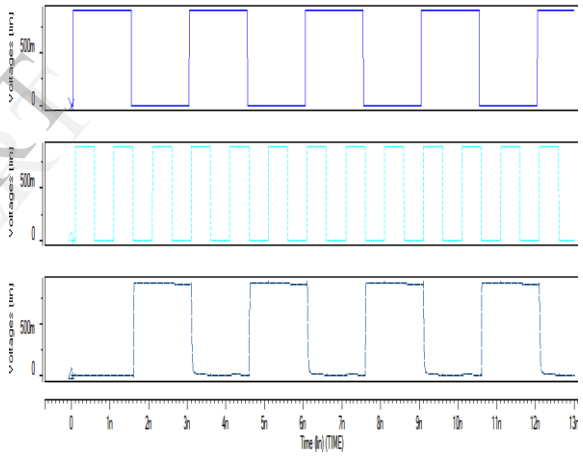

FIGURE 7: SISO SHIFT REGISTER

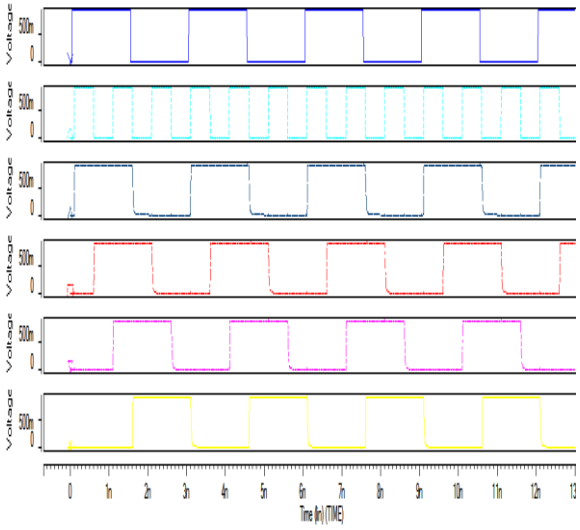

FIGURE 8: SIPO SHIFT REGISTER

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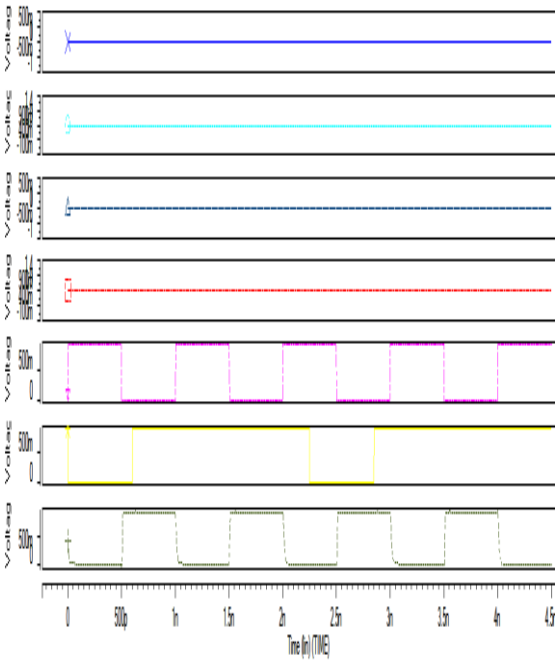

FIGURE 9: PISO SHIFT REGISTER

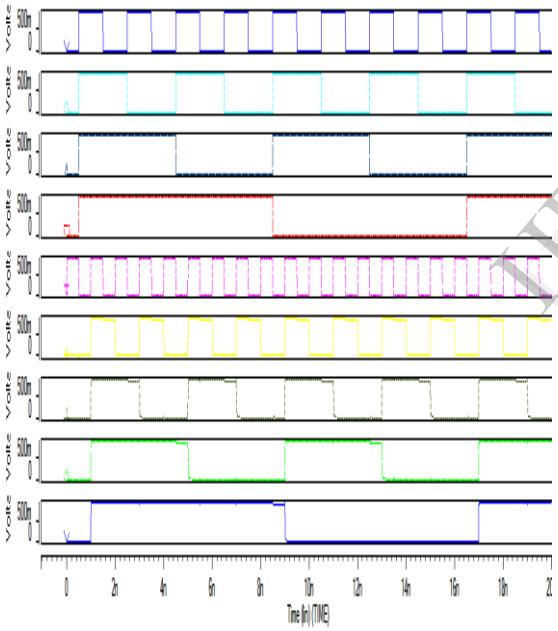

FIGURE 10: PIPO SHIFT REGISTER

5. Performance Analysis

The performance of the SISO, SIPO, PISO and PIPO shift registers are evaluated by considering the average power, delay and power delay product (PDP). In general, a PDP-based comparison is appropriate for low power portable systems in which the battery life is the primary index of energy efficiency. The following tables TABLE 1 and TABLE 2 furnished the performance parameters of SISO, SIPO, PISO and PIPO shift registers.

TABLE 1: 1GHz CLOCK FREQUENCY

SHIFT REG.	AVG POWER (µW)	DELAY (ns)	PDP (J)
SISO	16.84	1.5171	25.54e-15
SIPO	16.84	0.0170 0.5158 1.0171 1.5171	2.862e-16 86.86e-16 171.1e-16 255.4e-16
PISO	39.26	1.5338	60.21e-15
PIPO	14.92	0.0458	68.33e-17

TABLE 2: 2GHz CLOCK FREQUENCY

SHIFT REG.	AVG POWER (µW)	DELAY (ns)	PDP (J)
SISO	12.30	0.7668	9.431e-15
SIPO	12.30	0.0170 0.2664 0.5174 0.7668	2.091e-16 32.76e-16 63.64e-16 94.31e-16
PISO	40.61	0.7819	31.75e-15
PIPO	5.256	0.0122	64.12e-18

6. Conclusion

In this paper, we have designed a high performance Double Edge Triggered D-Flip Flop based shift registers in 32nm CMOS technology. We have made a performance analysis for exploring the average power, delay and PDP. The shift registers are simulated with different clock frequencies. The simulation results and performance analysis suggest that the designed shift registers are suitable for high performance applications.

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7. References

[1] Ravi.T, Irudaya Praveen.D and Kannan.V, "Design and Analysis of High Performance Double Edge Triggered D-Flip Flop," International Journal of Recent Technology and Engineering (IJRTE), Volume-1, Issue-6, pp. 139-142 January 2013.

[2] Imran Ahmed Khan, Danish Shaikh and Mirza Tariq Beg,, "2 GHz Low Power Double Edge Triggered flip- flop in 65nm CMOS Technology," IEEE Conference, 2012.

[3] Xiaowen Wang and William H. Robinson, "A Low-Power Double Edge-Triggered Flip-Flop with Transmission Gates and Clock Gating," IEEE Conference, pp 205-208, 2010.

[4] Yu Chien-Cheng,, "Low-Power Double Edge- Triggered Flip-Flop Circuit Design," Third International Conference on Innovative Computing Information and Control (ICICIC'08), IEEE Conference, 2008.

[5] G. M. Blair, "Low-power double-edge triggered flip-flop", Electron. Lett., Vol. 33, No. 10, pp. 845-847, 8 May 1997.

[6] Peiyi Zhao, Jason McNeely, Pradeep and Jianping Hu, "Low Power Design of Double-Edge Triggered Flip-Flop by Reducing the Number of Clocked Transistors," IEEE Conference, 2008.

[7] Sandeep Sriram, Arun Ramnath, Haiqing, Hojoon Lee and Ken Choi "A Novel Dual Edge Triggered Near-Threshold State Retentive Latch Design," IEEE Conference, 2011.

[8] M. W. Phyu, W. L. Goh and K. S. Yeo, "A Low-Power Static Dual Edge-Triggered Flip-Flop using an Output-Controlled Discharge Configuration" IEEE Conference, 2005.

[9] M. Pedram, Q. Wu, and X. Wu, "A New Design of Double Edge Triggered Flip-Flops," Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 417–421, 1998.

[10] Troy A. JohnsonP and Ivan S. Kourtev , "A Single Latch, High Speed Double-Edge-triggered flip-flop (DETFF)" IEEE, 2001, in press.

[11] Yu Chien-Cheng, "Design of Low-Power Double Edge-Triggered Flip-Flop Circuit", Second IEEE Conference on Industrial Electronics and Applications, pp 2054-2057, 2007.

[12] S.H.Rasouli, A.Amirabadi, A.Seyedi and A.Afazali-kusha, "Double Edge Triggered Feedback Flip-Flop in Sub 100nm Technology," IEEE Conference, 2006.

[13] Wing-Shan Tam, Sik-Lam Siu, Chi-Wah Kok, and Hei Wong. "Double Edge-Triggered Half-Static Clock-Gated D-Type Flip-Flop". IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC), 2010.

[14] Keisuke Inoue and Mineo Kaneko," Variable-Duty -Cycle Scheduling in Double-Edge-Triggered Flip-Flop-Based High-Level Synthesis," IEEE Conference, 2011.

[15] Fatemeh Aezinia, Sara Najafzadeh, and Ali Afzali-Kusha, "Novel High Speed and Low Power Single and Double Edge-Triggered Flip-Flops," IEEE Conference 2006.

[16] Hossein Karimiyan Alidash, Sayed Masoud Sayedi and Hossein Saidi, "Low-Power State-Retention Dual Edge-Triggered Pulsed Latch," Proceedings of ICEE 2010, May 11-13, IEEE 2010.

[17] M. Pedram, "Power minimization in IC Design: Principles and applications," ACM Transactions on Design Automation of Electronic Systems, vol. 1, pp.3-56, Jan. 1996.

[18] G. E. Tellez, A. Farrahi, and M. Sarafzadeh, "Activity-Driven Clock Design for Low Power Circuits," Proceedings of the IEEWACM International Conference on Computer-Aided Design (ICCAD), pp. 62-65, 1995.

[19] Yingbo Hu, Zhaolin Li and Runde Zhou, "A New Type of High Performance Low Power Low clock swing TSPC flip-flop," IEEE Conference, 2007.

[20] Guoqiang Hang 1,2, Xuanchang Zhou, "Novel CMOS Ternary Flip Flops using Double Pass Transistor logic," IEEE Conference, 2011.

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