8-bit Sigma-Delta Modulator for Biomedical Application

Nisarga R
Department of ECE
Vidyavardhaka College of Engineering
Mysuru, Karnataka, India

Pavan M s
Department of ECE
Vidyavardhaka College of Engineering
Mysuru, Karnataka, India

Charuhasa S R
Department of ECE
Vidyavardhaka College of Engineering
Mysuru, Karnataka, India

Indira B R
Department of ECE
Vidyavardhaka College of Engineering
Mysuru, Karnataka, India

CHethan K S
Department of ECE
Vidyavardhaka College of Engineering
Mysuru, Karnataka, India

Yogeshwari K R
Department of ECE
Vidyavardhaka College of Engineering
Mysuru, Karnataka, India

***Abstract*—This paper presents the design of an 8-bit sigma-delta modulator to be used in biomedical applications. It incorporates a negative feedback system. The proposed sigma-delta modulator consists of integrator, comparator and D flip-flop. A 1-bit DAC is added to the system in the feedback loop. Fabricated in 180nm CMOS process, the modulator occupies an area of only 0.075 mm2. Also the modulator has power consumption of only 1.768mV from 1.8V supply.**

Keywords—SDADC, two stage op-amp, summer integrator, comparator, flip-flop, DAC, modulator

I. INTRODUCTION

The signals that are available in the environment are basically analog signals. Biomedical or bio-potential signals are the signals that are extracted out from human body. These signals are very minute and require highly accurate measuring devices for their analysis. The frequency range of biomedical signals range from DC to several Kilo Hertz and the amplitude vary between milli-volts to micro-volts. The frequency and amplitude of some different types of bio-potential signals are summarized in Table I [1].

TABLE I. MEDICAL AND PHYSIOLOGICAL PARAMETERS

Type of Bio-Potential Signal	Amplitude	Frequency
Electro-oculogram (EOG)	50 – 3500 µV	0 – 50 Hz
Electroencephalography (EEG)	5 – 300 µV	0 – 150 Hz
Electrocardiography (ECG)	0.5 – 4 mV	0.01 – 250 Hz
Electromyography (EMG)	0.1 – 5 mV	0 – 10000 Hz

The general block diagram of the front-end of biomedical system is as shown in Fig.1[2]. It includes an instrumentation amplifier (IA), an anti-aliasing filter (AAF), an analog-to-digital converter (ADC) and a digital signal processor (DSP).

Instrumentation amplifier amplifies the biomedical signal to fit the ADC input range by removing the undesired low frequency noise. Anti-aliasing filter avoids signal aliasing. Analog-to-digital converter is used to convert the analog signal into its corresponding digital values. Digital signal processor is used for back-end signal processing [3].

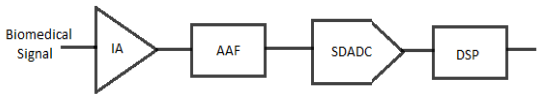

Fig. 1. General Front-end of biomedical system

The SDADC was first introduced by Inose in 1962. SD converters are ideal for converting signals over a wide range of frequency from DC to megahertz with high resolution. Due to oversampling the quantization noise will be spread over a wide bandwidth. This does not affect the total quantization noise, but reduces some noise at the band of interest. By oversampling the signal with frequency that is much greater than the signal bandwidth, it is possible to shape the frequency quantization noise for the feedback loop which separates the noise from signal band.

This paper is organized as follows. Section II presents the concept of SDADC modulator. In section III, the system description containing the different sub-circuits of the modulator is discussed. Then a complete design of SDADC modulator with function schematic layout and simulation using Cadence are described in Section IV. Conclusions with comparison table of most popular designs with current work (Table II) are drawn in Section IV.

II. CONCEPT OF SIGMA-DELTA MODULATOR

There are many different types of ADC architecture available. Some of them are flash ADC, pipelined ADC, SAR ADC, folding and interpolating ADC and dual slope ADC. All these ADC's can achieve resolution of only upto

8-20 bits, but Sigma-delta ADC (SDADC) can achieve resolution upto 32bits and is also able to operate in low frequency [4]. SDADC is commonly used because of its high resolution for the accurate conversion of weak bio-potential signals.

SDADC consists of two blocks: Modulator, which is the analog block and a Digital Decimator, which is the digital block. Thus SDADC is a mixed signal converter. The modulator being the analog block consumes more power when compared to the digital decimator. Fig.2 shows the block diagram of SDADC modulator.

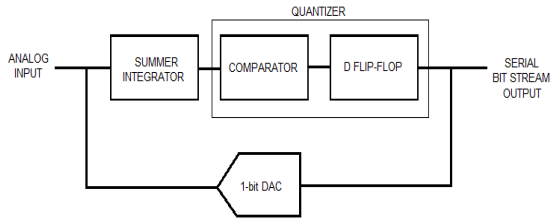

Fig. 2. Block diagram of SDADC modulator

The SDADC modulator consists of a Summer Integrator, Quantizer and a 1-bit DAC. The quantizer is a Comparator followed by D flip-flop.

The signal input is one of the inputs to the integrator. It takes the difference of the input signals and adds this value to the previously present value. The signal is then amplified and fed as input to the comparator. The comparator compares the signal level with the reference voltage producing a stream of binary ones and zeros.

D flip-flop basically performs the operation of sampling and is responsible for producing serial bit stream output of the modulator. This bit stream is then converted into parallel 8-bit stream using digital decimator. The 1-bit DAC produces an analog signal at the output which is given to integrator as a negative feedback so that the system maintains stability.

III. System Description

A. *Operatinal Amplifier*

Op-amp is critical in achieving high gain-bandwidth which is the main requirement to enhance the modulation performance. Op-amp has to be designed to consume less power to make it suitable for biomedical use. The schematic of op-amp implemented using Cadence is shown in Fig.3.

The first stage of the op-amp consists of a differential amplifier which amplifies the difference of the input signals. The second stage of the op-amp is the common source amplifier. The gain at the first stage of op-amp is only 33 dB which is very much less than the desired gain. Thus second stage is used. In the proposed two stage op-amp, an overall gain of 79 dB is obtained.

B. *Summer Integrator*

The integrator ramps up or down depending upon whether the difference is being fed are positive or negative. The basic building block of integrator is an op-amp. The summer integrator is the combination of op-amp connected to low pass RC filter whose output signal is time integral of its input signal.

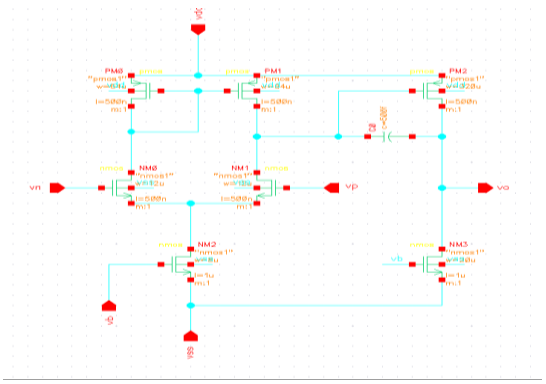

Fig. 3. Schematic of two stage op-amp

The schematic of integrator implemented using Cadence is shown in Fig.4. The current through the input resistor also produces a complementary current flow through the series capacitor due to virtual ground condition of an op-amp. This results in charging or discharging of capacitor over time. Also input current does not vary with capacitor charge due to connection of resistor and capacitor to virtual ground and this also maintains linear integration.

The ideal design of an op-amp integrator results in infinite DC gain. To prevent this, a large feedback resistor of 1MΩ in parallel with feedback capacitor of 200pF is connected. This limits both the DC gain and output drift to finite value. The transient response of the integrator with sinusoidal input gives a phase shift of 90 degree at the output. This can be observed in Fig.5.

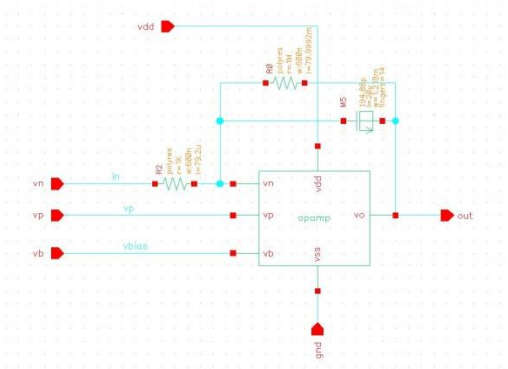

Fig. 4. Schematic of summer integrator

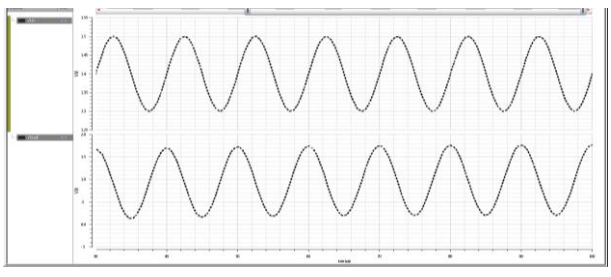

Fig. 5. Transient response of summer integrator

C. Comparator

The proposed comparator is designed for faster transition and lower power consumption. The comparator is implemented using a differential amplifier followed by an inverter. The input of the comparator, which is the output of integrator, is compared with the reference voltage of 1.4V. Fig.6 shows the schematic of comparator.

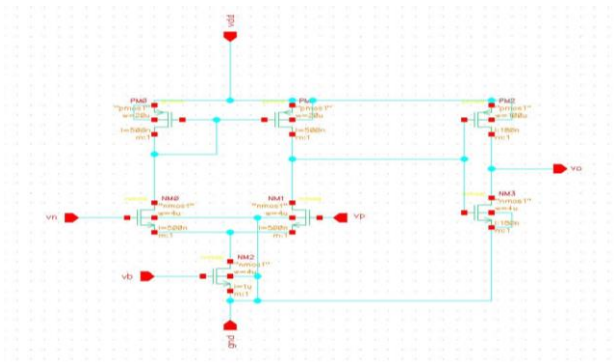

Fig. 6. Schematic of comparator

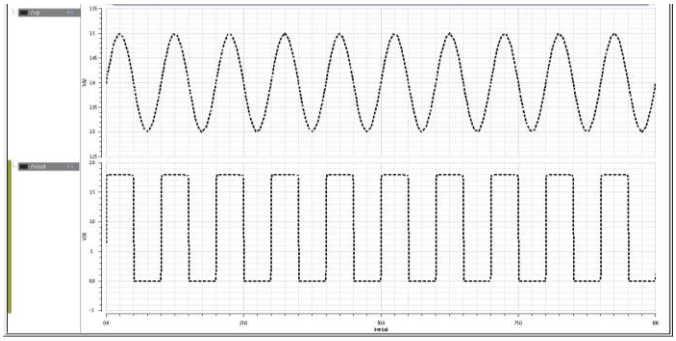

Fig. 7. Transient response of comparator

If the input is greater than 1.4V, the output rises to positive saturation level of 1.8V. If it is less than 1.4V, the output falls to negative saturation level i.e., 0V. The transient response of comparator is shown in Fig.7.

D. D flip-flop

The comparator and D flip-flop together form the quantizer. The D flip-flop in our design operates at lower frequencies. It is mainly used to sample the input signal. The schematic of D flip-flop is shown in Fig.8. The transient response simulated using Cadence, as shown in Fig.9 shows that the output follows the input at the rising edge of clock.

E. 1-bit DAC

For high resolution DAC accuracy is one of the major problems that it encounters. A single bit system can be used to overcome the accuracy problem. The 1-bit DAC is used to provide negative feedback to the integrator to maintain the overall stability of the modulator. It is implemented using the two stage op-amp. Its operation is to reconstruct the analog signal. A reference voltage of 1.4V is set to shape the analog signal at its output.

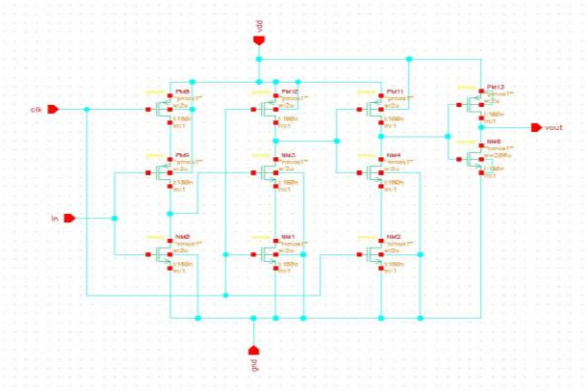

Fig. 8. Schematic of D flip-flop

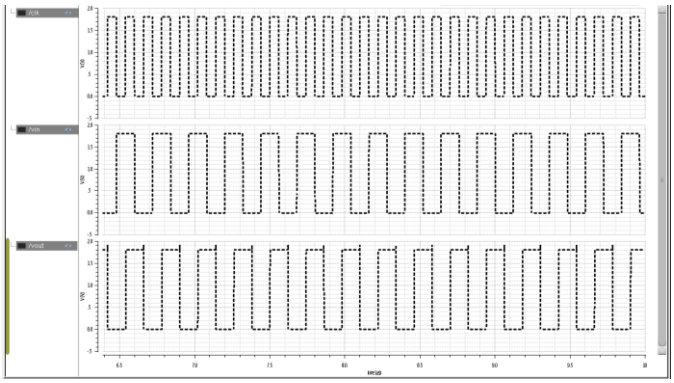

Fig. 9. Transient response of D flip=flop

IV. Layout and Simulation Result

The modulators that are designed using feedback structure greatly reduce the power consumption and improve stability. The proposed SDADC modulator is designed using op-amp and hence is a continuous time modulator. Fig. 10 shows the schematic of the proposed sigma-delta modulator.

Fig. 11 shows the simulated transient response of the modulator simulated using Cadence. Fig. 12 shows the layout of proposed SDADC. The core area is 0.075mm^2. The analog parts are covered by guard rings to eliminate substrate noise. The modulator is suitable for biomedical applications.

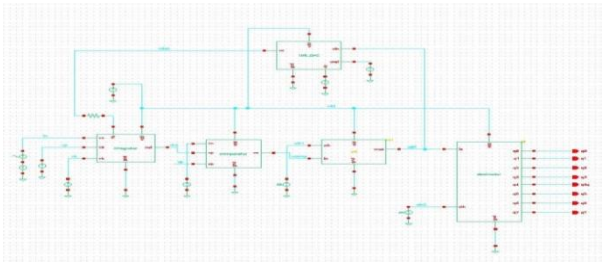

Fig. 10. Schematic of proposed sigma-delta modulator

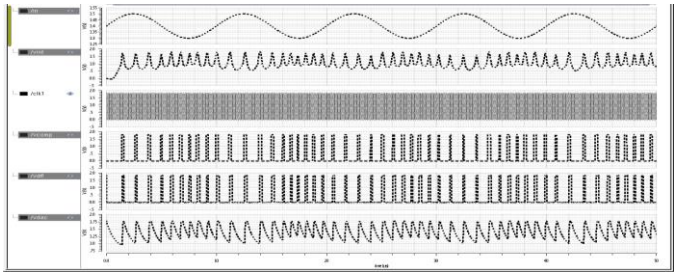

Fig. 11. Transient response of Modulator

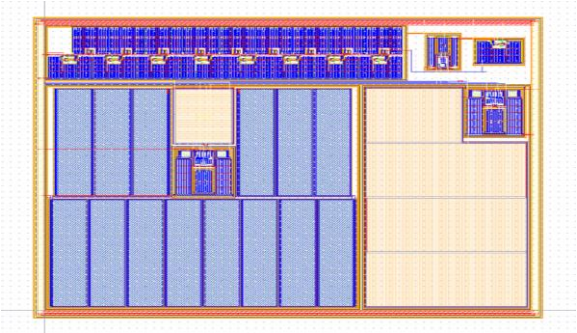

Fig. 12. Layout of proposed sigma-delta modulator

TABLE II. COMPARISON OF CURRENT WORK WITH OTHER WORKS

Reference	Resolution (bits)	Power (mW)	Technology (nm)	Area (mm2)
[5]	14	89.6	180	1.8
[6]	8	6.6	600	-
[7]	15	3	350	1.68
This work	8	1.768	180	0.075

V. CONCLUSION AND FUTURE WORK

In this paper, a first order sigma-delta modulator is presented and it is seen that the modulator can work in proper condition at a resolution of 8 bits. Given a power supply of 1.8V, the modulator is designed to consume a total power of only about 1.768mW. A comparison between the current work with the most popular published works is shown in Table II. Our design is implemented in 180nm CMOS technology using Cadence tool and it is observed thatthe total area consumed by the SDADC layout is only about 0.075mm^2. The simulation results show that the technique is promising and achieves an excellent performance. A higher resolution second order modulator can be designed for much better accurate measurements.

REFERENCES

[1] J. G. Webster, Medical instrumentation: Application and Design, New York: Wiley, 1995, pp. 10-11.

[2] E. López-Morillo, R. G. Carvajal, et al., “A 1.2-V 140-nW 10-bit Sigma-Delta Modulator for Electroencephalogram Applications,” IEEE Transactions on Biomedical Circuits and Systems, Vol. 2, pp. 223-230, Sep. 2008.

[3] Chih-Han Hsu, Kea-Tiong Tang, “A 1V Low Power Second-Order Delta-Sigma Modulator for Biomedical Signal Application,” International Conference of the IEEE EMBS, Japan, July, 2013.

[4] Aneeciya Mathew, Prameela B, “A Low Power Delta Sigma CT Modulator for Biomedical Application,” ICIIECS, 2017.

[5] José Barreiro da Silva, “High-Performance Delta-Sigma Analog-to-Digital Converters,” A THESIS submitted to Oregon State University, Presented July 14, 2004.

[6] Boujelben S, Rebai Ch., Dallet.D, Marchegay Ph., “Design and implementation of an audio analog to digital converter using oversampling.techniques,” IEEE, 2001.

[7] Sangyong Lee, Wonki Park, Kyongwon Min , Byong-Deok Choi,Sung Chul Lee, “Sigma-Delta (Σ-Δ) ADC for Complex Sensor Applications,” International Technical Conference on Ci, Vol.2009 No.7, 2009.

[8] Yi Yang, Changzhi Li, David M Binkley, “Continuous-time Sigma-Delta Modulator Design for Wireless Biomedical Sensing Applications,” IEEE, 2010.

[9] Wenbin Bai, Yifei Wang, Zhangming Zhu, “A 0.8-V 1.7μW 25.9-fJ Continuous-Time Sigma-Delta Modulator for Biomedical Applications,” IEE, 2016.

[10] J. B. da Silva, “High-performance delta-sigma analog-to-digital converters,” Oregon State University, vol. 28, pp. 92–94, Jan 2004.

[11] Radhouane LAAMIJI, Mohamed MASMOUDI, “High-Performance 8-bit Modulator used for Sigma-Delta Analog toDigital Converter,” IEEE, Tunisia, December, 2014.

[12] W.I.I.Restu,B.W.M.Nasir,andM.M.B.I.Reaz,“Lowpowerandhighspeedcmos current comparators,” in 2016 International Conference on Advances in Electrical, Electronic and Systems Engineering (ICAEES), Nov 2016, pp. 539–543.