A 2.4GHz Low Power, High Gain CMOS RF LNA in 90nm Technology

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***Abstract*-This proposed Low noise amplifier (LNA) consists of a simple design with three common source (CS-CS-CS) stages and cascode as output stage to achieve excellent gain, low power and good figure of merit (FOM) is presented. The inductorless low noise amplifier is designed for low cost and less area consumption on 90nm technology. A 2.4 GHz low noise amplifier has post layout results simulated for the temperature range of -30 to +50 degree Celsius with the performance featuring a record gain of 34 dB without output matching and the noise figure of 3.3-4.7dB. Cascode as end stage of amplifier provides a good reverse isolation with better overall bandwidth of 27.3 GHz, while consuming 1.56mW of power from 1.2v supply and the area is 26.4um by 13.6um with the capability of supporting 802.11b WLAN and Bluetooth applications.**

Keywords- CMOS; inductorless; low power; WLAN; 2.4GHz

I. INTRODUCTION

In recent years high speed wireless standards such as Bluetooth, wireless local area network (WLAN) and GPS etc. have boosted the rapid enhancement and development of the portable electronics. To keep the overall solution cost of portable devices low, the wireless transceiver should be highly integrated with the baseband as a system-on-chip (SoC) solution, preferably using a low-complexity CMOS process [1]. RF Integrated Circuits (RFICs) using inductors are preferred for reducing noise in LNA, but the inductors are expensive and it requires large chip area with more power consumption. Removing inductors for a good LNA is challenging task. As the scaling urge reduction in supply voltage with increase in noise. The LNA design involves tradeoffs between noise-figure (NF), gain, power dissipation, input matching, and harmonic content in the output signal [1]. For example few techniques with and without inductors such as, Inductorless gain enhanced noise cancelling technique [2], parasitic insensitive linearization topologies [3], low power inductorless double g_m enhancement [4], current reuse g_m boosted CG LNA [5], power efficient noise suppression technique [6]. However such techniques individually suffers from disadvantages like more power consumption, inadequate noise, less gain, large integrated chip area and imperfect layouts increases the design complexity. The noise cancelling techniques increase power consumption with area.

The design is focused on high gain at noise reducing condition with low power and good reverse isolation; which is achieved by three stage common source and cascode as output stage. The inductorless design has low complexity with less area requirement. And considered supply voltage variation as well as temperature variation. A supply voltage variation considered of 5% and temperature variation of -30℃ to +50℃. A simple design with the excellent gain, low power, better figure of merit, acceptable linearity and noise figure has achieved.

II. DESIGN OF THE 2.4GHZ CMOS LNA

A narrow band LNA according to the concept of fig.1 was designed in a 90nm standard CMOS process. The work done was aimed at high gain and low power over a frequency of 2.4GHz. High sensitivity applications were targeted with 2.4GHz frequency. So, no attempt made for linearity as there is tradeoff between gain and linearity.

The fig.1 shows schematic design Low power, high gain CMOS RF LNA for 2.4GHz LNA. It consists of three common source stages and cascode as end stage. Common source was used in initial stages to keep noise less with input impedance matching of 50 ohm with increase in gain. The end stage provides a good reverse isolation using cascode stage. A load capacitance of 50fF was connected externally. The MOSFETS used were of 30um width for first three common source stages. The design made simple with no linearity improvement, no noise reduction techniques and no inductors just to avoid complexity in 90nm CMOS technology

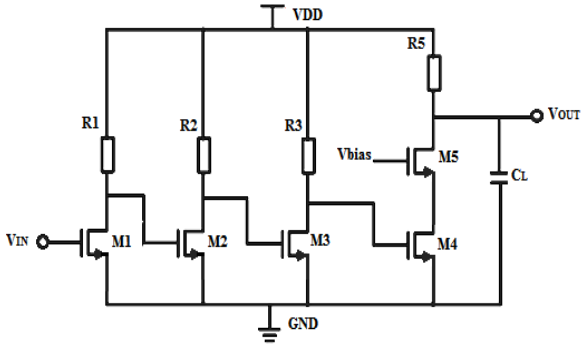

Fig.1. Schematic of RF LNA proposed.

Noise factor for LNA is calculated using,

$$NF = 1 + \frac{\overline{V_{n,out}^2}}{A_v^2} x \frac{1}{4KTRs} \quad (1)$$

Noise figure is measured for all stages with respect to the input resistance Rs. A modification of load resistance of each stage in layout reduced the power from 8.7mW to 1.56mW with sacrificing 0.6dB of noise considering nominal temperature with reduction in gain as well.

III. Results And Analysis

The proposed LNA has designed in 90nm RF CMOS technology. Without output matching the design has achieved 34dB of gain through post layout with RC extraction over a temperature range of -30℃ to +50℃ at the narrowband frequency of 2.4GHz. The fig.2 shows simulated results for voltage gain versus frequency considering temperature. At 2.4GHz frequency the gain is obtained varying temperature. The nominal temperature gain obtained is 37dB. The lowest LNA gain obtained of 34dB at the 50℃ temperature, with maximum gain of 39dB at the -30℃ temperature. And the gain of 38dB obtained at 0℃ temperature. The overall bandwidth obtained at unity gain is 27.39GHz. The LNA proposed has a capacity to work with positive gain at the obtained frequency. Fig.2 shows the obtained magnitude of output and input of the proposed LNA. The proposed LNA has not matched the output resistance but with input matching of 50ohm resistance LNA has achieved the low power and high gain with the CMOS technology. The gain obtained with less increased at initial stages with reduction in noise simultaneously. And increased more gain at end cascode stage with negligible noise.

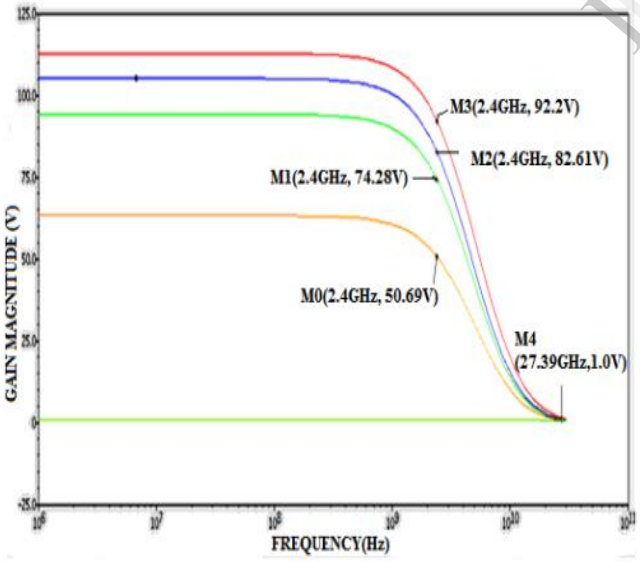

Fig.2. Simulated results for voltage gain magnitude versus frequency.

The calculated noise has obtained about 3.7dB ithout considering modification in layout which has changed the potential levels of all MOSFETS with positive effect on power reduction.

The noise figure simulated over a frequency range of 1GHz to 6GHz is as shown in fig.3

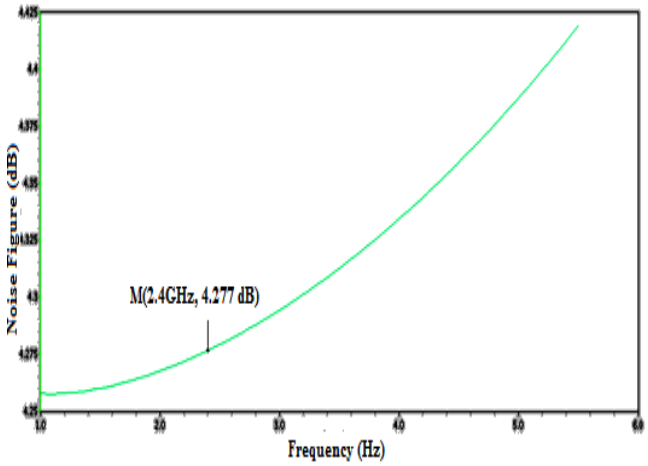

Fig.3. Simulated result for Noise figure versus frequency.

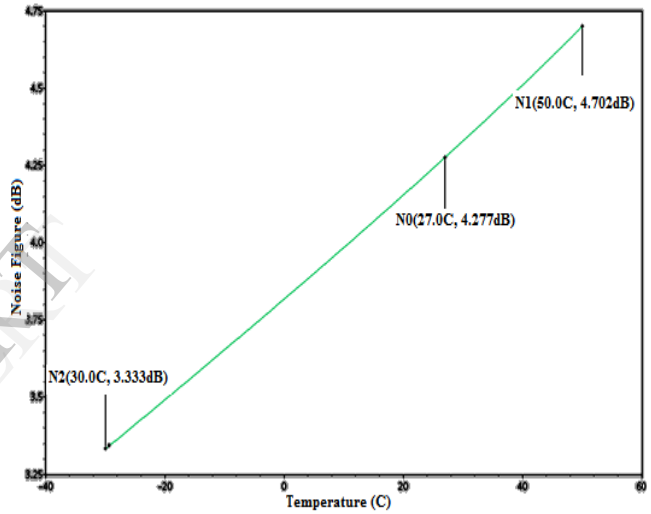

Fig.4. Simulated result for noise figure versus temperature.

The simulated noise obtained at 2.4GHz is 4.27dB and is about 4.4dB at 5GHz frequency. The noise figure simulated over a temperature range of -30℃ to +50℃ is 3.33dB to 4.7dB as shown in fig.4. A 5 % variation in supply voltage reduces gain to 22dB with overall bandwidth to 10.45GHz with same noise figure.

The performance comparing gain and noise over a temperature range of -30℃ to +50℃ at 2.4GHz is shown in table 1. The comparison is performed specific at temperatures points.

Table 1. Gain and Noise with variable temperature

Frequency GHz	Output/ Input	Temperature ℃	Gain (dB)	Noise (dB)
2.4	Output	50	34	4.7
2.4	Output	27	37	4.2
2.4	Output	0	38	3.8
2.4	Output	-30	39	3.3

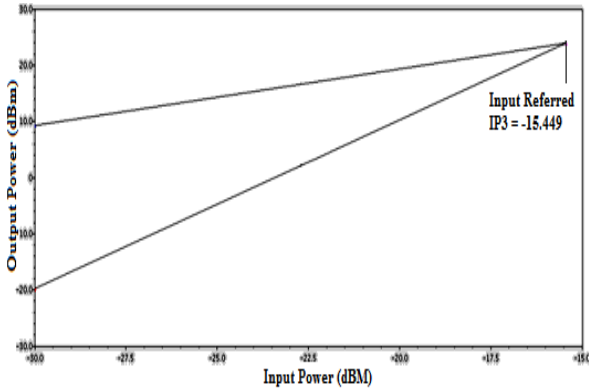

Fig.5. Simulated result for IIP3 of RF LNA at 2.4GHz.
The third order input referred intercept point is shown in fig.5. To get OIP3,

$$OIP3\ (dBm) = Gain\ (dB) + IIP3\ (dBm) \quad (2)$$

The third order output referred intercept OIP3 obtained is about 22dBm.

As there is tradeoff between gain and linearity the high gain reducing linearity. The LNA has ability to provide -15.4dBm of linearity with a gain of 37dB at the nominal temperature.

The area required for LNA with the post layout simulation is 26.4um x 13.6um, less area due to no use of inductor.

Table 2.
Performance comparison with published LNAs

	This Work	[1] FB	[1] BC	[2] 1st LNA	[2] 2nd LNA	[3] CS LNA	[3] Cascode LNA	[4]	[5]	[6]
Technology [nm]	90	180	180	65	65	90	90	130	130	180
Bandwidth [GHz]	2.4	5	5	10	5.2	58-65	54-69	0.1-2.7	3.1-4.8	1.4
Gain [dB]	37*	11	9.3	10.5	10.7	11.3	13.2	20	13	14.1
Noise Figure [dB]	4.27	0.95	1.9	2.7-3.3	2.9-5.4	4.8	4.4	4	3.5•	4
P_{DC} [mW]	1.56	12	12	13.7	7	10.8	14.4	1.32	3.4	1.53
IIP3 [dBm]	-15.44	5	6.5	-3.5	-6	0	11	-12	-6.1	2
Supply [V]	1.2	1.5	1.5	1	1	1.2	2.4	1.2	1	1.3
Area [mm²]	0.000359 **	0.2925	0.2925	0.02	0.03	0.27	0.3	0.007	0.4^	0.075
FoM [dB/mW]***	23.98	0.92	0.78	0.76	1.52	1	0.08	15.15	3.82	9.21
Inductor	NO	YES	YES	NO	NO	YES	YES	NO	YES	NO

* Gain obtained without output matching.
** Post layout simulated area.
a Minimum NF considered
*** Figure of Merit (FoM) is obtained by ratio gain to output power.
^Area including bonding pads and external filter.

IV. Conclusion

A 2.4GHz single ended CMOS RF LNA for Bluetooth and for 802.11b WLAN applications is presented. It achieves a power consumption of 1.56mW. The LNA design has achieved 4.2 dB NF and a large voltage gain of 37dB with IIP3 of -15.44dBm. Inductorless post layout implementation results the area of 26.4um x 13.6um.

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