A 9-Transistor Nanoscale Cmos Memory Cell by Using New Hardening Technique

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Abstract*-Tolerance to soft errors has become a strict requirement in today's nano scale CMOS designs. This paper proposes a new hardening design technique for CMOS memory cell at 120nm feature size. The proposed 11T hardened memory cell overcomes the problems associated with the previous designs by utilizing novel access and refreshing mechanisms. This paper proposes a new hardening design for an 11 transistors (11T) CMOS memory cell at 120 nm feature size. We analyze new hardening design-based differential-sensing static random access memory (SRAM) bit cells. In this paper we are going to propose a new SRAM bit cell for the purpose of read stability, less power consumption, less area than the existing hardened memory cell circuit design. Design and simulations were done using DSCH and Micro wind.*

Index Terms—Memory design, nanotechnology, radiation hardening*.*

I. INTRODUCTION

As nanotechnology is fast moving from explorative to industrial practice, the operation of CMOS circuits at nanoscale ranges is been extensively analyzed. These circuits are manufactured and integrated at high device density; however considerable attention must also be paid to other performance metrics (such as power consumption and delay). The scaling of CMOS technology has been made possible by improved fabrication and design techniques; the reliable operation of nano scaled CMOS circuits however, is still a concern. Due to the lower V_{dd} and the smaller node capacitance, the amount of charge stored on a circuit node is becoming increasingly smaller, thus making circuits more susceptible to spurious voltage and charge variations caused by *externally induced phenomena*, such as cosmic ray neutrons and α-particles [1].These energy particles travel through the silicon bulk and create minority carriers that may be collected by the source/drain diffusion, thus altering their voltage value [2]. This is particularly deleterious for storage cells, such as memories and latches because data integrity is affected [3].

An example of an hardening design approach has been reported in [5] and is commonly known as DICE. The DICE cell is shown in Fig.1 and uses twice the number of transistors of a standard storage cell (i.e. 12T vs. 6T) to achieve tolerance against a TF affecting any single node. The advantage of this design is that it does not require an increase in the size of the transistors or the capacitance of some nodes. In the DICE cell, the single node that is affected by a TF can be driven back to its previous state by the other transistors. A different hardened memory cell requiring 11 transistors (i.e.11T) has been proposed in [7]; the single node affected by a TF can be driven back by using novel access and refreshing circuits. Theoretically, these two cells are immune to any amount of charge collected at any single node.

This manuscript is organized as follows. Tolerance of existing hardened memory designs are analyzed in Section II. A new 9T design of the hardened memory cell is presented in Section III. Relevant figures of merit such as area and a power/delay are analyzed and assessed in Section IV. Section IV also presents a simulation-based assessment of variations and their effects on the proposed 9T SRAM cell. Section V concludes this manuscript.

II. EXISTING HARDENED MEMORY DESIGNS

In this section, the single node hardened capabilities of two existing memory cell designs (i.e. DICE and 11T) are evaluated. The charges on the primary and secondary nodes are found to assess by MICROWIND simulation the tolerance of these designs to this new scenario.

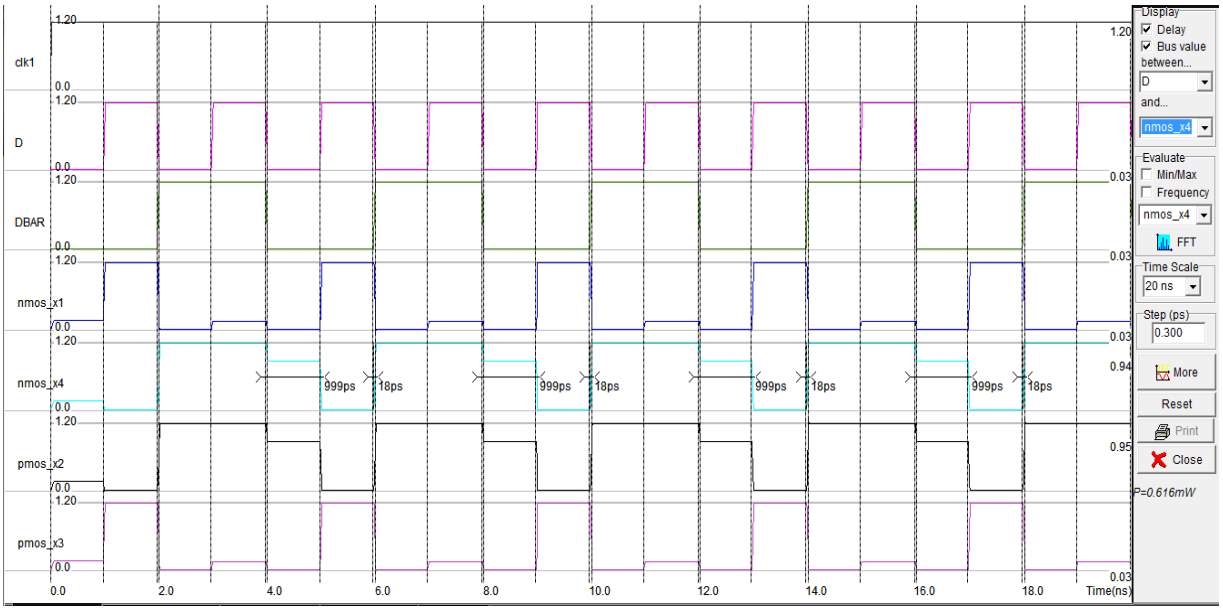


Figure 1. Wave form of DICE cell

A. DICE Cell

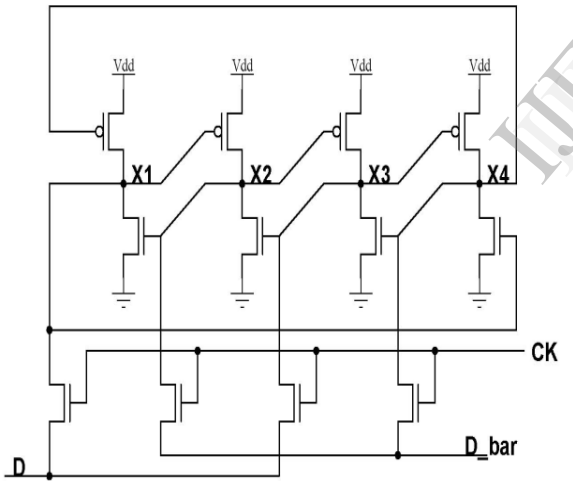


Figure2. DICE cell

As shown in Fig.1, the DICE cell uses twice the number of transistors of a standard storage cell [5]. The DICE cell has two states, the 0 state (X1=0, X2=1, X3=0, X4=1) and the 1 state (X1=1, X2=0, X3=1, X4=0). In any of these two states upon the occurrence of a soft error (on a single node), the state of the node is always driven back to its original value. For example, in the 0 state, if the node struck by a particle is X2, the state of X2 goes from 1 to 0. However, this strike will not propagate along the feedback loop due to the interlocked configuration. Meanwhile, the state 0 stored in X1 can restore the state of X2; however, when a strike occurs on multiple nodes, the DICE cell is unable to drive back the original state. For example, in the 0 state, if the node struck by a particle is X2, the state of X2 goes from 1 to 0. Meanwhile, if node X1 is also affected by the strike, then it goes from 0 to 1. In this case, due to the strike on X1, the state of X2 will not be restored and a soft error is said to occur. Simulation results show that if there is a strike on X1, a very small amount of charge on X2 can change the state of the DICE cell.

B. 11T Hardened Cell

A single node hardened memory cell has been proposed in and shown in Fig.3. The basic storage element used in this memory cell relies on the hardening scheme of. In the memory cell of Fig.3, its feedback loop is cut off by the transistors M5, M6, M7, and M8, i.e. for a single node upset, a transient pulse cannot be propagated along this loop back to its starting point. The gates of the PMOS and NMOS transistors are separated from the hardened nodes a1 and a2. Signal regeneration at a1 and a2 is controlled by the transistors M5 and M8. In this cell, the access pass gates (M1 and M2) are connected to node d instead of nodes a1 and a2 to prevent the high leakage current from BL to change the data stored in the memory cell.

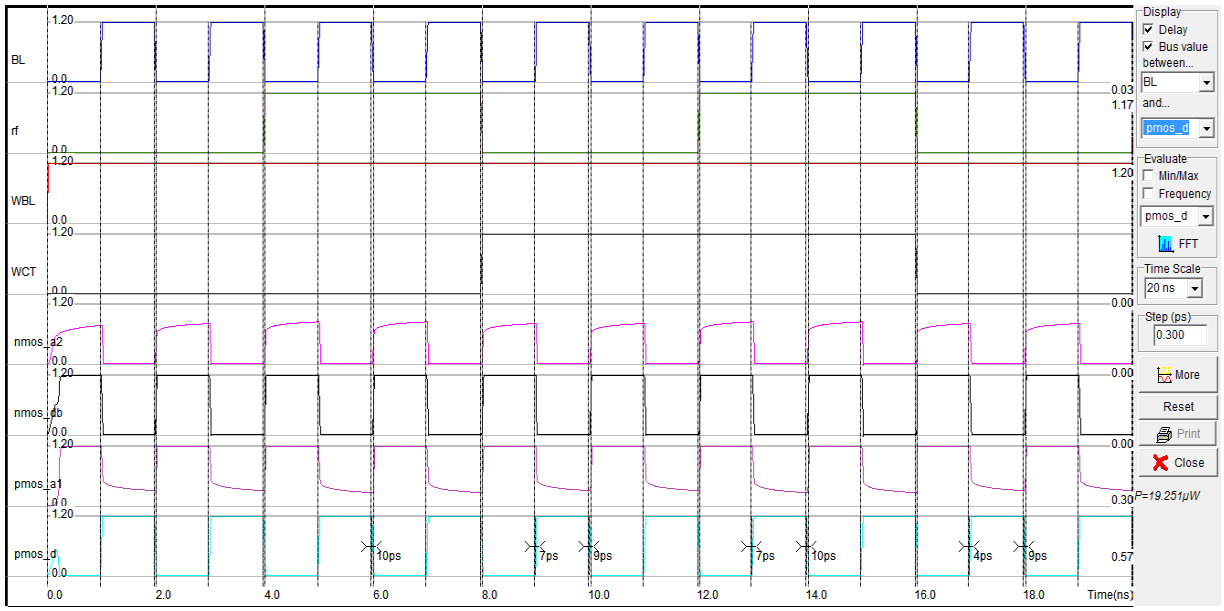


Figure3:Wave forms of 11T SRAM

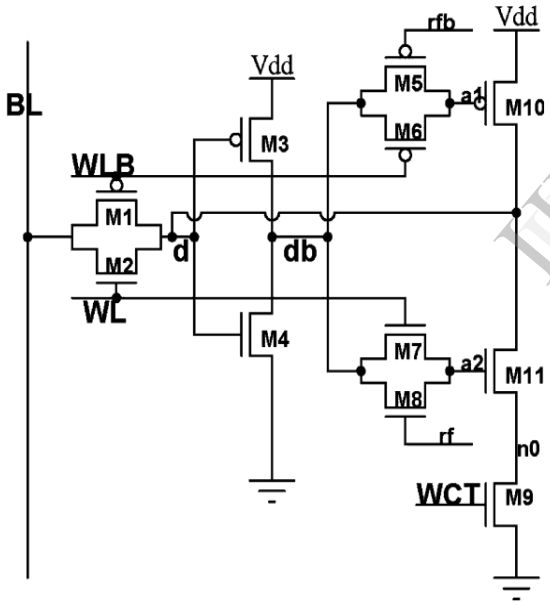
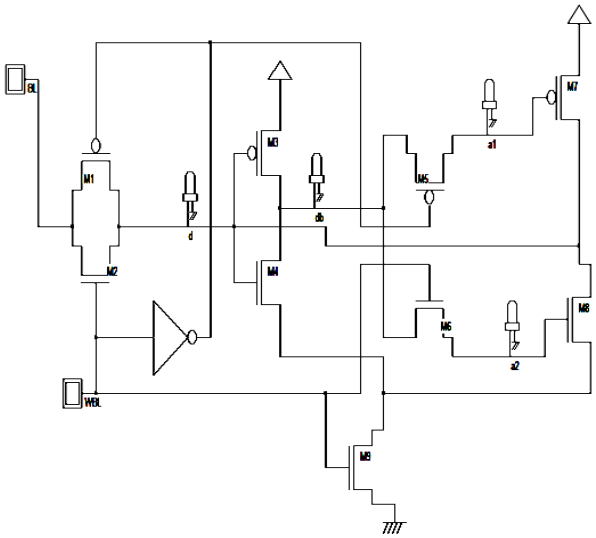


Figure4.11T hardening memory cell.

A TF on a1 or a2 will not change the data stored in the memory cell. A NMOS write control transistor is added to this memory cell for the write operation. As discussed in, a single ended SRAM cell operates correctly when writing a "0" as data, but it may encounter problems when writing a "1". Therefore, a write control transistor is added between M11 and ground to write a "1". With this write control transistor, the hardened memory cell consists of eleven transistors, i.e. one transistor less than the DICE cell configuration. The 11T memory cell is unable to restore the state of the node when a single event causes a multiple node upset. Similar to the DICE cell, the 11T cell has two states, the 0 state (d=0, db=1, a1=1, a2=1) and the 1 state (d=1, db=0, a1=0, a2=0). If nodes a2 and d are affected by a strike, the state of the 11T memory cell will be changed, i.e. it has limited tolerance under a single event with a two node upset.

III. PROPOSED 9T HARDENED MEMORY CELL



Figur5:Proposed 9T hardened memory cell.

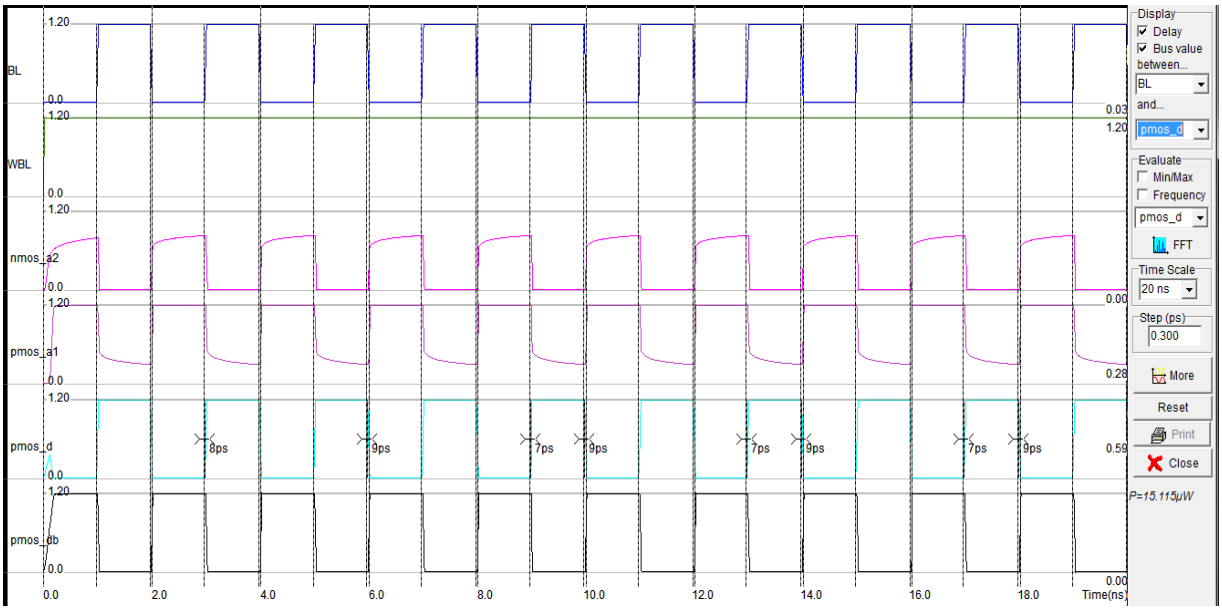


Figure6:Wave form of proposed 9TSRAM

A new hardened memory cell is proposed in this paper to improve the multiple node upset tolerance. Its design is shown in Fig.3. In the 11T memory cell, the critical pair of the cell is "a2 1->0, d 0->1", i.e. when node a2 stores a state 1 and a charge is collected on the primary node a2, a transient fault causes the node to change from state 1 to state 0. At the same time under this scenario, charge is also collected by the secondary node d; this causes the node to change from state 1 to state 0. In order to resolve the conflicting read versus write design requirements in the proposed 9T hardening Memory Cell, the new hardened principle for the cross-coupled inverter pair is applied. A M9 transistor is used to modulate the switching threshold of an inverter depending on the direction of the input transition, , the feedback mechanism is used only in the pull-down path, as shown in figure1.During input transition, the feedback transistor tries to preserve the logic "1" at output node by raising the source voltage of pull-down nMOS . This results in higher switching threshold of the inverter with very sharp transfer characteristics.

The total leakage power in SRAM cell is determined by the Contribution of leakage currents in each transistor of SRAM cell. The leakage current has two main sources, sub-threshold leakage current and gate leakage current (leakage current is dominated by sub-threshold leakage), Band to Band Tunnelling leakage current is very small for existing Technologies and that can be ignored .As the oxide thickness of gate is decreases the gate leakage current of transistor increases exponentially and when gate oxide thickness reaches 3nm and below the gate leakage current comes to the order of sub-threshold leakage current. The gate leakage current is also increases with gate oxide voltage. Due to process variation, variability in oxide thickness ignoring, so the variability of gate voltage is only possible consideration for analysis of gate leakage current. So for getting low static power a nine-transistor SRAM cell structure has been proposed. In proposed 9T-SRAM cell, two transistors are reduced to the cell, to improve the stability in the read mode, the cell stability is improved at the cost of small decreasing the cell area. The proposed 9T-SRAM cell is two techniques based design that reduces the gate leakage current and static power dissipation in the SRAM cells.

The proposed 9T hardened SRAM cell is reduced the area, power consumption and delay when compared with the previous memory cells such as DICE cell, 11T memory cell. The total comparison is discussed in next section.

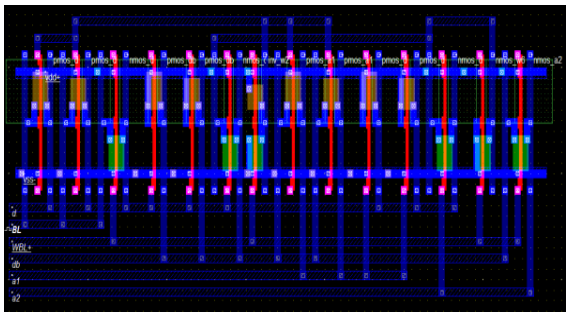


Figure7: layout of proposed 9T hardened memory cell.

IV. PERFORMANCE ANALYSIS OF SRAM ARCHITECTURAL CO-DESIGN

This section resents the performance analysis of SRAM bit cells such as Dice Cell, Proposed Hardening Memory cell and 9T based cell designs. The simulations are carried out in micro wind using 120nm technology.

TABLE I. COMPARISONS OF MEMORY CELLS

Sram	Power (mw)	Delay (pS)	Area (μm^2)
DICE	0.616	999	1.4688
11T HARDENING CELL	0.019	10	1.3464
PROPOSED 9 T	0.015	8	1.1016

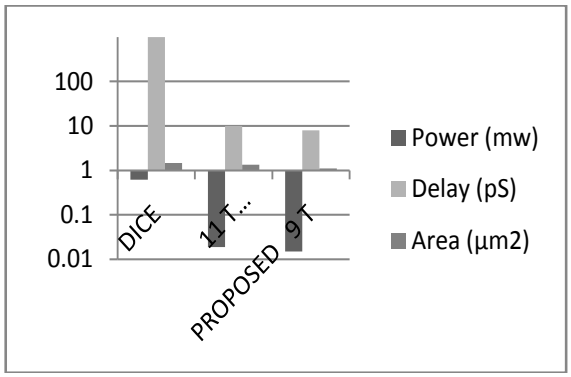


Figure8:Comparison of SRAM's.

V. CONCLUSIONS

Performance comparison of various SRAM bit cells such as Dice Cell, Proposed Hardening Memory cell and 9T based cell designs is performed. It has been shown that in terms of leakage power reduction and energy, 9T SRAM cell has the best performance in comparison to dice and proposed hardened cell. In terms of robustness to variation in temperature.

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