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A Cascaded H-Bridge Multilevel Inverter Topology with a Bidirectional Switch

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***Abstract*—** In recent years, multilevel inverters (MLIs) have emerged to be the most empowered power transformation technology for numerous operations such as renewable energy resources (RERs), flexible AC transmission systems (FACTS), electric motor drives, etc. MLI has gained popularity in medium- to high-power operations because of numerous merits such as minimum harmonic contents, less dissipation of power from power electronic switches, and less electromagnetic interference (EMI) at the receiving end. The MLI possesses many essential advantages in comparison to a conventional two-level inverter, such as voltage profile enhancement, increased efficiency of the overall system, the capability of high-quality output generation with the reduced switching frequency, decreased total harmonic distortions (THD) without reducing the power of the inverter and use of very low ratings of the device. Although classical MLIs find their use in various vital key areas, newer MLI configurations have an expanding concern to the limited count of power electronic devices, gate drivers, and isolated DC sources. In this paper, a new topology for a cascaded multilevel inverter with a bidirectional switch is presented. A deduction in the cascaded H-bridge inverter switch count of seven against eight compared to a conventional multilevel inverter and two dc supplies constitutes the proposed five level inverter. The reduced switch inverter can be utilized in electric vehicle drives and renewable energy systems.

Keywords— cascaded inverter, multicarrier modulation, total harmonic distortion.

I. INTRODUCTION

Multilevel inverters are DC-AC static power converters exhibiting at their output terminals more than two-level voltage waveforms. Nowadays they find increasing attention especially for medium-voltage and high-power applications [1, 2]. In the mid 1970's, Baker and Bannister have proposed the first multilevel inverter [3]. It consists of series connected single phase H-bridges. Later, Nabae et al. developed another multilevel inverter called 3L-NPC (Neutral Point Clamped diodes) [4]. In such topology, several diodes ensure levels construction of output voltage by linking capacitive sources to switches. Following the NPC, a Flying Capacitors topology (FLC) was proposed by putting clamping capacitors instead of diodes [5]. Therefore, cascaded H-bridge, NPC and FLC are the basic and most used multilevel inverters. After that, multitude of derived and hybrid multilevel topologies were introduced [6-16]. However, they still on the shadow of the major multilevel configurations previously stated. The most industrialized multilevel topologies are the three-level NPC (3L-NPC), the cascaded H-bridge (MLCHB), and the four-level flying capacitors (4L-FLC) [17]. Typically, multilevel topologies have been used to overcome the limitations of conventional two-level inverters.

Particularly, the voltage stress on switching devices is decreased by putting in series power switches. The total harmonic distortion is reduced by adding steps or levels in the output voltage waveform fitted with the sinusoidal reference. In practice, this is achieved by multiplying the number of DC sources and also by considering their terminals as positions to be switched [18]. Multilevel inverters features have several other promising advantages over two level topologies such as: i) the possibility to overcome the problem related to the maximum voltage drop of the main power semiconductors. ii) Transformer-less inverter architecture desirable in renewable energy applications [19]. iii) Reduction of the common mode voltage which causes inherent damages of the bearings. iv) High resolution of the output waveforms [20, 21]. Therefore, the voltage adjustment is smooth which reduces the stress on the load, otherwise the voltage in conventional inverter varies between two values. The rating of passive filters, sometimes necessary to limit these stresses, can be also reduced. Consequently, the system wins more dynamic and allows faster regulation. v) Minimized electromagnetic interference issues [22]. Multilevel inverters applications cover mainly the variable speed area as motors drives [23-26], pumps [27], conveyors [27, 28] and electric traction [29-31]. Multilevel inverters are also used for electrical power conditioning as voltage rectifier, static compensator (STATCOM), Back-to-Back inverter connected to the network [32-35]. Recently, they are associated with renewable energy systems in photovoltaic applications and wind generation [22, 36-39]. Thanks to the development of semiconductors dedicated to high power, particularly IGBTs at 3.3 kV, 4.5 kV and 6.5 kV, the power ranges associated to multilevel inverters were significantly extended to medium and high voltages (2-13 kV). Regarding control algorithms, the frequently used techniques are Selective Harmonic Elimination (SHE) and Pulse width modulation (PWM) [40]. Advanced methods developed thereafter are improvements of those above. PWM based techniques are most relevant in industrial field including multi carriers and space vector modulation. With those techniques, we can reduce switching losses and achieve a low total harmonic distortion, so better voltage quality.

Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and MW power level. For a medium voltage grid, it is troublesome to

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connect one power semiconductor switch directly. The application of ac variable frequency speed regulations are widely popularized, high power and medium voltage inverter has recently become a research focus so far as known there are many problems in conventional two-level inverter in the high-power application. Multilevel inverter has been gained more attention for high power application in recent years which can operate at high switching frequencies while producing lower order harmonic components [1]-[6], A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel inverter system for a high-power application [7] - [12]. There are several topologies such as neutral point clamped inverter, flying capacitor based multilevel, cascaded H-bridge multilevel inverter, hybrid H-bridge multilevel inverter and new hybrid H-bridge multilevel inverter [13]-[15].

The most attractive features of multilevel inverter areas follow

1) They can generate output voltage with very low distortion and lower rate of change of voltage.

2) They can generate very low distorted input current and can operate with a lower switching frequency.

3) The voltage handling capacity of the existing devices can be enhanced in multiple folds, not disturbing the complications of static and dynamic voltage sharing that occur in series connected devices.

4) Spectral performance of multilevel waveforms is superior to that of their two- level counterparts.

5) Multilevel waveforms naturally rectify the challenges of large voltage transients that occur due to the reflections on cables, which can damage the motor windings as well as adding extra problems.

II. FIVE LEVEL MULTILEVEL INVERTER

Figure 1 shows the circuit diagram of the reduced switch five level inverter. The reduced switch topology can produce five levels of DC voltages ($2V_s$, V_s, 0, $-V_s$ and $-2V_s$). This topology requires only five fully controlled unidirectional-blocking bidirectional-conducting switches and a single bidirectional-blocking-bi-directional conducting switch and two DC sources for attaining a five-level output. The low frequency requirement of higher voltage rated switches and reduced device count are the advantages. The topology attains a 12.5 % reduction in the number of main power switches compared to conventional cascaded five level inverter

$\% r = \frac{N_c - N_r}{N_c}$, where N_c represents number of switches of conventional five level inverter, N_r represents number of switches of reduced switch five level inverter and % r represents the percentage reduction in the number of main power switches). The topology developed has the advantage of operation of higher voltage rated switches at line frequency. The developed topology requires only three active switches for a particular voltage level in comparison with activation of four active switches required for generation of a specific voltage level in conventional cascaded five level inverter.

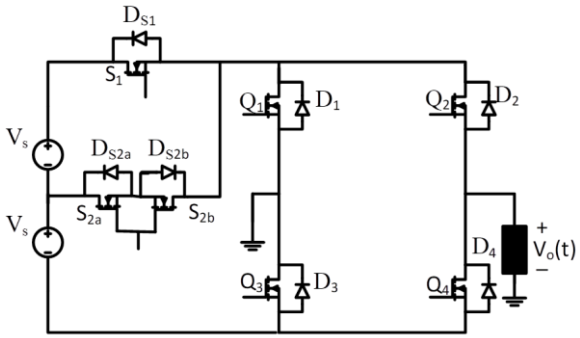

Figure 1 Power stage for new reduced switch five level topology

Figure 2 (a - e) shows the circuit diagrams for different voltage levels (modes of operation) for the new reduced switch five level topology. The diode rating has been taken based on the magnitude of five level inverter output voltage. The activated switches are represented in bold lines in each mode of Figure 2 (a - e).

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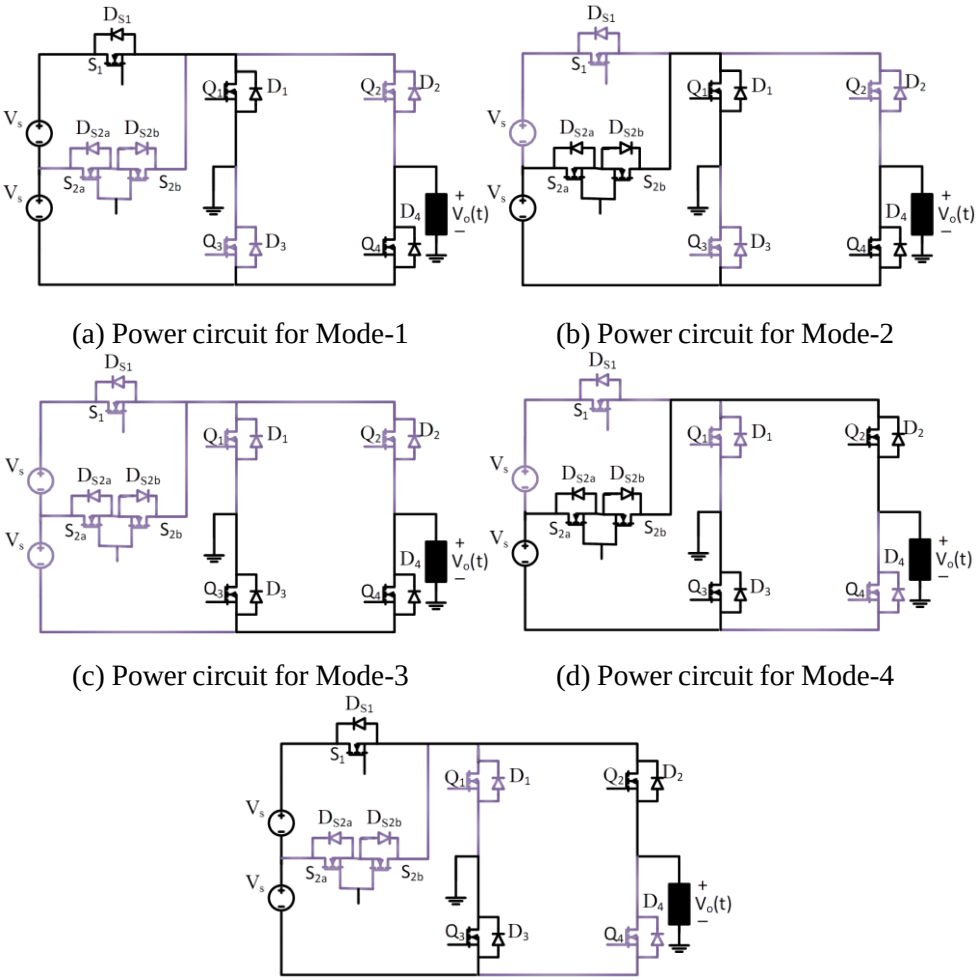

(a) Power circuit for Mode-1

(b) Power circuit for Mode-2

(c) Power circuit for Mode-3

(d) Power circuit for Mode-4

(e) Power circuit for Mode-5

Figure 2 Power stages for new reduced switch five level topology

The switching pattern for generation of control signals for reduced switch five level inverter is shown in Table 1

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Table 1: Generation of control signals for Reduced switch five level inverter

Modes	Switching pattern for inverter						
	V_o	Q_1	Q_2	Q_3	Q_4	S_1	S_2
Mode - 1	$2V_s$	1	0	0	1	1	0
Mode - 2	V_s	1	0	0	1	0	1
Mode - 3	0	0	0	1	1	0	0
Mode - 4	$-V_s$	0	1	1	0	0	1
Mode - 5	$-2V_s$	0	1	1	0	1	0

III POWER STAGE OPERATION (R - LOAD)

The different modes of operation of reduced switch five level inverter with resistive load is as follows.
Mode - 1: Switches Q1, Q4 and S1 acts to get maximum positive output voltage level of 2Vs.
Mode - 2: Switches Q1, Q4, S2a and DS2b acts to get half level positive output voltage level of Vs.
Mode - 3: Switches Q3 and Q4 acts to get zero output voltage level.
Mode - 4: Switches Q2, Q3, S2a and DS2b acts to get half level negative output voltage level of −Vs.
Mode - 5: Switches Q2, Q3 and S1 acts to get maximum negative output voltage level of −2Vs.

IV MULTICARRIER SCHEME

Reduced switch MLI topology uses the possibility of multicarrier scheme for generation of control signals (MAHATO *et al.*, 2018). Constant frequency carrier PWM with phase disposition (PD PWM) has been utilized for generation of carrier signals of reduced switch topology with a slight modification which is explained in this section. Sine wave of fundamental frequency can be considered as modulating signal and high frequency triangular waves are taken as carrier signals. The switching pattern for the reduced switch inverter is obtained with proper utilization of logical gates.

The main advantage of PWM inverters in power electronics is the reduction of harmonics and passive component sizes by operating at increasingly high frequencies. However, the switching losses increase as the switching frequency increases and the losses become significant at higher frequencies. Though low frequency switching can be implemented by using modulation strategies like selective harmonic elimination and space vector control, carrier based PWM methods are preferred due to the complication offered by the fundamental switching frequency methods (McGrath and Holmes, 2002). The multicarrier phase disposition technique has a superior line to line harmonic performance over other methods (Kant *et al.*, 2015). High frequency rating of the higher voltage rated switches reduces the efficiency of carrier based PWM inverters. The reduced switch topology overcomes this disadvantage by switching the higher voltage rated switches at fundamental frequency.

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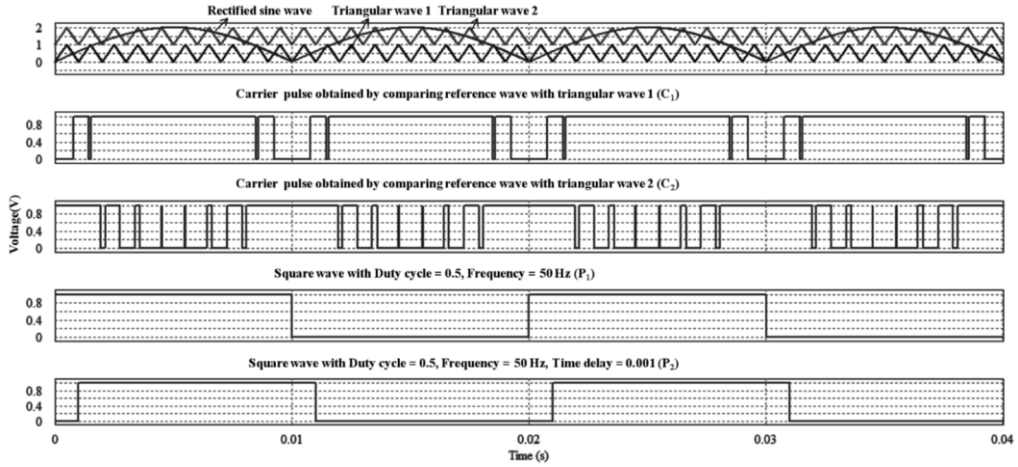
The theoretical waveforms for representation of carrier pulses for the generation of control signals is shown in Figure 4. The logical equations for implementation of control circuit are summarized using Equations 1 - 4. C_1 and C_2 represents the control pulses generated by comparing sine wave with triangular carriers and P_1 is a square pulse having duty cycle of 0.5 and frequency 50 Hz. P_2 is the delayed pulse of P_1 shifted by 0.001 s from the orgin.



$$Q = Q = (P_1(C_1 + P_2)) + (\overline{P_1}(C_1 + \overline{P_2})) \quad (1)$$

$$Q_2 = Q_3 = (P_1(C_1 + P_2)) + (P_1(C_1 + (P_2)) \quad (2)$$

$$S_1 = C_2 \quad (3)$$

$$S_2 = C_1C_2 \quad (4)$$

Modulation index (M_a) is defined as ratio of amplitude of modulating signal to carrier signals in PWM schemes. In multicarrier schemes, a greater number of triangular carriers are used to generate control pulses. Here two triangular carriers are required to generate a five-level output. So, a factor of (k-1) is multiplied to amplitude of each of carrier signals to obtain modulation index and is expressed by Equation 5.

$$M_a = \frac{A_m}{(A_c(k-1))} \quad (5)$$

Here k is the number of voltage levels per half cycle, A_c is the peak-to-peak value of carrier wave and A_m is the peak value of modulating signal. Modulation index (M_a) for reduced switch five level inverter is given by Equation 6.

$$M_a = \frac{A_m}{2A_c} \quad (6)$$

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V CONTROL CIRCUIT

The control circuit of reduced switch five level inverter is represented in Figure 5 as per boolean equations 1 - 4. An increase in the number of pulses for output waveform of inverters produces a clean spectrum devoid of harmonics. The harmonic distortions can be reduced to a great extent by introducing low pass filter circuits following the output because the amplitude of high frequency signals will be less and can be easily filtered out. As the modulation index decreases beyond 0.5, the output voltage waveform approximates to two level inverter output voltage. Multicarrier modulation technique utilizes high frequency carrier signals either by phase disposition or phase shifting method. The reduced switch topology utilizes constant frequency phase disposition method of multicarrier modulation. PD PWM has been established to be an optimal solution for pulse width modulated inverters.

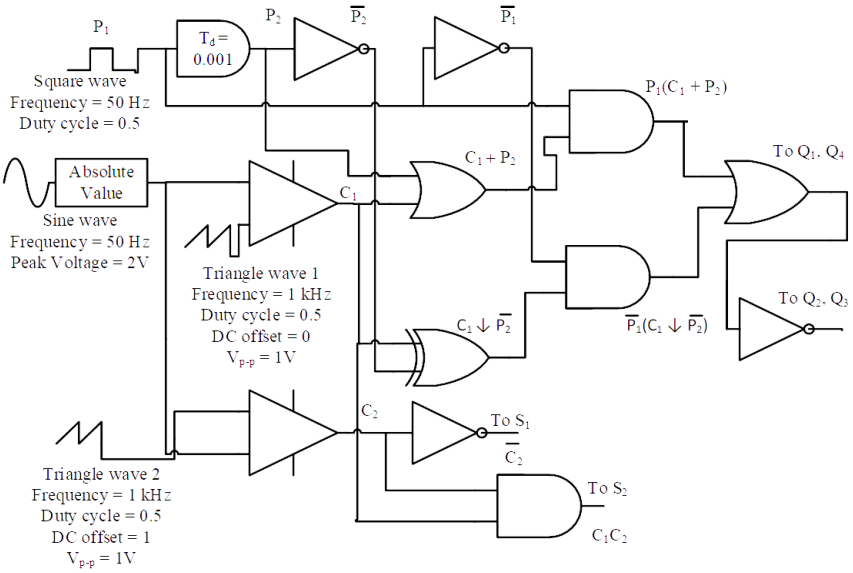

Figure 5: Control circuit for reduced switch five level inverter

VI .SIMULATION STUDIES

Simulation results of reduced switch five level inverter have been obtained using PSIM Professional Version 9.0.3.400. Simulation results are helpful in analyzing THD of the inverter before visualizing harmonic effects in harmonic analyzer. High frequency triangular carriers of frequency 1 kHz with full wave rectified sine wave of frequency 50 Hz, two DC voltage sources which constitute a dual voltage supply of 30 V each and total voltage of 60 V have been selected. Simulated results for multicarrier modulating signals and switching pattern of the reduced switch five level inverter are shown in Figure 6 and Figure 7 respectively. It can be seen from Figure 7 that MOSFET switches S_1 (14 pulses per half cycle) and S_2 (20 pulses per half cycle) are high frequency switches with switching frequencies of 700 Hz and 1000 Hz respectively. But H-Bridge switches Q_1−Q_4 (1 pulse per half cycle) will be having a switching frequency of 50 Hz. Simulation results for reverse blocking voltage waveforms across MOSFET switches are shown in Figure 5.8.

Output voltage waveform, current waveform and FFT Spectrum of new inverter for different modulation indexes (M_a) (M_a=1, M_a=0.8, M_a=0.6 and M_a=0.4) are shown in Figure 9 - 12. It is seen that as the modulation index decreases, the THD of inverter increases.

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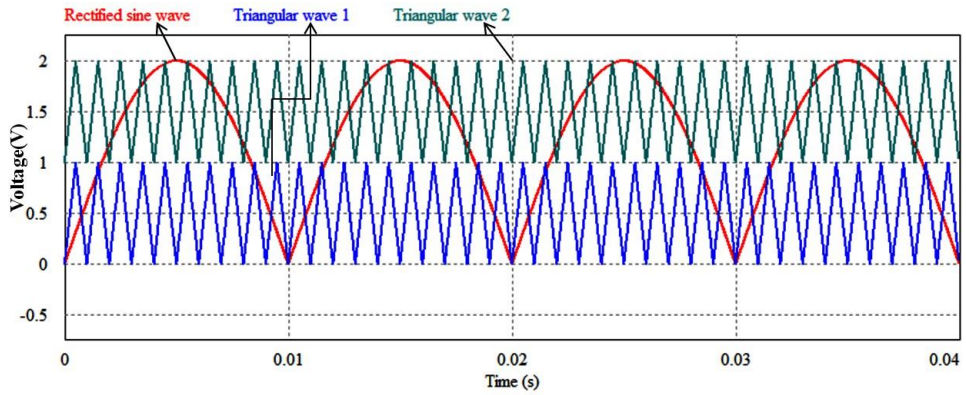

Figure 6: Multicarrier modulating signals

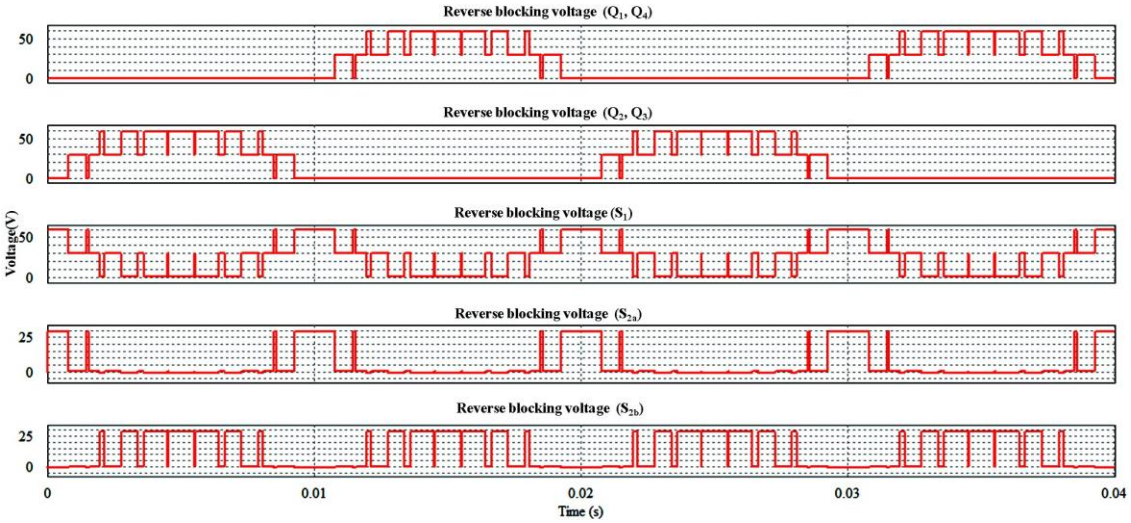

Figure 7: Switching pattern for reduced switch five level inverter (M_a=1)

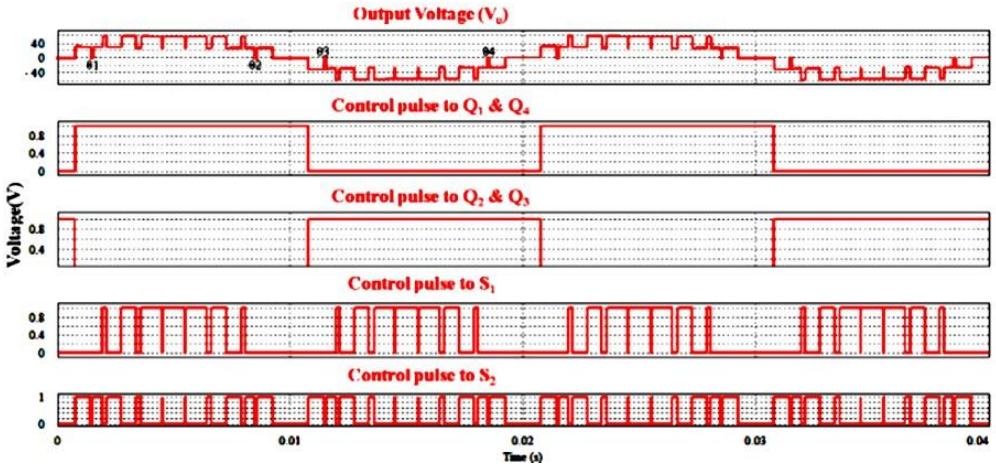

Figure 8: Reverse blocking voltage waveform across switches (M_a=1)

Results from simulation agrees with output pattern of a conventional five level inverter. Five distinct levels of voltages have been obtained in both cases. The analytical calculation of THD (V) for various modulation indexes has also been verified along with simulation results. It has been concluded that for small values of modulation index, PWM waveform degenerates into a

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nearly squared waveform. The harmonic spectrum has been distorted for smaller values of modulation index less than unity. With proper selection of modulation index above 0.5, total harmonic distortion of the waveform can be made smaller.

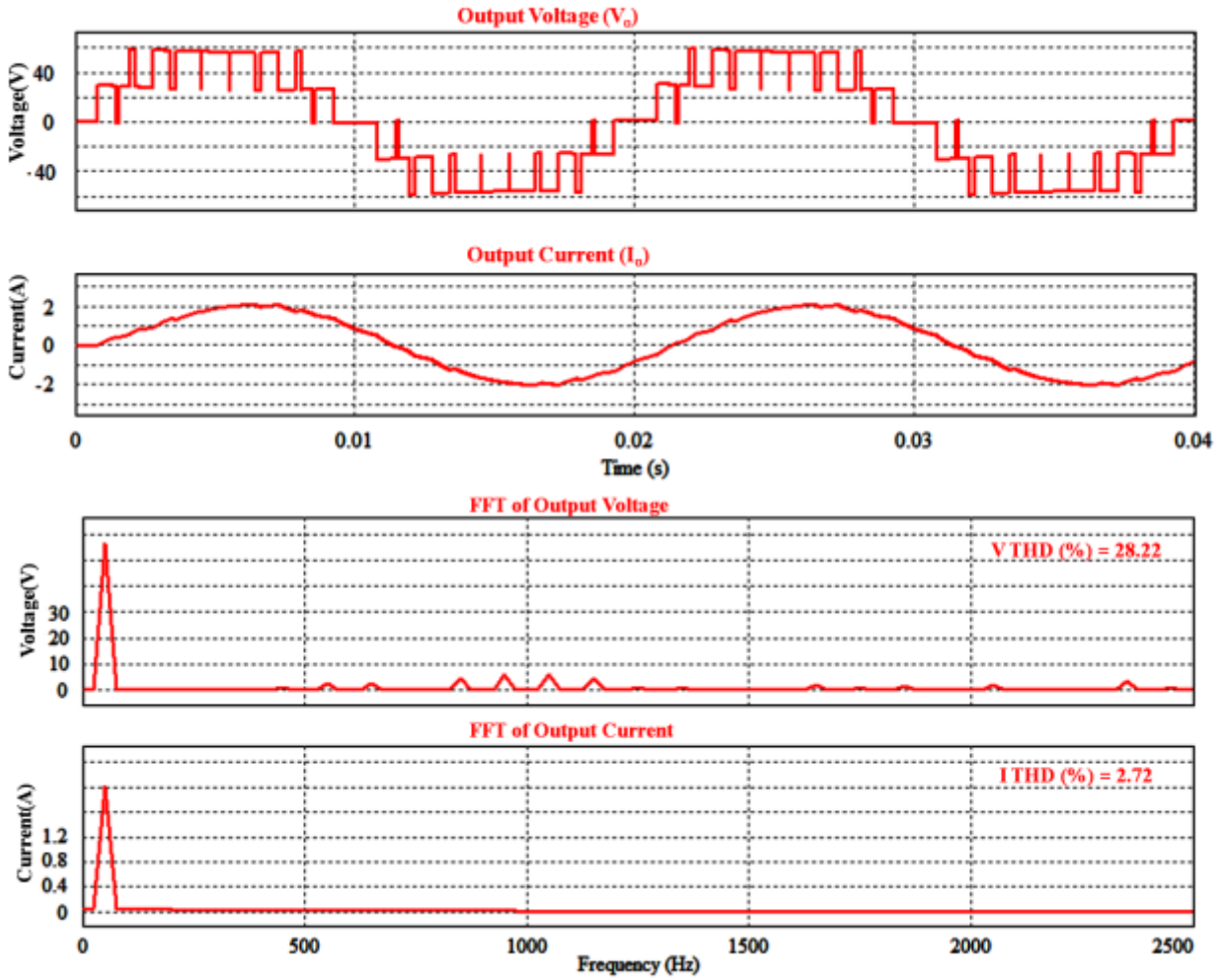

Figure 9: Output voltage waveform, current waveform and FFT spectrum for reduced switch five level inverter (Ma=1)

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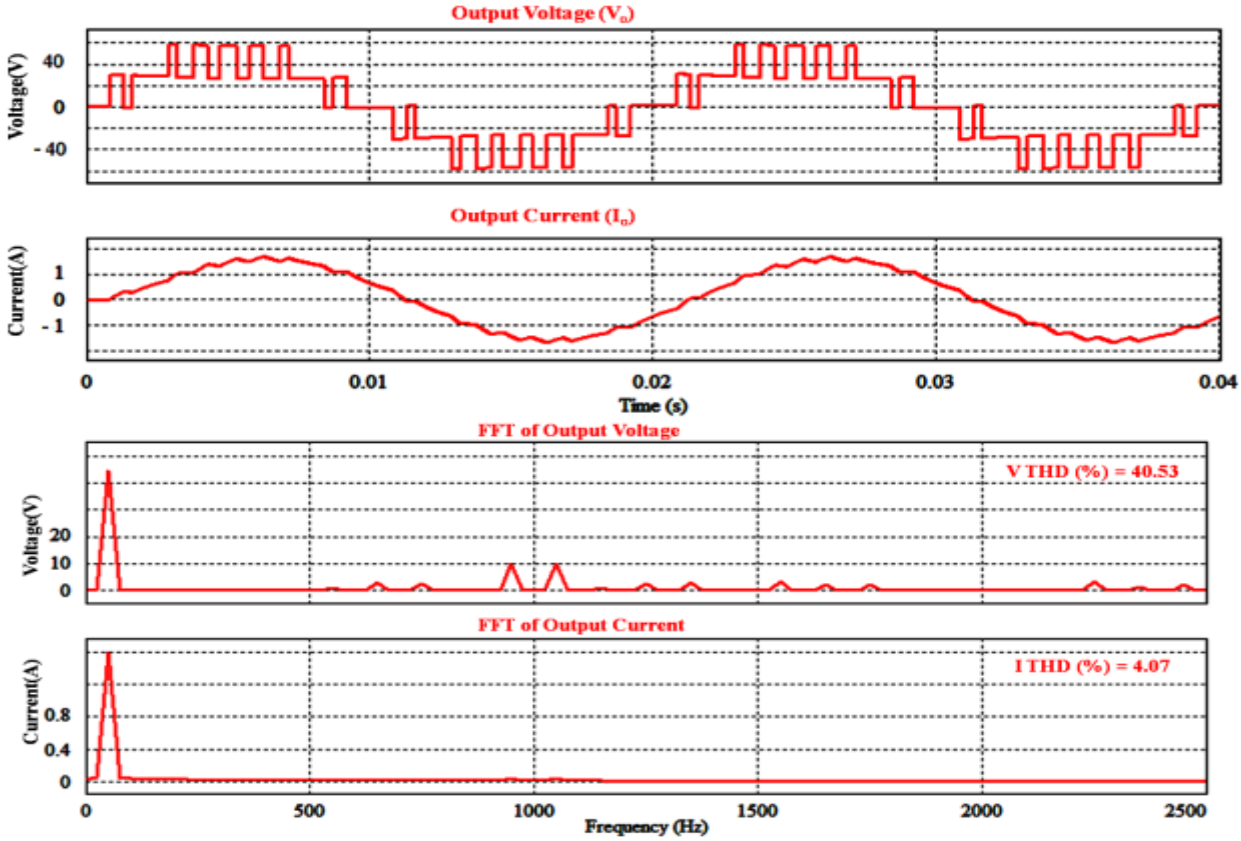

Figure 10: Output voltage waveform, current waveform and FFT spectrum for reduced switch five level inverter (Ma=0.8)

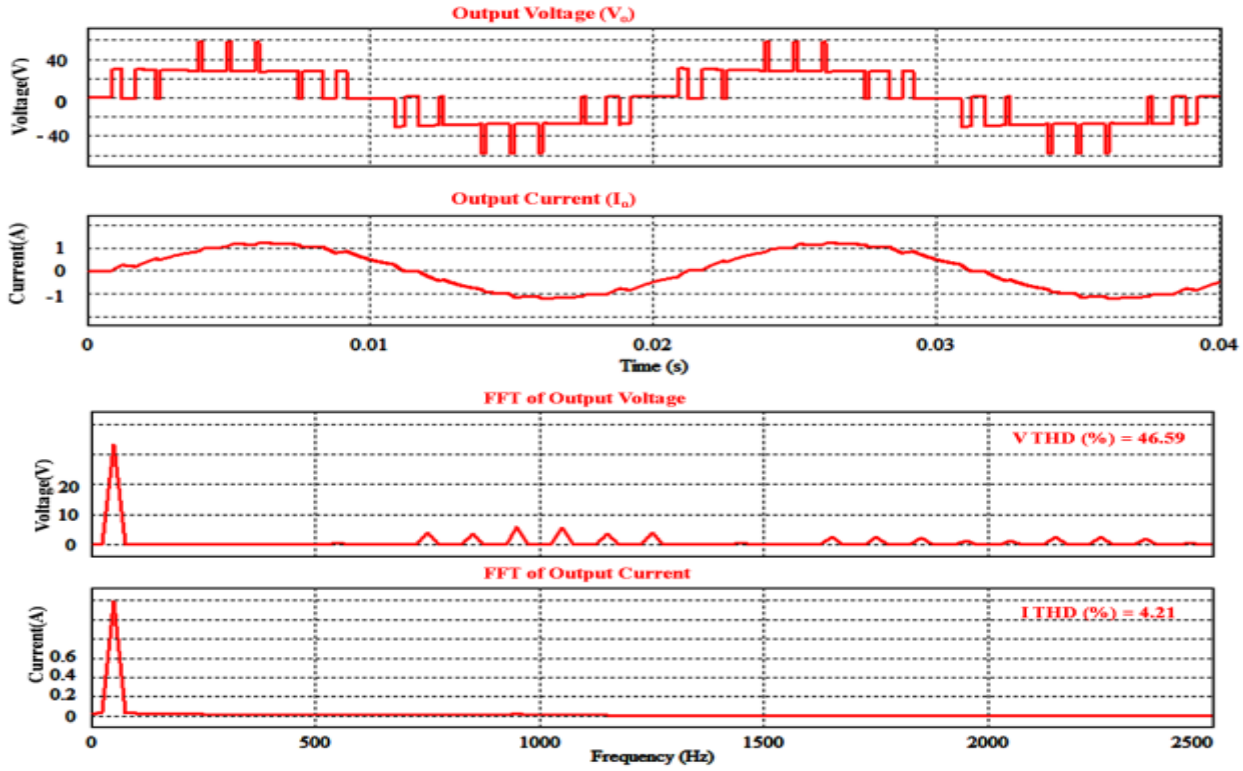

Figure 11: Output voltage waveform, current waveform and FFT spectrum for reduced switch five level inverter (Ma=0.6)

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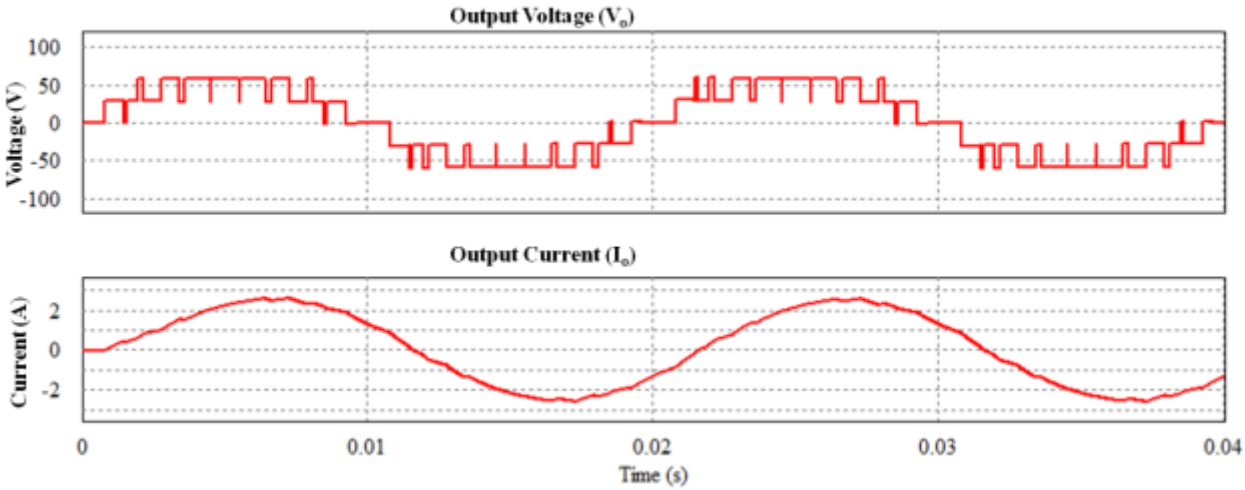

Figure 12: Output voltage and current waveforms (Ro = 25Ω)

VII CONCLUSION

Results from simulation agrees with output pattern of a conventional five level inverter. Five distinct levels of voltages have been obtained. FFT spectrums for different modulation indexes have been visualized experimentally. The analytical calculation of THD (V) for various modulation indexes has also been verified along with simulation results. It has been concluded that for small values of modulation index, PWM waveform degenerates into a nearly squared waveform. The harmonic spectrum has been distorted for smaller values of modulation index less than unity. With proper selection of modulation index above 0.5, total harmonic distortion of the waveform can be made smaller- The reduced switch inverter can be utilized in electric vehicle drives and renewable energy systems. Renewable energy systems play a key role in utilization of electric power. These renewable sources can be easily interfaced to multilevel inverters where reduced switch five level inverter can be utilized. It can also be used in power factor compensators and active filters. As the main switches are operating at fundamental frequency, the switching losses of the inverter will be low.

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