# A Comparative Analysis Of Power Efficient Flip-Flops

Priyanka Sharma[1] Ganesh Lakshmana Kumar Moganti[2] Kavita Khare[3]

[1]Deptt. Of Electronics & Communication Engg., M.A.N.I.T., Bhopal, India.

[2]Deptt. Of Electronics & Communication Engg., M.A.N.I.T., Bhopal, India.

[3]Deptt. Of Electronics & Communication Engg., M.A.N.I.T., Bhopal, India.

## *Abstract*

*A power efficient flip flop dissipates very less power as compared to normal flip flops. In this paper different power efficient flip-flops with different specific features are compared. A specified category of power efficient flip-flops known as the Dual Edge Triggered flip-flops are also considered in this comparison. The Dual Edge Triggered flip-flops responses to both positive and negative edge of clock. Hence this flip-flop can significantly reduce the clock related power. In this article, we compare several published implementations of power efficient flip-flops for performance & power consumption.*

## *Keywords*

*Dual Edge Triggering, Conditional Capture Technique, Conditional Precharge, Power Delay Product, Clock Distribution Network.*

## 1. INTRODUCTION

Low power is becoming a critical issue with the increasing integration complexity of modern VLSI. Active and Passive power dissipation has become the leading limiting factor for Mos performance, device reliability and further integration. On the other hand high clock frequencies are the major cause of increased power consumption in case of high performance processors. Clock distribution network of Digital VLSI design , which forms the clock system , alone consumes 30% to 60% of the system power. In the recent trend in which we are going for deep pipelining and frequency scaling , the problem of clock system power dissipation is more severe. Now when we are using portable digital circuit which has limited power budget it is important to reduce the power dissipation of flip flop as well as clock distribution network , to enable us to extend the battery life of battery operated systems. Along with reducing clock system power Dual edge triggering mechanism also reduces the flip-flop latency.

## 2. REVIEW AND MOTIVATION

While going for power reduction, active and dynamic power dissipation which is the major element of power consumption , should be of main concern. The static power component is relatively small but the dynamic power dissipation increases with level of integration and complexity of the system. The clock power dissipation in synchronous VLSI circuits
is divided into three major components **[1]:**

(i) power dissipation in clock net, (ii) power dissipation in clock buffers and (iii) power dissipation in flip-flops. The total power dissipation of the clock network can be computed as follows:

$$\mathbf{P_{CLK} = V_{DD}^2( f_{clk}( C_{clk} + C_{ff,clk})+ f_{data}.C_{ff,data})}$$

where $V_{DD}$ is the supply voltage, $f_{Clk}$ the clock frequency, $f_{data}$ the average data frequency, $C_{clk}$ the total capacitance related to the clock signal excluding flip-flops, $C_{ffClk}$ the total capacitance related to the clock signal connected to the flip-flops, and $C_{ffdata}$ the total capacitance of the flip-flops connected to the data input.

One of the earliest power efficient DET flip-flop is proposed by Unger in 1981 [7]. He suggested DET flip-flop usage would result into reduced power consumption power in digital circuits. A number of power efficient flip-flop implementations were proposed earlier. In spite of several recent DET flip-flops and their potentials in power reduction, DET flip-flops are not widely used. DET flip-flops have larger number of transistors compared to a conventional flip-flop. As a consequence, DET flip-flops have larger propagation delay. DET flip-flops also have larger input capacitance that makes their setup and hold times larger compared to the conventional flip-flop.

This article is organized as follows. In following section we study some of the published power efficient and DET flip-flop configurations. In the next Sections , simulation results are presented. Finally in last Section, conclusions are drawn.

## 3. IMPLEMENTATION OF POWER EFFICIENT FLIP-FLOPS

In the first power efficient flip-flop PEFF(1) master-slave latch configuration is taken, which consists of two cascaded latch.In this flip flop master latch is replaced by the pulse generator stage, which is generally the first stage of flip-flop and is a function of the clock and data signals.

The PEFF(1) consists of the SA in the first stage and the slave set-reset (SR) latch in the second stage as shown in Fig. 1, [2]. Thus PEFF(1) is a flip-flop where the SA stage provides a negative pulse on one of the inputs to the slave latch: $\hat{R}$ and $\hat{S}$ or (but not both), depending whether the output Q is to be set or reset. The pulse-generating stage of this flip-flop is the SA described in [3], [4]. It senses the true and complementary differential inputs. The SA stage produces monotonic transitions from one to zero logic level on one of the outputs, following the leading clock edge. Any subsequent change of the data during the active clock interval will not affect the output of the SA. The SR latch captures the transition and holds the state until the next leading edge of the clock arrives. After the clock returns to inactive state, both outputs of the SA stage assume logic one value. Therefore, the whole structure acts as a flip flop.

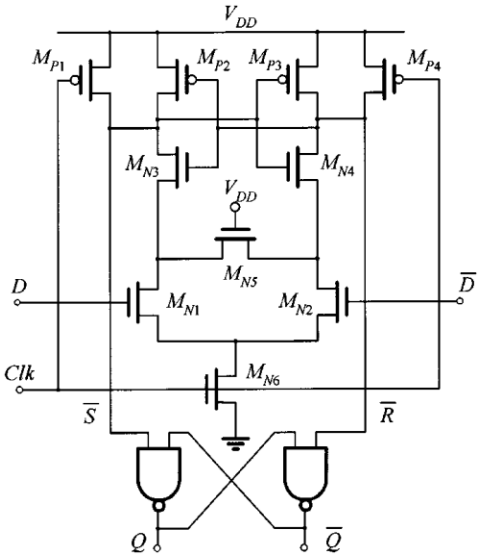


Fig. 1 An Implementation of PEFF(1) proposed in [2]

In the next PEFF i.e. PEFF(2), reduction in statistical power is obtained. The schematic diagram of the proposed flip-flop, the conditional-capture flip-flop (CCFF), is shown in Fig. 2. As per [5] the PEFF(2) consists of two stages, the differential circuit with a pair of NOR gates and clock inverters I1 and I2 in the first stage, and the high-speed SR latch with the cross-coupled circuit in the second stage. The NOR gates are driven by the outputs to make the discharge of precharge nodes SB and RB , depend on the equivalence of input and output data. They are also driven by the delayed version of the clock, CKD, to determine the transparency period. The outputs, N and NB, of the NOR gates drive the transistors, M4 and M3, of the pull-down paths, respectively. Two weak inverters, I3 and I4, are used to maximize the noise immunity of precharge nodes by making them fully static. Two pairs of outputs, S/SB and R/RB, from the first stage are fed into the second stage, where the SR latch is stationed. The latch captures each transition and holds the outputs until the next pull-down transition occurs on one of the precharge nodes. The cross-coupled circuit consisting of four weak transistors M12 through M15 is used for compensating the leakage and preserving the output data statically during the period in which the SR latch is opaque.

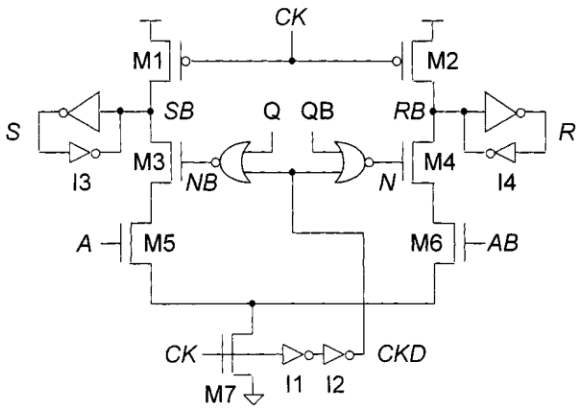


Fig. 2 An implementation of PEFF(2) proposed in [5]

The third flip-flop PEFF(3) is the modification of previous one in the terms of low switching activity. This is based on the conditional precharge and conditional capture technique[6] which is very efficient to reduce clock system power. This technique is based on the clock gating idea. Flip-flops employ clock gating feature a transparent window period that is used to sample the input. In Fig. 3 the PEFF(3) is introduced to reduce redundant power at the internal node. This flip-flop employs a scheme much like the JK-type-flip-flop, but it adds one more gate that is switching with the clock. This addition leads to an increase in the power consumed by the clock system, and it may offset the savings gained from reducing the internal redundant switching power. Moreover, employing the double-edge triggered technique will be complicated and the transistor count would increase because it requires the duplication of the NOR gate and other clocked transistors. A revised condition captured flip-flop (imCCFF), Fig. 4, is proposed to improve the energy-delay-product (EDP). A further enhancement on this flip-flop could be employed to reduce the switching activity on the internal node , which may further improve the EDP.

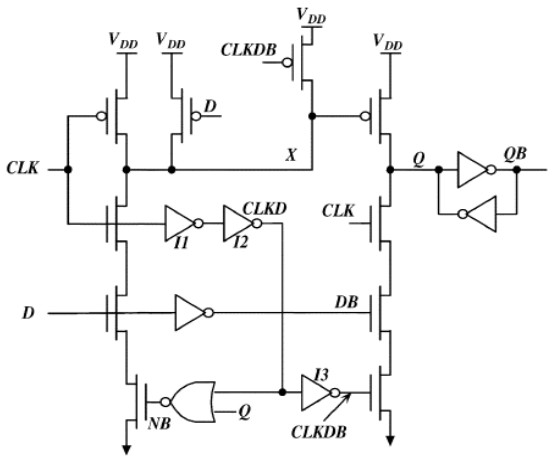


Fig. 3 An implementation of PEFF(3) proposed in [6]

In the next modified flip-flop PEFF[4], dual edge triggering is also employed along with conditional precharge technique[13]. In the dual edge triggering flip-flop triggers at both positive and negative transition of the clock pulses. In PEFF(4) redundant internal node transitions are reduced.There are three major parts of this flip flop [8] 1) the inverter chain to generate delayed clock signals 2)the front end core to sample data that is based upon sense amplifier flip-flop 3) the SR latch consisted of the two cross-coupled NAND gates. In order to achieve dual edge-triggering, we use an inverter chain to produce delayed clock signals. CLK and CLK3 both are high for a short period of time on the CLK rising edge and so are CLK1 and CLK4 on the CLK falling edge.

For the front-end core, we add two cascoding transistors M5 and M8, to implement conditional capturing .If the D input is the same as the Q output, nodes SB and RB stay high and NAND cross-coupled SR latch retains its previous outputs. If the D input is different from the Q output, the outputs of the front end are fed into a SR latch consisting two cross-coupled NAND gates. They convert the falling pulsed SB or RB signals to static Q outputs.

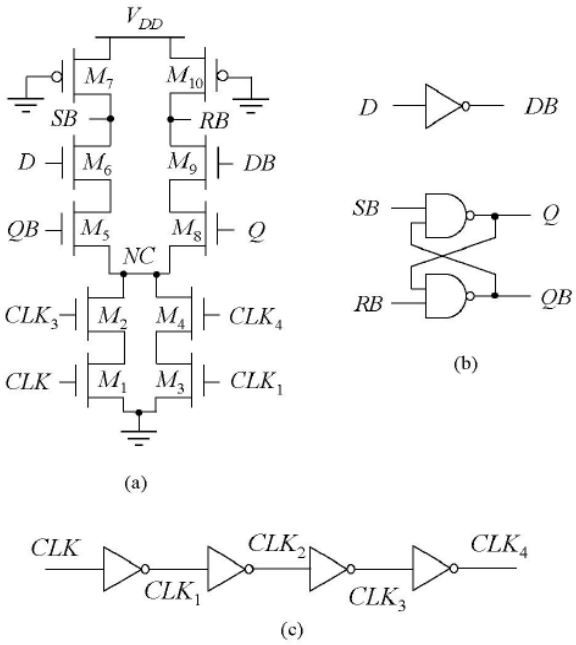


Fig.4 An implementation of PEFF(4) proposed in [8]

## 4. PERFORMANCE PARAMETERS

For this analysis, single poly, 0.18 micron CMOS technology is used. Transistor sizes are selected to be compatible of the technology. For this comparative study, transistors sizes in all flip-flops were kept of the comparable dimensions. All PEFF configurations are circuit simulated with Virtuso in Cadence design environment. Data and clock rise/fall times of 1ns are used. In addition, the PEFFs are simulated at room temperature, 1.2V input supply voltage and no load conditions

**Table.I**.Comparing the PEFF intearms of power analysis

| S.No | Name | # of Tr | DQ(ps) | P(uW) | PDP(fj) |
|---|---|---|---|---|---|
| 1 | $PEFF_1$ | 24 | 545 | 21.8 | 11.88 |
| 2 | $PEFF_2$ | 28 | 185 | 20.2 | 3.74 |
| 3 | $PEFF_3$ | 33 | 226 | 21.6 | 4.88 |
| 4 | $PEFF_4$ | 24 | 447 | 20.8 | 9.06 |

# of Tr –No. of Transistor ,DQ-Delay , P-Power, DDP-power delay product

The performance of a flip-flop is characterized by its setup and hold times, propagation delay, and power dissipation. The performance parameters of PEFF are compiled in Table 1 and Table 2. As shown in the table, PEFF2 depicts the smallest power dissipation while PEFF1 has the largest power dissipation. Flip-flops often show negative setteling time. PEFF4 has the most negative setteling time. PEFF2 has the smallest propagation delay. PEFFl on the other hand has the largest propagation delay followed by PEFF4.

**Table.II**. Numerical results at 50% data switching activity

| S.No | Name | $T_S$ (ps) | $T_H$(ps) | Total Width (µm) |
|---|---|---|---|---|
| 1 | $PEFF_1$ | -18.8 | 56.0 | 46.2 |
| 2 | $PEFF_2$ | -26.5 | 88.0 | 56.3 |
| 3 | $PEFF_3$ | -21.3 | 62.0 | 47.2 |
| 4 | $PEFF_4$ | -165.3 | 327.0 | 40.3 |

Ts-setting time, $T_H$ –Hold time

# 5. VARIATIONS WITH ENVIRONMENTAL PARAMETERS

Environmental parameters such as Temperature (T), supply voltage (Vdd) and clock and data rise and fall time (Tr and Tf) plays a major role in determining the robustness of the flip-flop.In this section sensitivity of flip flop is measured in terms of variation of propagation delay with this parameters.

## 5.1. Clock and Data Rise and Fall Times

Figure 5 illustrates the propagation delay (tpd) of PEFF as a function of clock and data rise and fall times. In the ideal case (i.e. zero rise and fall times), PEFFl and PEFF2 have substantially higher propagation delays compared to the other PEFFs. On the other hand, PEFF3 flip-flop exhibits the smallest propagation delay amongst all. As the rise and fall time increase, propagation delays of flip-flops also increases monotonically as is cleared from Fig.5.

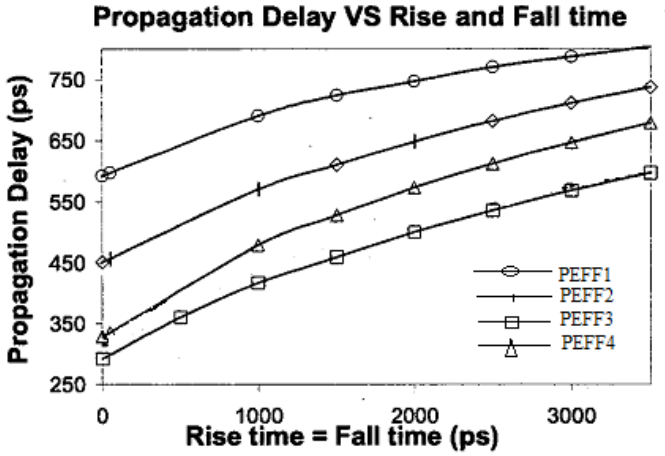


Figure 5: Propagation delay as a function of clock and data rise and fall times.

## 5.2. Supply Voltage

In the battery powered applications insensitivity towards supply voltage are desirable. As is clear from Fig. 6 Transistor delay increases as supply voltage is reduced. Therefore, logic delay is also increased as supply voltage is reduced . As can concluded from Figure 6, PEFFl and PEFF2 have the highest propagation delay. The other PEFF have relatively smaller propagation delays. PEFF3 has the smallest propagation delay.

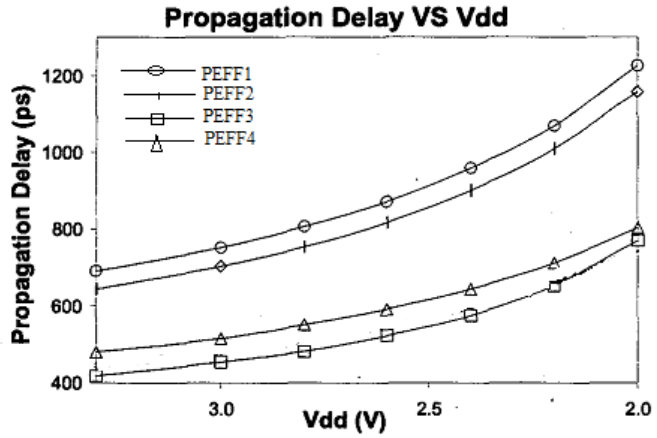


Figure 6: Propagation delay as a function of supply voltage Vdd.

### 5.3. Temperature

Propagation delay increases monotonically as temperature is increased. This is becaue of mobility degradation at higher temperature. All PEFF exhibit higher propagation delay with increasing temperature (Figure 7).

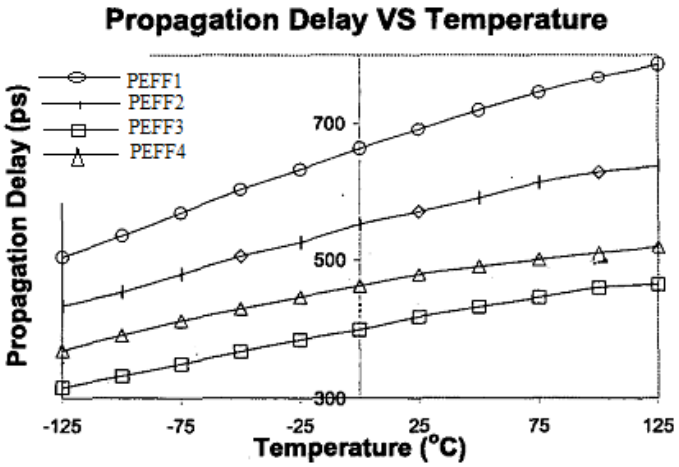


Figure 7: Propagation delay as a Function of temperature

## 6. CONCLUSION

In this paper we have done the comparison of different Power efficient flip-flops in terms of their performance and robustness. As per the analysis done in this paper PEFF3 is found to have the best performance among the PEFF in the discussion. This is the preliminary analysis and it can be extend further for different parameters. These Power efficient Flip-flops are very useful to incorporate into larger VLSI designs for power saving and robustness.

# 7. REFERENCES

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**Authors**

Priyanka Sharma, at present, is pursuing M.Tech in VLSI & Embedded System from MANIT,Bhopal,INDIA.She has completed her Graduation in Electronics & Communication Engineering from Guru Ghasidas University, INDIA in 2009.

Ganesh Lakshmana kumar.Moganti, at present, is pursuing M.Tech in VLSI & Embedded System from MANIT,Bhopal,INDIA.He has completed his Graduation in Electronics & Communication Engineering from Gudlavalleru Engineering College,JNTUK,INDIA in 2010. Since he has a keen interest in VLSI Design & Embedded Coding, he has successfully completed many projects on it.