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A Comprehensive Analysis of Design and Simulation of Power Optimized CRC Algorithm for ZIGBEE Application

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***Abstract*— In this paper, a power optimized ZigBee transmitter with efficient 16 bit CRC has been proposed. The standardized protocol is suitable for low power communications. This protocol is mostly suitable for Wireless Personal Area Networks (WPAN) applications. The rapid growth which has been experienced by the Sector pertaining to wireless communication is conspicuous in the recent years. There are many wireless monitoring and control applications for industrial and home markets which require lower date rates, longer battery life and less complexity than available from existing wireless standards. The ZigBee Protocol is adopted for wireless communication for achieving Portability, Applicability and High Integration. The Low-Power ZigBee-SOC is being simulated by the Xilinx ISE and targeted for FPGA SPARTAN 3E device.The evaluation of simulation mainly confirms in fixing the errors. The Error Detection techniques which are most commonly used are redundancy checking, checksum, longitudinal redundancy checking, and cyclic redundancy checking which are done during the proposed research work. Using the CRC the proposed work attempts to detect 99.99% errors during transmission. The block check sequence uses the 16 bit width in CRC-16 to generate the continuous binary number with the data stream. From the results it is observed that the power reduction achieved for the proposed system is around 10 % less when compared to conventional system.**

Keywords*— *ZigBee, CRC, LUTs, occupied slices, Xilinx, Verilog,MAC, PHY.

I. INTRODUCTION

The power of wireless communication is rapidly progressing towards a newer direction in establishing personal wireless networks built on low power systems. Evolutionary communication technologies like WIFI, Bluetooth, and ZigBee predominantly play a major role in the life of a common man. Of the late, ZigBee is slowly getting its popularity in establishing personal wireless networks which is built on small and low-power digital radios. Conceptually ZigBee can be viewed as a specification for a suite of advanced communication protocols which are primarily used to establish personal area networks. The technology is developed based on an IEEE 802.15.4 standard. Despite of its low power consumption bounds transmission distances to 10–100 meters line-of-sight, still ZigBee devices based on input power and surrounding environment, can transmit data over long distances by passing data through the help of a mesh network which is comprised of intermediate devices to reach more distant ones. Applications of ZigBee include wireless electrical switches, domestic electric meters, traffic management systems, consumer and industrial equipment which require short-range low-rate wireless transfer of data. The technology which was defined by the ZigBee specification is aimed to be simpler and economically cheaper than other contemporary wireless personal area networks (WPANs), such as Bluetooth or Wi-Fi. The technology has been developed during late 1990's and got standardized in the year 2003. Several revisions in the suite of ZigBee protocols are still going on done to establish effective and efficient personal wireless networks.

ZigBee can be used as a wireless networking standard that is primarily aimed at remote control and a sensor based applications which are suitable for operation in sever radio environment. ZigBee was built on IEEE standard 802.15.4 which defines PHY and MAC layers. The specification also defines the application and Security Layer specifications for interoperability between products from various type of manufacturers. Such enhancement makes ZigBee as a superset of the 802.15.4 specification. NetSim, NS2, and OPNET are some network simulators which can be used to simulate IEEE 802.15.4 ZigBee networks. These simulators are developed using open source C or C++ libraries and released for the end users to modify. So that, the users can determines the validity of new algorithms prior to hardware implementation.

II. OBJECTIVE OF THE WORK

Numerous procedures, methods and tools available with the theory of electronics concepts that drive in developing resulted hardware components. Real-time operational evaluation to assess the nature of hardware component, process or method in an embedded circuit sometimes could not deliver the expectations because of their criticalness. After a thorough survey of literature, it is found that several researchers have designed the ZigBee transmitter using a Mat lab/Simulink, a Schematic and also using VHDL targeted for Spartan and a Virtex FPGA family. Transmitter designed using Verilog uses lesser number of slices, LUTs, etc. The problem is to evaluate by simulation of the underlying nature of ZigBee transmitter with respect to its MAC and PHY layer using the widely accepted and advanced hardware description language Verilog.

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Thus, the proposed research work is aimed in designing of ZigBee transmitter for PHY & MAC layer of IEEE 802.15.4 standard, with the help of Verilog and to be analyzed with the Simulated results which will be obtained throutg Xilinx in order to reduce cost and complexity. The proposed design operation performance should satisfy the specifications mentioned in theory and must be verified with the simulation results. To accomplish the objectives, compatible algorithms or procedures have to be developed using Verilog HDL. During the process, both the physical and MAC layers are studied and configured accordingly to the power constraints and surrounding environment. The evaluation of simulation mainly confirms in fixing the errors. The error detection techniques which are most commonly used are redundancy checking, checksum, longitudinal redundancy checking, and cyclic redundancy checking which are done during the proposed research work. Using the CRC the proposed work attempts to detect 99.99% errors during transmission. The block check sequence uses the 16 bit width in CRC-16 to generate the continuous binary number with the data stream. The proposed transmitter is assumed to be working at the ISM frequency 2.4GHz and the modulation technique adopted is Offset Quadrature- Phase Shift-Keying (OQPSK) with half sine pulse shaping. The proposed system is designed with a data rate of 250 Kbps over a 16 channel medium operating on a 2.4GHz. The channel spacing is fixed with 5MHz working with direct sequence spread spectrum at a chip rate of 2 Mega chips per second.

III. ZIGBEE TRANSMITTER

A. Specifications

ZigBee [13] is a high-level communication specification suite based on an IEEE 802.15.4 standard intended to establish personal area networks using low-power digital radios. Normally ZigBee devices have the transmission capacity of 10 – 100 meters due to its low power consumption. However, these devices could also transmit data to long distances with the help of intermediate boosting devices. ZigBee networks are potentially secured by 128-bit symmetric encryption keys and are widely used in low data rate applications. Applications of ZigBeeinclude, domestic electric meters, wireless light switches, traffic management systems, and industrial data exchange systems etc. ZigBee chips are integrated with microcontrollers and radios that work in the range of 60 – 256 KB flash memory. ZigBee is the simpler and cheaper than other wireless personal area networks like WIFI and Bluetooth. The concept ZigBee was designed in the year 1998, standardized in 2003, and enhanced for revision in the year 2006. The name has been coined representing the waggle dance of honey bees after their return to the beehive.

ZigBee chips are typically integrated with radios and with microcontrollers that work in the frequency range 60-256 KB flash memory. Table 1.5 lists the worldwide operational frequency range of ZigBee. The minimum data range is 20 kbit/s (868 MHz band) and can work up to 250 kbit/s (2.4 GHz band). The network supports star, tree and mesh topology. A network coordinator device is to be dedicated to the network for controlling and maintenance.

The PHY and MAC layers of ZigBee are defined in IEEE standard 802.15.4 for low-rate WPANs. Four (4) additional key components via application layer, network layer, a *ZigBee device objects* (ZDOs) and also manufacturer defined application objects for user specific customization are included in the ZigBee network. The specifications are listed in table 2.

Table 1: Worldwide operating frequency range of ZigBee

Geography	Standard Regulatory frequency Range
China	784 MHz
Europe	868 MHz
USA and Australia	915 MHz
Other Nations	2.4 GHz

Table 2: Specifications

PARAMETER	SPECIFICATION
Data rate	250 Kbps
No. of channels	16
Operating frequency	2.4 GHz
Channel spacing	5 MHz
Spread spectrum	Direct Sequence Spread
Chip rate	2 Mega chips per second
Modulation	OQPSK with Half sine Pulse
Spectrum	shaping

The frame structure of 802.15.4 MAC is depicted in the figure 1. The MAC frame composed of MAC header (MHR), MAC payload or service data unit (MSDU) and MAC footer or FCS. The basic MAC frame has frame control field of 2 octets. This indicates the type of frame, source and destination addresses.

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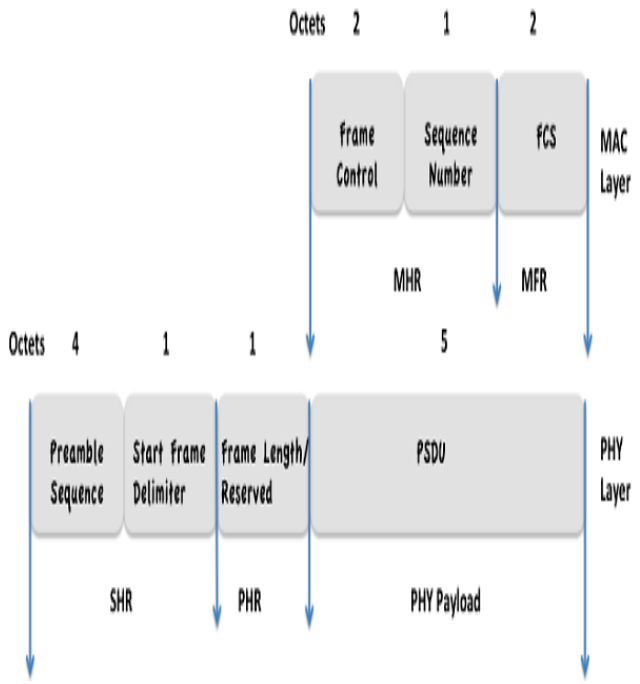
Figure 1: MAC basic frame structure



The IEEE 802.15.4 defines four MAC frame structures: beacon, data, acknowledgement and MAC command frames. The beacon frame is transmitted by a coordinator. The beacons are usedfor synchronizing all the device clocks within the network itself. The data frame will be used for transmitting data. Meanwhile, the acknowledgment frame is used to confirm successful framereception. The MAC commands are transmitted using a MAC command frame.

B. Architecture

The super-frame specification in the Beacon frame manages in synchronizing the associated devices, publicizing the existence of PAN, and informing the pending data between coordinators. The super-frame is composed of two parts i.e., active and inactive (refer figure 1.21). Again, the active component is comprised of 16 slots, can further be divided into two subcomponents namely contention access period (CAP) and contention free period (CFP). Inactive part holds the slept devices.

Devices use the slotted CSMA/CA for the usage of the channels in a beacon enabled network. Un slotted CSMA/CA channel mechanism is employed in non-beacon enabled network. Also, network coordinators could provide guarantee time slot (GTS) to the FFDs based on the requisition for fixed rate transmission. The PAN coordinator can be allocated up to 7 GTSs simultaneously. Two parameters control the structure of super-frames. They are beacon order (BO), provide the length of a super-frame and super-frame order (SO), and gives the length of the active portion of the super-frame. A relationship has been developed and evaluated between BO and SO in a beacon enabled network. The relationship is given in the equation 1.

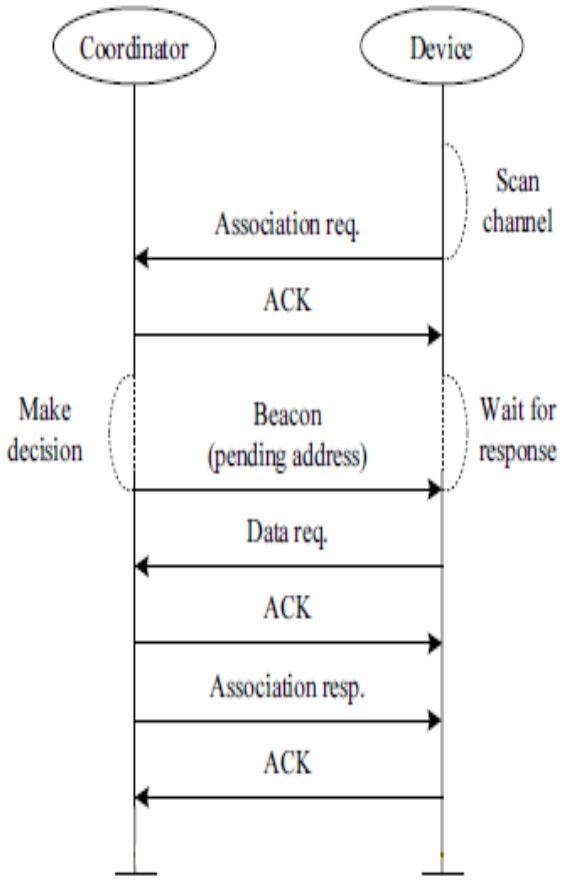
$$0 \leq SO \leq BO \leq 14 \quad \ldots. 1$$

Duty cycle deals could be the ratio of active period to the whole frame duration and is represented in the equation 2. This indicates that the each device gets active for $2^{-(BO-SO)}$ duration of time and goes to sleep for $2^{-(BO-SO)}$ portion of time.

$$\text{Duty Cycle} = 2^{-(BO-SO)} \quad \ldots. 2$$

In the 802.15.4 standard, the association parameters are informed in an indirect fashion. Coordinator receives the association request raised by the devices and responds by appending the *long address* of devices in the beacon frames. Thereafter devices are required to send a data request to the coordinator to fetch the association result. Once association is established, each device will be assigned with a 16-bit *short address.* Figure 2 illustrates the procedure of establishing the associated with the coordinator.

Figure 2: Association Procedure



In the data transfer process for a Beacon enabled network, device locates the beacon to synchronize its super-frame specification. Here CSMA/CA protocol is employed to transmit the data. In a non-beacon enabled network, data transfer is performed by device using un-slotted CSMA/CA. Figure 3 illustrates both the data transfers in the ZigBee MAC.

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Figure 3a: Beacon Network Enabled

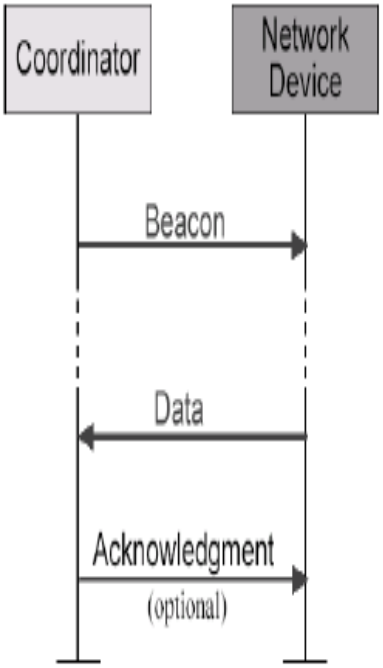
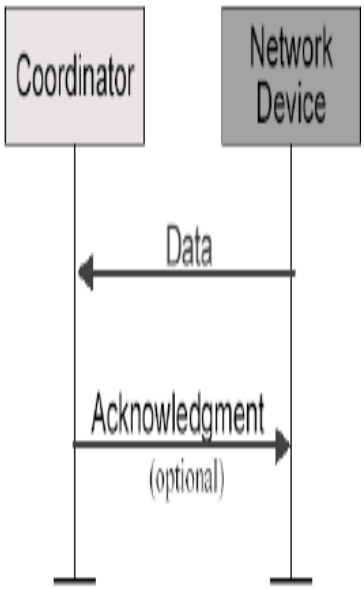
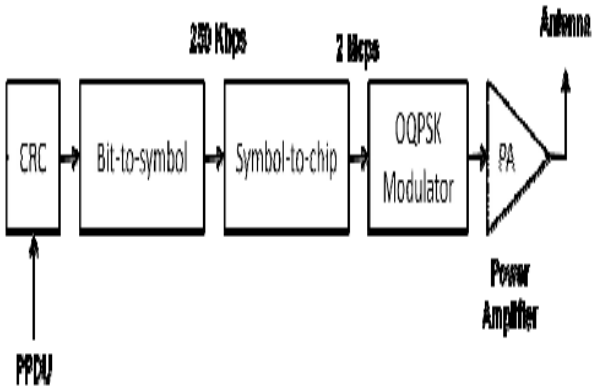


Figure 3b: Non-Beacon Network Enabled ZigBee MAC.



The ZigBee Digital Transmitter which has been designed for an acknowledgment frame is shown in Figure 3 based on IEEE 802.15.4 standard. In existing work, the resultant signal from the general architecture is amplified and then transmitted, which undergoes inter symbol interference. This will result in erroneous information transmission.

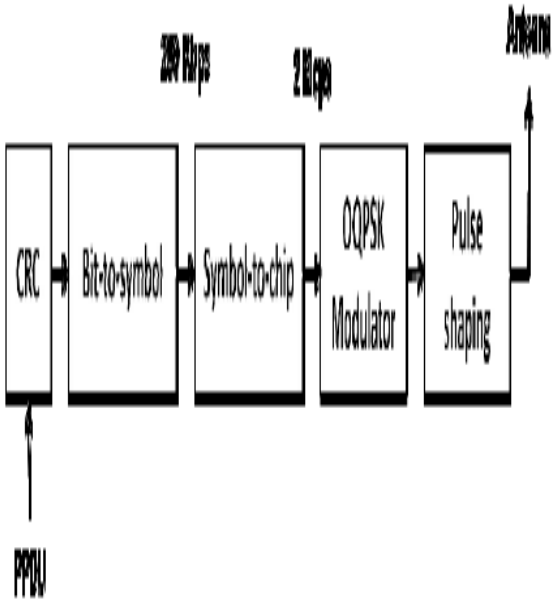
Figure 4: Transmitter Architecture



C. Proposed system

A ZigBee transmitter is to be designed for PHY and MAC layer for an acknowledgement frame. This design (Refer figure 4) is going to be modeled using Verilog HDL and simulated through Xilinx. The performance in terms of power utilization of operation of the proposed design should satisfy the theoretical specifications and is evaluated with the simulation results.

Figure5: Proposed Transmitter Architecture



Since the output of the modulator is not assured to be transmitted without error. So, in order to avoid such distortions, at the output of the OQPSK Modulator we need to add Pulse Shaping block to avoid Inter Symbol Interference and some transmission noises

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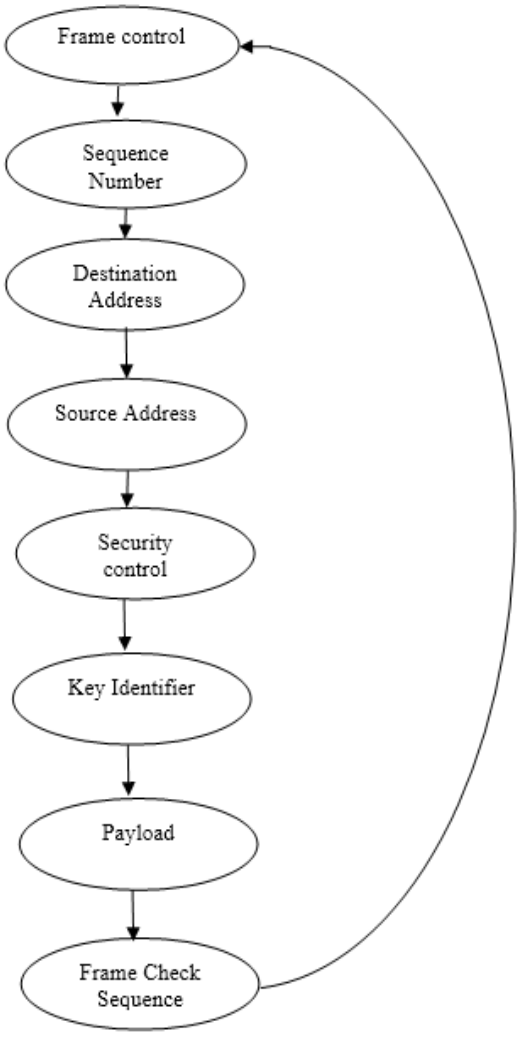
IV. DESIGN METHODOLOGY

A. *Proposed method algorithm:*

The design algorithm defines the frame structure generated by ZigBee MAC layer as follows in figure 6. Generic MAC layer frame has 2 octets frame control field. The useful information which it carries is frame type, source and destination addressing modes. Frame type can be any of the following beacon frame, data frame, ACK of data and MAC command frame. The same is shown as 'Frame type subfield' in the table below with 3 bits. The Sequence number describes the frame sequence order. Destination address is sent first to indicate the target device which is ready to receive the data. Source address is sent after to indicate from which device data is received to the target. Security control field indicates whether outgoing frame is security enabled or not. The Actual data is sent on a payload field. At last the frame check sequence is sent to tell the receiver whether the data is received correctly at the destination or it may collided with unknown data. The receiver also calculates the frame check sequence according to the same polynomial used by the transmitter to calculate the frame check sequence.

Figure 6: Algorithm used for ZigBee MAC transmitter design



B. *Frame Check Sequence*

a) *Cyclic redundancy check:* Error detection is a process to generate the redundant bits using the CRC polynomial with respect to data transmission and identifies the error occurred by comparing the CRC generated with the receiving CRC. Error-detection techniques only detects whether an occurred in the transmitted but will not correct any errors nor identifies the error position. The purpose of error detection is not to prevent errors from occurring but to prevent undetected errors from occurring. The most widely used error detection techniques are redundant bit check such as vertical redundancy checking, checksum, longitudinal redundancy check and cyclic redundancy check.

b)CRC polynomial: The most dependable redundancy check technique for error detection is a convolution coding scheme called Cyclic Redundancy Check Technique (CRC). With CRC, approximately 99.999% of all transmission errors are detected. In CRC-16, 16 bits are used for the block check sequence. Here, the entire data stream is being treated as a long continuous binary number. The Block CheckSequence (BCS) is transmitted separately from the message and CRC is considered as a separate systematic code. The Cyclic Block Code is very often written as (n, k), cyclic codes where n = bit length of transmission and k = length of the message in bits. Therefore the Block Check Character (BCC) length in bits is

$$BCC = n - k \qquad (1)$$

A CRC-16 BCC is the process of binary division to obtain the remainder. P(x) is the generator polynomial is used to divide the message polynomial G(x) to obtain the remainder and append to the BCS message. The generator polynomial must be a prime number. With CRC Generation Polynomial, the division is not done with standard arithmetic division. In the proposed system the division logic is obtained by using modulo-2 division and the remainder is obtained by XOR operation. Whereas in the receiver data stream including the CRC code is divided by the same generating function P(x). The remainder will be zero if no transmission errors are present in the received data.

Mathematically, a CRC can be expressed as

$$\frac{G(x)}{P(x)} = Q(x) + R(x) \qquad (2)$$

Where,
G(x) = message polynomial,
P(x) = generator polynomial,
Q(x) = quotient,
R(x) = remainder,

The generator polynomial for CRC-16 is

$$P(x) = x^{16} + x^{15} + x^2 + x^0$$

Figure 7: CRC-16 Generating circuit

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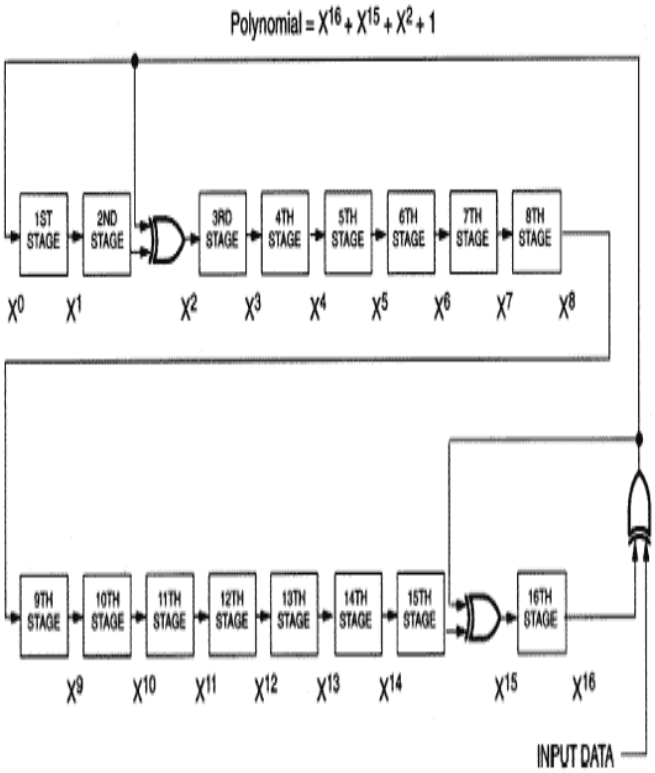

A CRC generating circuit requires a one shift register for each of the bit in the BCC. A review of CRC creation process is as follows:

- Get one raw frame
- Left shift the raw frame by n bits and then divide it by P.
- The remainder of the last action is the Frame Check Sequence.
- The FCS is appended to the message frame. The result is the frame to transmit.

CRC-16 detects

- Any single-bit errors
- All double-bit errors
- All odd number of bit errors
- All error bursts with 16 bits or less
- 99.9% of error bursts with more than 16 bits

c) *3Bit-to-symbol block:* All the 88 bits from the CRC block is inserted into the bit-to-symbol block. This binary data is mapped into the data symbol. The four LSBs (b0,b1,b2,b3) of each octet is being mapped into one data symbol and maps 4 MSBs (b4, b5, b6, b7) of each octet into the next symbol of message. The bit-to-symbol block is used to process sequentially the each octet of PPDU, beginning with the Preamble field and ending with the PSDU octet which is the last one and 22 symbols shall be the output of the bit-to-symbol block for the final result.

d) *Results and discussion:*

Figure 8: Transmitter Simulation Waveform

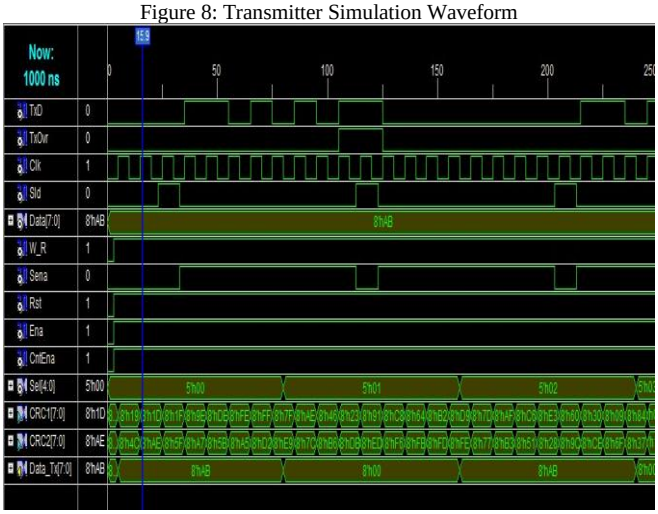

Figure 9: CRC Simulation Waveform

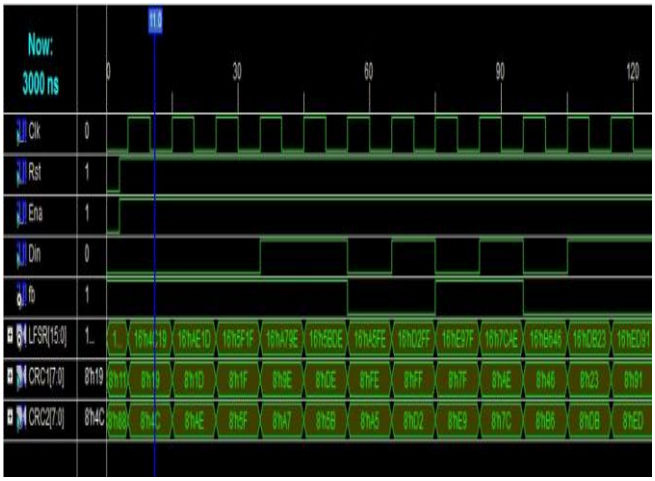

Figure 10: RTL schematic of ZigBee transmitter

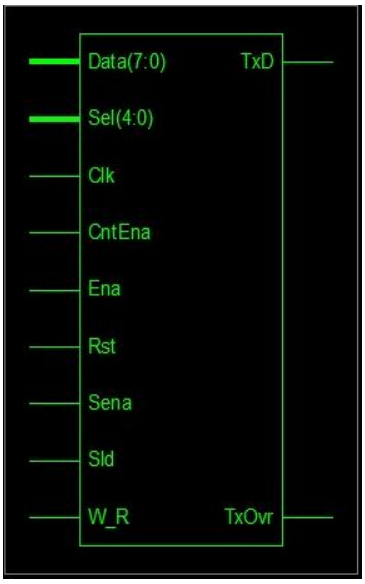

Figure 11: RTL schematic of ZigBeeTtrans mitter

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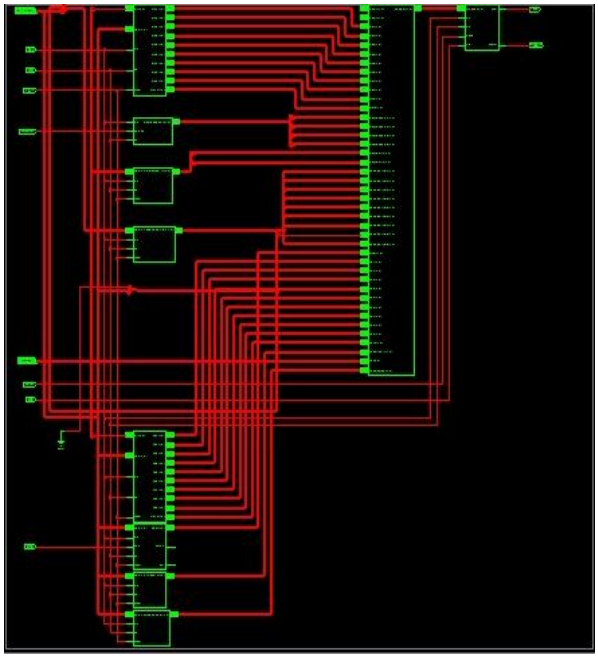


Figure 13: Power Report of Existing ZigBee Transmitter

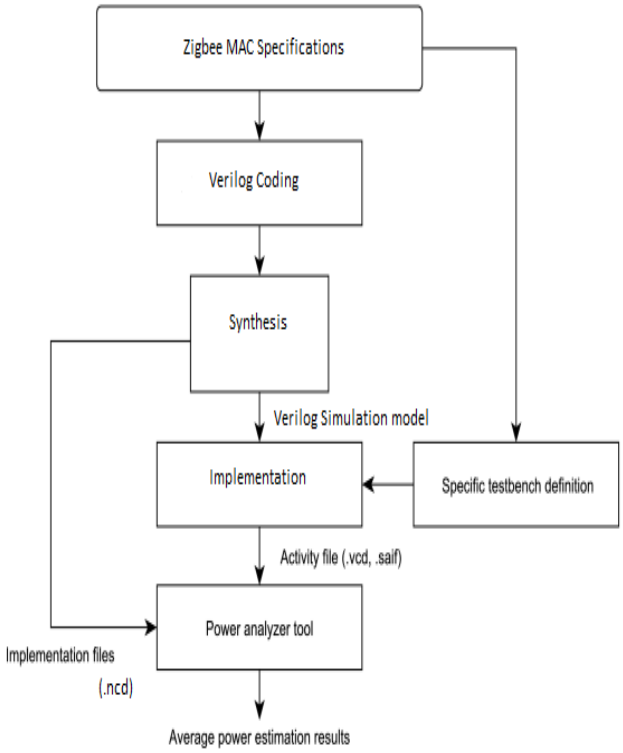


Figure 13: Power Report of Existing ZigBee Transmitter

Design:	E:\vlsi\nits\mtech\can\76326052canbus(FPGA)\zigbee_crc\TOP_ existing.ncd
Preferences:	E:\vlsi\nits\mtech\can\76326052canbus(FPGA)\zigbee_crc\TOP_ existing.pcf
VCD File:	E:\vlsi\nits\mtech\can\76326052canbus(FPGA)\zigbee_crc\top_ tb_existing.vcd
Part:	3s500ecp132-5
Data version:	ADVANCED,v1.0,10-03-03

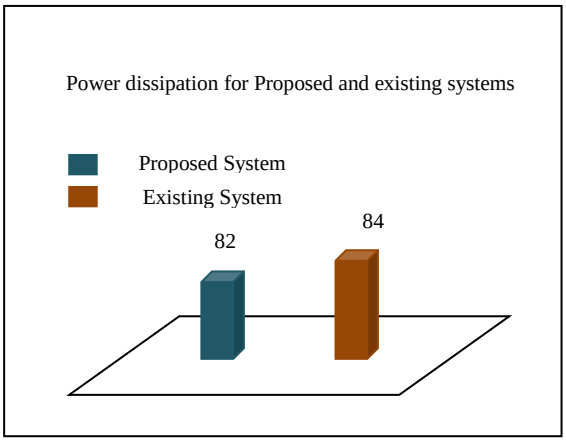
Power summary:	I(mA)	P(mW)
Total estimated power consumption:		84
Vccint 1.20V:	26	32
Vccaux 2.50V:	18	45
Vcco25 2.50V:	3	8
Clocks:	0	0
Inputs:	0	0
Logic:	0	0
Outputs:		

Figure 14: Power Report of Proposed ZigBee Transmitter

Design:	E:\vlsi\nits\mtech\can\76326052canbus(FPGA)\zigbee_crc\TOP_ proposed.ncd
Preferences:	E:\vlsi\nits\mtech\can\76326052canbus(FPGA)\zigbee_crc\TOP_ existing.pcf
VCD File:	E:\vlsi\nits\mtech\can\76326052canbus(FPGA)\zigbee_crc\top_ tb_proposed.vcd
Part:	3s500ecp132-5
Data version:	ADVANCED,v1.0,10-03-03

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		82
Vccint 1.20V:	26	32
Vccaux 2.50V:	18	45
Vcco25 2.50V:	2	6
Clocks:	0	0
Inputs:	0	0
Logic:	0	0
Outputs:		

Figure 15: The Pictogram representation of Power reduction



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The digital transmitter has been partially designed and synthesized for Spartan 3E with a speed grade of 5. The power results have been obtained from the Xilinx power estimator XPOWER tool. From the power resultspower obtained for the proposed ZigBee transmitter is reduced when compared to the existing ZigBee transmitter. From the results it is observed that the power reduction achieved for the proposed system is around 10 % less when compared to conventional system.

V . FUTURE WORK PLAN

The Bit-to-Symbol is to be successfully verified to feed the next block. Otherwise this block has to be synthesized and number of Slices is to be utilized has got to study and design Symbol-to-Chip Mapper. So this part is to be designed with the help of Direct Sequence Spread Spectrum Technique and to study and design Offset Quadrature Phase Shift Keying (O-QPSK). To study and design offset Quadrature Phase Shift Keying (O-QPSK) modulation technique. This Modulation Technique alone is very much suitable for 2.4GHz band of ZigBee Transmitter. To deeply study and design pulse shaping block for modulated output, which will reduce the Inter Symbol Interference (ISI).

V. CONCLUSION

This paper shows the Verilog based design of digital transmitter for 2.4GHz band ZigBee applications. The behavior of CRC and Bit-to-symbol were characterized using Verilog. From the discussion, so far, part of the ZigBee transmitter alone is characterized and synthesized. The synthesis is done by using XILINX ISE and targeted for SPARTAN 3E FPGA. The power results have been obtained from the Xilinx power estimator XPOWER tool. The results obtained for the Proposed ZigBee have consumed less power when compare to the existing. Hence the proposed method proves the ZigBee design by optimized power.

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