International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 4 Issue 06, June-2015

A Comprehensive Review on Single-Phase Five-level Inverter Topologies

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***Abstract*— Multilevel inverters have been developed to handle high power and high voltage in the flexible power systems. These inverters offer some inherent advantages over conventional 2-level inverters. High quality of the output voltage of the multilevel inverters is one of the most important advantages. Though the multilevel inverters hold attractive features, usage of more switches in the conventional configuration poses a limitation to its wide range application. The emphasis is on reducing the number of switches, which inturn reduces switching losses, and avoiding the capacitors, which may likely to cause voltage imbalance, and using less number of DC sources, which may increase additional isolation Transformer requirements, while designing a new prototype. A review has been done on the recently proposed topologies. A control strategy is proposed in this paper to minimize total harmonic distortion (THD) and a comparative analysis has been made with level shifted pulse width modulation (LSPWM).A prototype has been constructed with less switch count. The simulation analysis is done using PSIM-9.3 and validated through experimentation.**

Keywords*— Cascaded Multilevel Inverter, Hybrid Topologies, Total Harmonic Distortion, switch count.

I. INTRODUCTION

In order to reach high voltage and high power with available switching devices and improve output waveforms, multilevel inverters have been developed. Over the last decade, great advances have been made in multilevel inverter/converter topologies. In the literature, there are three traditional structures that were investigated in early and mid-1990s: the diode-clamped multilevel inverter, which derived from the neutral-point clamped inverter invented in 1979, the capacitor-clamped multilevel inverter or flying capacitor in 1992, and the cascade multilevel inverter in 1995. As multilevel inverters are gaining increasing importance, newer topologies are being proposed to reduce part count for large number of levels in output voltage. These research breakthroughs have made the cascade multilevel inverters a perfect topology for power system applications such as FACTS devices. Many papers have addressed the voltage unbalance problem that is inherent to all these multilevel inverters, unless each voltage level is provided by a separate and isolated dc source such as the cascaded multilevel inverter for medium voltage motor drives [8]. A generalized multilevel inverter topology was proposed to achieve automatic voltage balance of each dc voltage without additional balancing circuits in 2000.More recently published topologies[1-5] can categorized as Type-A, Type-B and Type-C Multi Level Inverter (MLI) topologies. Basic single phase five level topologies presented here requires minimum of Two Isolated DC Voltage sources or Series of Capacitors supplied from one DC source.

In this paper section II gives comparative analysis of various topological structures. The operating modes of adopted topology is discussed in section III. Section IV describes the proposed control scheme. The simulation and experimental results are presented in section V, followed by concluding remarks in section VI.

II. FIVE LEVEL INVERTER TOPOLOGIES

A. Type A topology

In Type A there exist two sections namely Level selection part and Polarity Reversal part [1]. Level selection can be done by an Auxiliary bidirectional switch and a 4-switch Bridge takes care of polarity reversal enabling bipolar voltage levels. The basic five level Topology is shown in Fig. 1. (a)

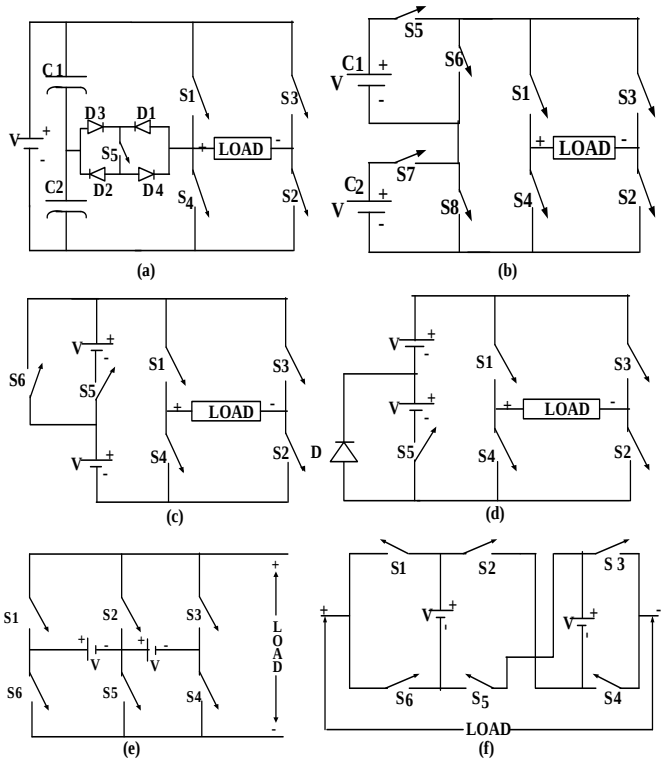


Fig. 1. Recently proposed topologies

B. *Type B topology:*

The Level selection in Type B contains switches only and/or Diodes and Polarity Reversal part [2,4]. The Level selection can be done by only four bidirectional switches and a 4-switch Bridge takes care of polarity reversal enabling bipolar voltage levels as depicted in Fig. 1.(c) and Fig. 1.(d)

C. *Type C topology*

The Type C is formed by back-to-back connection of two H bridges [3-5], which has three leg structure with six unidirectional as depicted in Fig. 1.(e).In the literature same three leg topology is depicted in Fig.1.(f) as cross-connected structure and in Asymmetrical case this topology synthesizes seven levels with middle leg requiring bidirectional natured.

D. *Cascaded H-Bridge multilevel inverter*

The cascaded H-bridge multilevel inverter single phase five level as shown in Fig.2. In conventional multilevel inverters cascaded H-bridge is best topology due to its inherent advantages for medium voltage and high power applications.

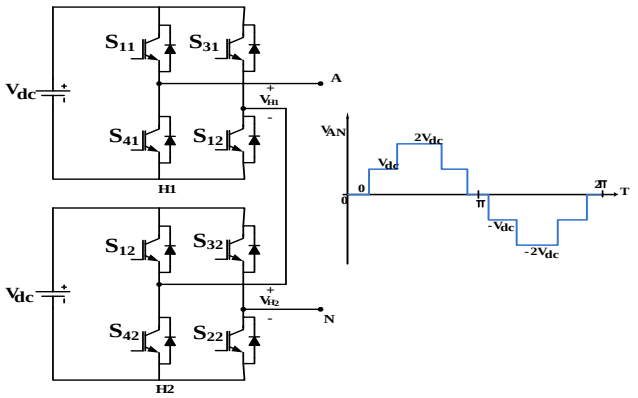


Fig.2 Cascade H-Bridge inverter

E. *comparision:*

Cascade H-Bridge is compared with various recent topologies. A comparative analysis has been done as listed in the Table I keeping in the view of minimizing number of switching devices for synthesizing five level output waveform. The analysis is further generalized for N levels as shown in Fig. 3. The topology shown in Fig. 1. (d) Is adopted for implementation for further analysis.

Table. I. Comparison of various topologies

Sr.No	Topology	Number of Switches		Diodes
		n levels	5 level	
1	Cascaded H-Bridge	2(n-1)	8	0
2	Type A	(n+5)/2	5	4
3	Type B Fig 1.b	n+3	8	16
4	Type B Fig 1.c	n+1	6	0
5	Type B Fig 1.d	(n+5)/2	5	1
6	Type C	n+1	6	0

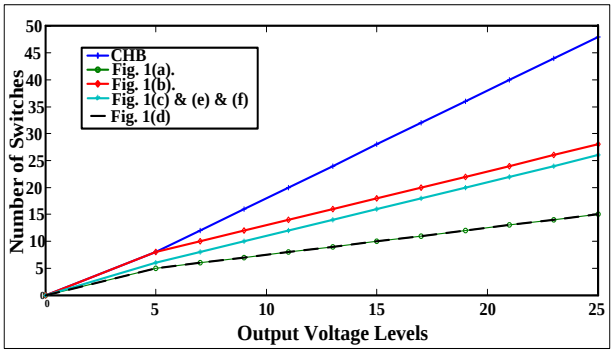


Fig. 3. Comparison of Various Topologies.

In view of less number of switch count the type A suits. Type B Fig.1. (d) is preferable for a basic five level topology.

III. OPERATING MODES OF IMPLEMENTED FIVE-LEVEL INVRTER

The inverter produces output voltage in five levels: zero, Vdc, $2V_{dc}$, 0,$-V_{dc}$ and $-2V_{dc}$.The advantages of the inverter topology are: Improved output voltage quality, smaller filter size, Lower Electromagnetic interferences, and Lower total harmonics distortion compared with conventional five level pulse width modulation ,Reduced number of switches compared to the conventional 5-level inverter. The cascaded H-bridges multilevel inverter introduces the idea of using separate dc sources to produce an ac voltage waveform. Each H-bridge inverter is connected to its own DC source V_{dc}. By cascading the ac outputs of each H bridge inverter, ac voltage waveform is produced. By closing the appropriate switches, each H-bridge inverter can produce five different voltages: When a switch S1 and S_3 of one particular H-bridge inverter are closed, the output voltage is 0 as shown in Fig.4. (a) .When a switch S_1 and S_2 are closed, the output voltage is +Vdc as shown in Fig.4. (b). When a switch S_1, S_2 and S_5 are closed, the output voltage is +2Vdc as shown in Fig.4. (c). When a switch S_2 and S_4 are closed, the output voltage is 0 as shown in Fig.4. (d).when a switch S_3 and S_4 of one particular H-bridge inverter are closed, the output voltage is $-V_{dc}$ as shown in Fig.4. (e). When a switch S_3, S_4 and S_5 are closed, the output voltage is $-2V_{dc}$ as shown in Fig.4. (f). Where the H stands for one particular H-bridge inverter. Therefore, to obtain the total ac voltage produced by the multilevel inverter, these five distinct dc voltages are added together.

Table. II. Switching States.

S.no	S1	S2	S3	S4	S5	V_0
1.	On	On	Off	Off	On	2V
2.	On	On	Off	Off	Off	V
3.	On	Off	On	Off	Off	0
4.	Off	On	Off	On	Off	
5.	Off	Off	On	On	Off	-V
6.	Off	Off	On	On	On	-2V

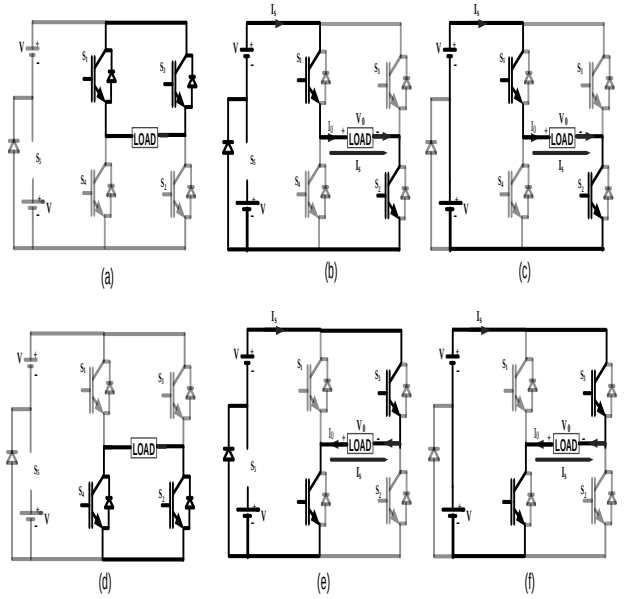


Fig. 4. Operating modes

(a) '0' Level (b) 'V' Level (c) '2V' Level

(d) '0' Level (e) '-V' Level (f) '-2V' Level

IV. PROPOSED CONTROL SCHEME

In literature various switching procedure is like level-shifted sinusoidal pulse-width modulation (LS-SPWM), selective harmonic elimination (SHE) and SVPWM [10].The popular scheme is space-vector PWM but it becomes very complicated for more than three levels and hence the scheme is not dealt with in this paper. The proposed switching scheme to get minimum THD as shown in Fig.6.

A. Calculation of switching angles

THD Derivation For 5-Level:

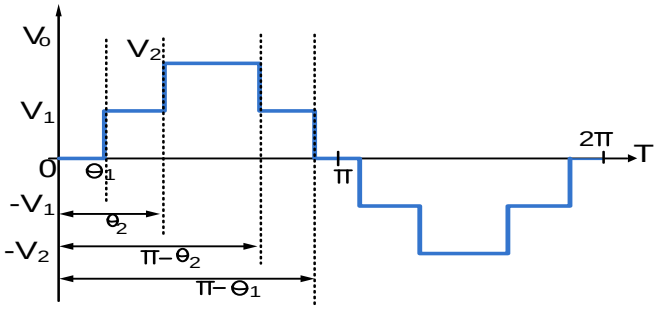


Fig. 5. Five level output voltage waveform.

Rms value output voltage calculated below

$$V_{Orms}^{2} = \frac{1}{\pi}\left[\int_{\theta 1}^{\theta 2} V_1^2 d\theta + \int_{\theta 2}^{\pi-\theta 2} V_1^2 d\theta + \int_{\pi-\theta 2}^{\pi-\theta 1} V_1^2 d\theta\right] \quad \ldots\ldots\ldots\ldots(1)$$

$$V_{O,rms} = \sqrt{\frac{2V_1^2(\theta_2-\theta_1)+V_2^2(\pi-2\theta_2)}{\pi}} \quad \ldots\ldots\ldots\ldots(2)$$

Fundamental value of output voltage calculated using Fourier analysis

$$V_{Out} = B_n * \sin(nwt)\ ; n = 0 \ \ to\ \infty \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(3)$$

$$B_n = 2\left(1-(-1)^n\right)\left[a(\cos n\theta_1 - \cos n\theta_2) + b(\cos n\theta_2)\right]/n\pi$$

$$V_{f1} = 4\left[a(\cos\theta_1 - \cos\theta_2) + b(\cos\theta_2)\right]/\pi \ldots\ldots\ldots\ldots(4)$$

$$THD = \sqrt{\frac{V_{Orms}^2 - V_{frms}^2}{V_{frms}^2}} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(5)$$

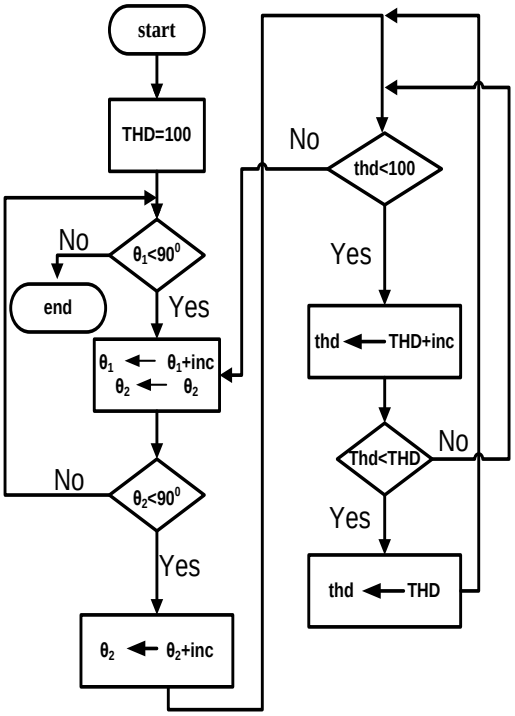


Fig.6. Proposed control scheme.

Using (2), (4), (5) equations and proposed control scheme shown in fig.6. These implemented through Matlab programming switching anglesθ_1, θ_2 are calculated.

V. SIMULATIO RESULTS AND EXPERIMENTAL RESULTS

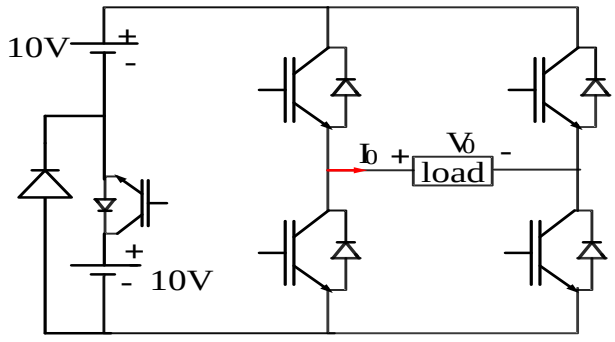


Fig.7. Switched diode structure five-level inverter

A. *Simulation Results*

The switched diode structure is simulated using PSIM 9.3 for symmetrical sources of each V_{dc}=10V as shown in Fig. 7. The results are obtained with a resistive load with R=200 Ω using LSSPWM with the switching frequency of 1.15 kHz with modulation index m=1.0. The voltage waveform and its FFT analysis as shown in Fig.8.

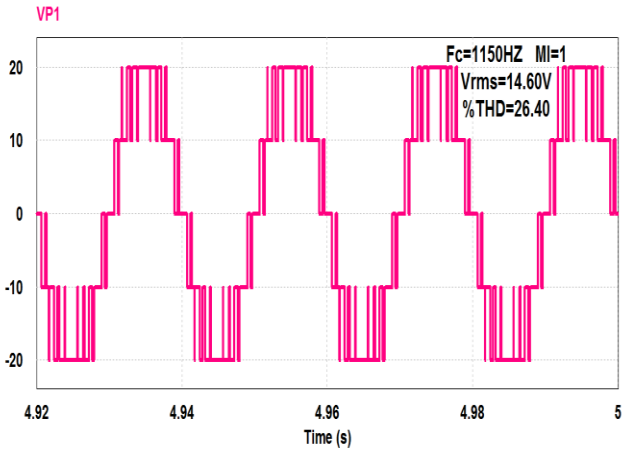


Fig. 8. (a) Output voltage

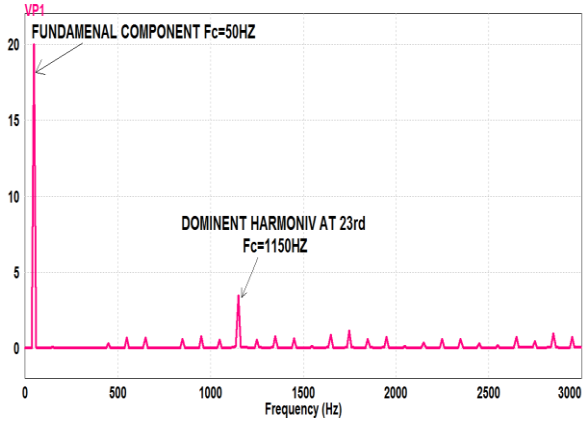


Fig. 8. (b) FFT analysis

Table .III. Percentage of THD in Output voltage of recent topology

Modulation index	%THD at fc= 1KHz	%THD at fc= 2 KHz	%THD at fc= 3 KHz	%THD at fc= 5 KHz
0.3	106	106.27	106.1	108.7
0.5	52.05	52.29	52.05	53.68
0.7	41.3	42.07	41.83	42.25
0.75	40.18	40.12	40.26	40.52
0.8	38.28	38.37	38.38	38.70
0.9	33.26	33.61	33.45	33.92
1	26.81	27.04	26.78	27.30

From table we observed that as the modulation index increases percentage THD of output voltage decreases.

The switched diode structure is simulated using PSIM 9.3 for symmetrical sources of each V_{dc}=10V as shown in Fig. 7. The results are obtained with a resistive load with R=200 Ω using proposed control scheme with fundamental frequency. The voltage waveform and its FFT analysis as shown in Fig.9.

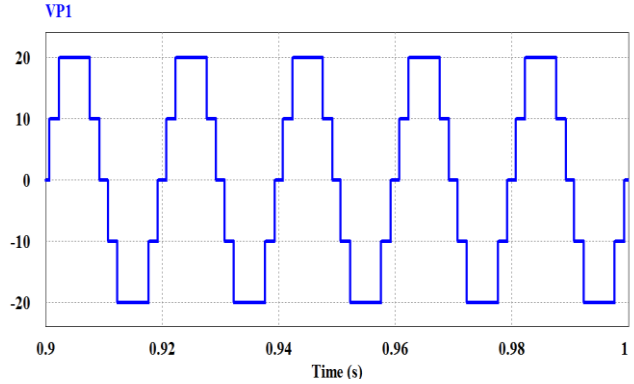


Fig. 9. (a) Output voltage waveform of proposed scheme

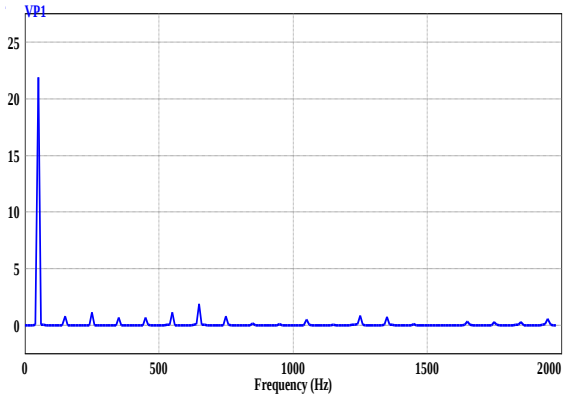


Fig. 9. (b) FFT analysis

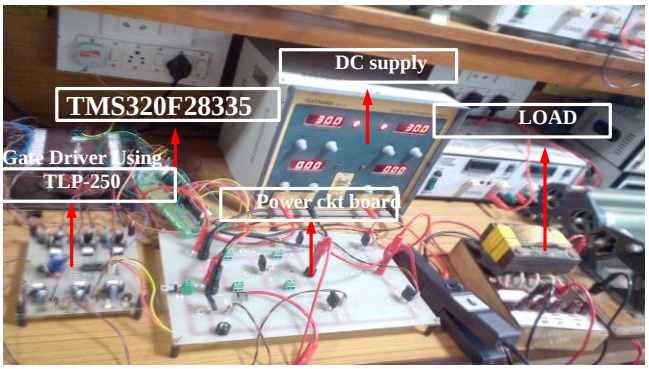
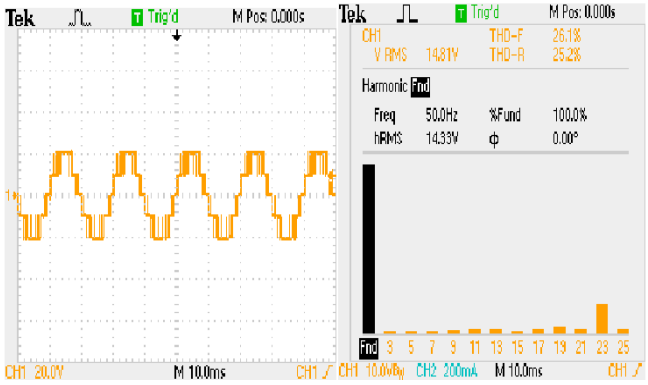


Fig. 10. Hardware Setup

B. *Experimental results*

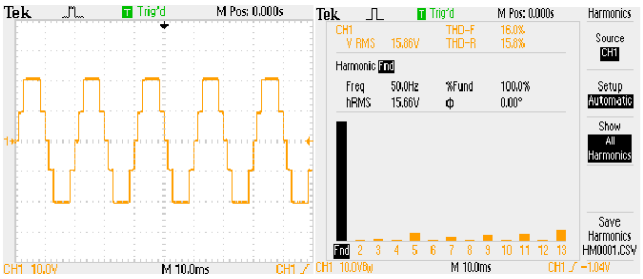
The prototype hardware setup as shown in Fig.10.the proposed algorithm implemented digitally by using DSP TMS320F28335 with the code composer studio 6.0. The Switched diode structure five-level inverter is accommodated in the laboratory shown in Fig. The IGBTs are used in the prototype are IRG4PH50UD and the diode used is RHRP30120. The recent multilevel inverter is tested with isolated dc power supplies of 10V, 2A with R-load R=200 ohm .The THD analysis is done using TPS2024B with application key, which can evaluate harmonics up to 50th order.

The output voltage waveform and FFT analysis are shown in Fig.11 (a) and (b) with switching frequency 1.15 KHz and with proposed control algorithm in Fig.12 (a) and (b) respectively



(a) (b)

Fig. 11. (a) Output voltage waveform (b) FFT analysis



(a) (b)

Fig. 12 (a) Output voltage waveform (b) FFT analysis

VI. CONCLUSION

The comparison has been made on recent multi-level inverter topologies in view of reducing number of switches. A control strategy is proposed to reduce the THD in output voltage and the results are compared with those of LSPWM by simulation. The simulation results are validated by constructing the prototype. The results are summarized in the table IV. The proposed control scheme produce minimum THD with less switching loss. The topology implemented in this paper is an efficient one because it consists of less switches producing less switching loss, and it is operated by proposed control scheme which produces minimum THD with minimum switching loss.

TABLE IV Comparison of simulation and hardware results

Sr.No.	Switching technique	Switching frequency	%THD	
			Simulation result	Hardware result
1.	Level shifted SPWM	1.15 kHz	26.4	26.1
2.	Proposed control scheme	50 Hz	16.42	16.0

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