

A DC/DC Converter with High Voltage Gain Using Soft-Switching Technique

B.Srujana, D.Kumaraswamy, D.R.K Paramahamsa

Abstract—A soft-switching dc/dc converter with high voltage gain is proposed in this paper. It provides a continuous input current and high voltage gain. Moreover, soft-switching characteristic of the proposed converter reduces switching loss of active power switches and raises the conversion efficiency. The reverse-recovery problem of output rectifiers is also alleviated by controlling the current changing rates of diodes with the use of the leakage inductance of a coupled inductor. The paper can be extended with some features like ZVS technique to reduce losses even more. A zero-voltage-switching (ZVS) dc–dc converter with high voltage gain can be presented. It consists of a ZVS boost converter stage and a ZVS half-bridge converter stage and two stages are merged into a single stage. The ZVS boost converter stage provides a continuous input current and ZVS operation of the power switches. The ZVS half-bridge converter stage provides a high voltage gain.

Index Terms—Boost converter, high voltage gain, soft switching.

I. INTRODUCTION

RECENTLY, the demand for dc/dc converters with high voltage gain has increased. The energy shortage and the atmosphere pollution have led to more researches on the renewable and green energy sources such as the solar arrays and the fuel cells [1]–[5]. Moreover, the power systems based on battery sources and super capacitors have been increased. Unfortunately, the output voltages of these sources are relatively low. Therefore, the step-up power conversion is required in these systems [6], [7]. Besides the step-up function, the demands such as low current ripple, high efficiency, fast dynamics, light weight, and high power density have also increased for various applications. Input current ripple is an important factor in a high step-up dc/dc converter [8], [9]. Especially in the fuel cell systems, reducing the input current ripple is very important because the large current ripple shortens fuel cell's lifetime as well as decreases performances [10]–[14]. Therefore, current-fed converters are commonly used due to their ability to reduce the current ripple [15].

In applications that require a voltage step-up function and a continuous input current, a continuous-conduction-mode (CCM) boost converter is often used due to its advantages such as continuous input current and simple structure. However, it has a limited voltage gain due to its parasitic components. Moreover the

reverse-recovery problem of the output diode degrades the system's performances. At the moment when the switch turns on, the reverse-recovery phenomenon of the output diode of the boost converter is provoked. The switch is submitted to a high current change rate and a high peak of reverse-recovery current. The parasitic inductance that exists in the current loop causes a ringing of the parasitic voltage, and then, it increases

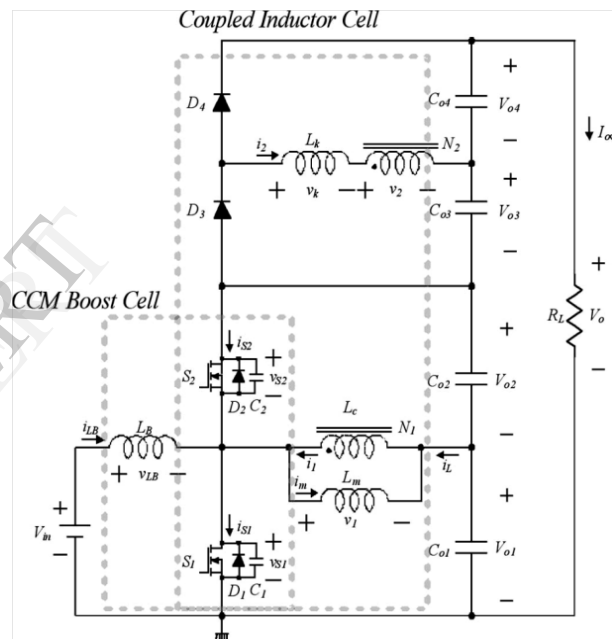


Fig. 1. Circuit diagram of the proposed dc/dc converter.

the voltage stresses of the switch and the output diode. These effects significantly contribute to increase switching losses and electromagnetic interference. The reverse-recovery problem of the output diodes is another important factor in dc/dc converters with high voltage gain [16], [17]. In order to overcome these problems, various topologies have been introduced. In order to extend the voltage gain, the boost converters with coupled inductors are proposed in [18] and [19]. Their voltage gains are extended, but they lose a continuous input current characteristic and the efficiency is degraded due to hard switching of power switches. For a continuous input current, current-fed step-up converters are proposed in [20] and [21]. They provide high voltage gain and galvanic isolation. However, the additional snubbers are required to reduce the voltage stresses of switches. In order to

increase the efficiency and power conversion density, a soft-switching technique is required in dc/dc converters [22]–[27].

A soft-switching dc/dc converter with high voltage gain, which is shown in Fig. 1, is proposed. A CCM boost cell provides a continuous input current. To increase the voltage gain, the output of the coupled inductor cell is laid on the top of the output of the CCM boost cell. Therefore, the high voltage gain is obtained without high turn ratio of the coupled inductor, and the voltage stresses of the switches are confined to the output voltage of the CCM boost cell. A zero-voltage-switching (ZVS) operation of the power switches reduces the switching loss during the switching transition and improves the overall efficiency.

II. ANALYSIS OF THE PROPOSED CONVERTER

Fig. 1 shows the circuit diagram of the proposed soft switching dc/dc converter with high voltage gain. Its key waveforms are shown in Fig. 2. The switches S_1 and S_2 are operated asymmetrically and the duty ratio D is based on the switch S_1 . D_1 and D_2 are intrinsic body diodes of S_1 and S_2 . Capacitors C_1 and C_2 are the parasitic output capacitances of S_1 and S_2 . The proposed converter contains a CCM boost cell. It consists of L_B , S_1 , S_2 , C_{o1} and C_{o2} . The CCM boost cell provides a continuous input current. When the switch S_1 is turned on, the boost inductor current i_{LB} increases linearly from its minimum value I_{LB2} to its maximum value I_{LB1} . When the switch S_1 is turned off and the switch S_2 is turned on, the current i_{LB} decreases linearly from I_{LB1} to I_{LB2} . Therefore, the output capacitor voltages V_{o1} and V_{o2} can be derived easily as

$$V_{o1} = V_{in} \quad (1)$$

$$V_{o2} = \frac{D}{1-D} V_{in} \quad (2)$$

To obtain ZVS of S_1 and S_2 and high voltage gain, a coupled inductor L_c is inserted. The coupled inductor L_c is modelled as the magnetizing inductance L_m , the leakage inductance L_k , and the ideal transformer that has a turn ratio of $1:n$ ($n = N_2/N_1$). The voltage doubler consists of diodes D_1 , D_2 and the output capacitors C_{o3} , C_{o4} , and the secondary winding N_2 of the coupled inductor L_c is on the top of the output stage of the boost cell to increase voltage gain. The coupled inductor current i_L varies from its minimum value $-I_{L1}$ to its maximum value I_{L2} . The operation of the proposed converter in one switching period T_s can be divided into six modes. Fig. 3 shows the operating modes. Before t_0 , the switch S_2 and diode D_4 are conducting.

Mode 1 [t_0, t_1]: At t_0 , the switch S_2 is turned off. Then, the boost inductor current i_{LB} and the coupled inductor current i_L start to charge C_2 and discharge C_1 . Therefore, the voltage v_{S1} across S_1 starts to fall and the voltage v_{S2} across S_2 starts to rise. The transition interval T_{t1} of switches can be considered as

$$T_{t1} = \frac{(C_1 + C_2)V_{in}}{(1-D)(I_{L1} \cdot I_{LB2})} \quad (3)$$

Since the output capacitances C_1 and C_2 of the switches are very small, the transition interval T_{t1} is very short and it can be neglected. Therefore, the inductor currents i_{LB} and i_L can be considered to have constant values during mode 1.

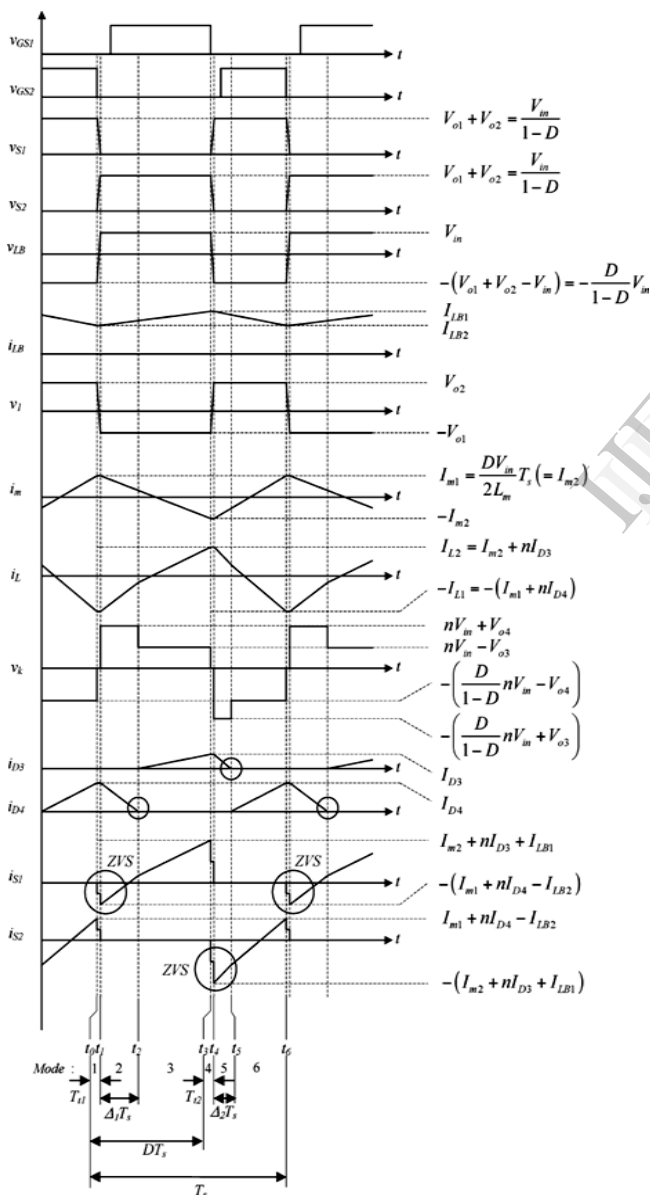


Fig. 2. Key waveforms of the proposed converter.

Mode 2 [t_1, t_2]: At t_1 , the voltage v_{S1} across the lower switch S_1 becomes zero and the lower diode D_1 is turned on. Then, the gate signal is applied to the switch S_1 . Since the current has already flown through the lower diode D_1 and the voltage v_{S1} becomes zero before the switch S_1 is turned on, zero-voltage turn-ON of S_1 is achieved. Since the voltage across the boost inductor L_B is V_{in} , the boost inductor current increases linearly from I_{LB2} . Since v_1 is $-V_{in}$ and v_k is $V_{O4} + nV_{in}$, the magnetizing current i_m , the primary current i_1 , the secondary current i_2 , and the inductor current i_L are given by

$$i_m(t) = i_{m1} - \frac{V_{in}}{L_m}(t - t_1) \tag{4}$$

$$i_2(t) = -I_{D4} + \frac{V_{O4} + nV_{in}}{L_k}(t - t_1) \tag{5}$$

$$i_1(t) = ni_2(t) = nI_{D4} + n \frac{V_{O4} + nV_{in}}{L_k}(t - t_1) \tag{6}$$

$$i_L(t) = -i_m(t) + i_1(t) = -i_{m1} - nI_{D4} + \frac{V_{in}}{L_m}(t - t_1) + n \frac{V_{O4} + nV_{in}}{L_k}(t - t_1) \tag{7}$$

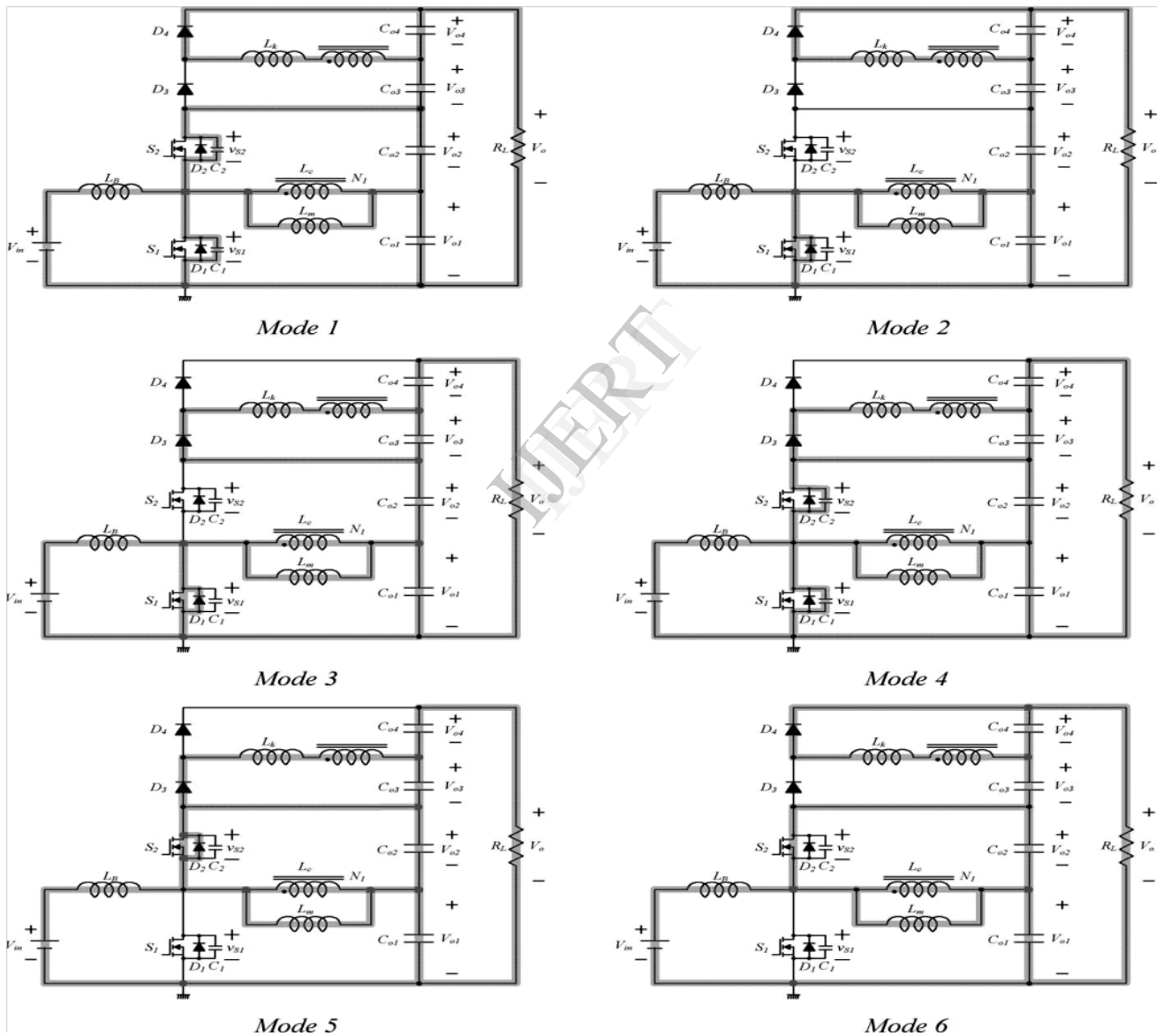


Fig. 3. Operating modes.

Mode 3 [t_2, t_3]: At t_2 , the secondary current i_2 changes its direction. The diode current i_{D4} decreases to zero and the diode D_4 is turned off. Then, diode D_3 is turned on and its current increases linearly. Since the current changing rate

of D_4 is controlled by the leakage inductance of the coupled inductor, its reverse-recovery problem is alleviated. Since v_1 is $-V_{in}$ and v_k is $nV_{in} - V_{O4}$, the current i_m , the primary

current i_1 , the secondary current i_2 , and the inductor current i_L are given by

$$i_m(t) = i_m(t_2) - \frac{V_{in}}{L_m}(t - t_2) \quad (8)$$

$$i_2(t) = \frac{nV_{in} - V_{o3}}{L_k}(t - t_2) \quad (9)$$

$$i_1(t) = ni_2(t) = n \frac{nV_{in} - V_{o3}}{L_k}(t - t_2) \quad (10)$$

$$\begin{aligned} i_L(t) &= -i_m(t) + i_1(t) \\ &= -i_m(t_2) + \frac{V_{in}}{L_m}(t - t_2) + n \frac{nV_{in} - V_{o3}}{L_k}(t - t_2) \end{aligned} \quad (11)$$

Mode 4 [t_3, t_4]: At t_3 , the lower switch S_1 is turned off. Then, the boost inductor current i_{LB} and the coupled inductor current i_L start to charge C_1 and discharge C_2 . Therefore, the voltages v_{s1} and v_{s2} start to rise and fall in a manner similar to that in mode 1. The transition interval T_{t2} of switches can be considered as

$$T_{t2} = \frac{(C_1 + C_2)V_{in}}{(1-D)(I_{L2} - I_{LB1})} \quad (12)$$

T_{t2} is also negligible. Therefore, the inductor currents i_{LB} and i_L can be considered to have constant values during T_{t2} .

Mode 5 [t_4, t_5]: At t_4 , the voltage v_{s2} across the upper switch S_2 becomes zero and the diode D_2 is turned on. Then, the gate signal is applied to the switch S_2 . Since the current has already flown through the diode D_2 and the voltage v_{s2} becomes zero before the switch S_2 is turned on, zero-voltage turn-ON of S_2 is achieved. Since the voltage across the boost inductor LB is $-(V_{in}/(1-D) - V_{in})$, the boost inductor current decreases linearly from I_{LB1} . Since v_1 is $DV_{in}/(1-D)$ and v_k is $-V_{o3} - nDV_{in}/(1-D)$, the magnetizing current i_m , the primary current i_1 , the secondary current i_2 , and the inductor current i_L are given by

$$i_m(t) = -i_{m2} + \frac{DV_{in}}{L_m(1-D)}(t - t_4) \quad (13)$$

$$i_2(t) = I_{D3} - \frac{V_{o3} + (D/1-D)nV_{in}}{L_k}(t - t_4) \quad (14)$$

$$\begin{aligned} i_1(t) &= ni_2(t) \\ &= nI_{D3} - n \frac{V_{o3} + (D/1-D)nV_{in}}{L_k}(t - t_4) \end{aligned} \quad (15)$$

$$\begin{aligned} i_L(t) &= i_{m2} + ni_{D3} \\ &- \left(\frac{DV_{in}}{L_m(1-D)} + nn \frac{V_{o3} + (D/1-D)nV_{in}}{L_k} \right) (t - t_4) \end{aligned} \quad (20)$$

Mode 6 [t_5, t_6]: At t_5 , the secondary current i_2 changes its direction. The diode current i_{D3} decreases to zero and the

diode D_3 is turned off. The reverse-recovery problem of D_3 is also alleviated due to the leakage inductance of L_c . Then, the diode D_4 is turned on and its current increases linearly. Since v_1 is $DV_{in}/(1-D)$ and v_k is $V_{o4} - nDV_{in}/(1-D)$, the current i_m , the primary current i_1 , the secondary current i_2 , and the inductor current i_L are given by

$$i_m(t) = -i_m(t_5) + \frac{DV_{in}}{L_m(1-D)}(t - t_5) \quad (17)$$

$$i_2(t) = -\frac{(D/1-D)nV_{in} - V_{o4}}{L_k}(t - t_5) \quad (18)$$

$$i_1(t) = ni_2(t) = -n \frac{(D/1-D)nV_{in} - V_{o4}}{L_k}(t - t_5) \quad (19)$$

$$\begin{aligned} i_L(t) &= -i_m(t_5) \\ &- \left(\frac{DV_{in}}{L_m(1-D)} + nn \frac{V_{o3} + (D/1-D)nV_{in}}{L_k} \right) (t - t_5) \end{aligned}$$

The average values of v_{LB} and v_1 , V_{o1} can be considered to be V_{in} . Referring to the voltage waveforms v_{LB} in Fig. 2, the volt-second balance law gives

$$V_{in}DT_s - (V_{o1} + V_{o2} - V_{in})(1-D)T_s = 0. \quad (21)$$

From modes 3 and 5, the current I_{D3} can be written as follows:

$$\begin{aligned} I_{D3} &= \frac{nV_{in} - V_{o3}}{L_k}(D - \Delta_1)T_s \\ &= \frac{V_{o3} + (D/1-D)nV_{in}}{L_k} \Delta_2 T_s \end{aligned} \quad (22)$$

from where, the output voltage V_{o3} can be obtained by

$$V_{o3} = \frac{D - \Delta_1 - (D/1-D)\Delta_2}{D - \Delta_1 + \Delta_2} nV_{in} \quad (23)$$

From modes 2 and 6, the current I_{D4} can be written as follows:

$$\begin{aligned} I_{D4} &= \frac{nV_{in} + V_{o4}}{L_k}(\Delta_1)T_s \\ &= \frac{-V_{o4} + (D/1-D)nV_{in}}{L_k}((1-D) - \Delta_2)T_s \end{aligned} \quad (24)$$

from where, the output voltage V_{o4} can be obtained by

$$V_{o4} = \frac{D - \Delta_1 - (D/1-D)\Delta_2}{1 - D + \Delta_1 - \Delta_2} nV_{in} \quad (25)$$

Since the average value of the current i_2 is zero, the following relation can be obtained:

$$(D - \Delta_1 + \Delta_2) I_{D3} = (1 - D + \Delta_1 - \Delta_2) I_{D4}. \quad (26)$$

From (22), (24), (25), and (26), the relation between Δ_1 and Δ_2 is obtained by

$$\frac{\Delta_1}{\Delta_2} = \frac{D}{1-D} \quad (27)$$

Since the average value of the current i_m is zero, its peak values I_{m1} and I_{m2} have the following values:

$$I_{m1} = I_{m2} = \frac{DV_{in}T_s}{2L_m} \quad (28)$$

The output current I_o in Fig. 1 can be represented by

$$I_o = (D - \Delta_1 + \Delta_2) \frac{I_{D3}}{2} = (1 - D + \Delta_1 - \Delta_2) \frac{I_{D4}}{2}. \quad (29)$$

From (22), (27), and (29), Δ_1 and Δ_2 are obtained by

$$\Delta_1 = \alpha D \quad (30)$$

$$\Delta_2 = \alpha (1 - D) \quad (31)$$

where

$$\alpha = \frac{1}{2} \left(1 - \sqrt{1 - \frac{8L_k I_o}{nDV_{in}T_s}} \right)$$

III. CHARACTERISTIC AND DESIGN PARAMETERS

A. Input Current Ripple

The input current ripple ΔI_{LB} can be written as

$$\Delta I_{LB} = I_{LB1} - I_{LB2} = \frac{DV_{in}T_s}{L_B}. \quad (32)$$

To reduce the input current ripple ΔI_{LB} below a specific value I^* , the inductor L_B should satisfy the following condition:

$$L_B > \frac{DV_{in}T_s}{I^*} \quad (33)$$

B. Voltage Gain

From (1), (2), (23), (25), (27), (30), and (31), the voltage gain of the proposed converter is obtained by

$$\frac{V_o}{V_{in}} = \frac{1}{1-D} + \frac{nD(1-\alpha)}{(D-\alpha(2D-1))(1-D+\alpha(2D-1))} \quad (34)$$

$$\frac{V_o}{V_{in}} = \frac{1+n}{1-D} \quad (35)$$

C. ZVS Condition

The ZVS condition for S_2 is given by

$$I_{m2} + nI_{D3} + I_{LB1} > 0 \quad (36)$$

from where, it can be seen that the ZVS of S_2 is easily obtained. For ZVS of S_1 , the following condition should be satisfied:

$$I_{m1} + nI_{D4} > I_{LB2}. \quad (37)$$

On the assumption that α is small, I_{D4} and I_{LB2} can be simplified as follows:

$$I_{D4} = \frac{2I_o}{1-D} \quad (38)$$

$$I_{LB2} = \frac{(n+1)I_o}{1-D} - \frac{\Delta I_{LB}}{2} \quad (39)$$

From (38) and (39), the inequality (37) can be rewritten by

$$I_{m1} + \frac{2nI_o}{1-D} > \frac{\Delta I_{LB}}{2} + \frac{(n+1)I_o}{1-D} - \frac{\Delta I_{LB}}{2} \quad (40)$$

Since I_{m1} , I_o , and ΔI_{LB} are all positive values, the inequality (40) is always satisfied for $n > 1$. From (36) and (40), it can be seen that ZVS conditions for S_1 and S_2 are always satisfied. Moreover, dead times of two switches S_1 and S_2 should be considered. The gate signal should be applied to the switch before the current that flows through the anti parallel diode changes its direction. Namely, the leakage inductance L_k should be large enough for the current to maintain its direction during dead times of two switches, S_1 and S_2 . This condition can determine the minimum value of the leakage inductance. From (30), the leakage inductance L_k should satisfy the following condition:

$$L_k > \frac{nV_{in}DT_s}{8I_o} \left[1 - \left(1 - \frac{2\Delta I^*}{D} \right)^2 \right] \quad (41)$$

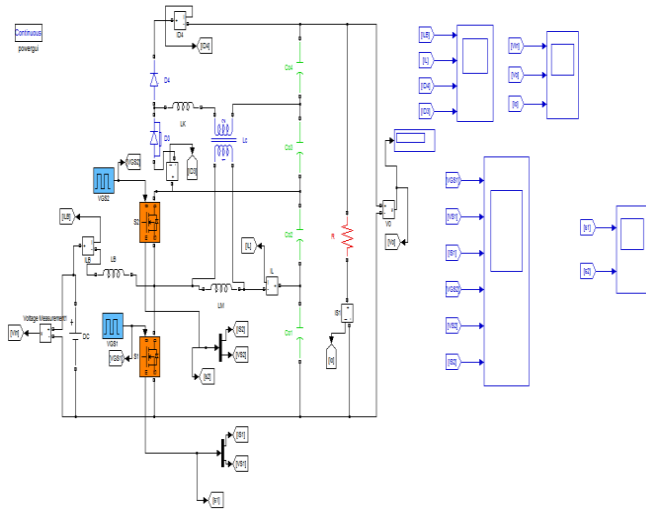
Where ΔI^* is a predetermined minimum value of ΔI_1 . The leakage inductance of the coupled inductor also alleviates the reverse recovery problem of output diode. Large leakage inductance can remove the reverse-recovery problem but it reduces the voltage gain as shown in Fig. 4(b).

III. Future Scope of Work

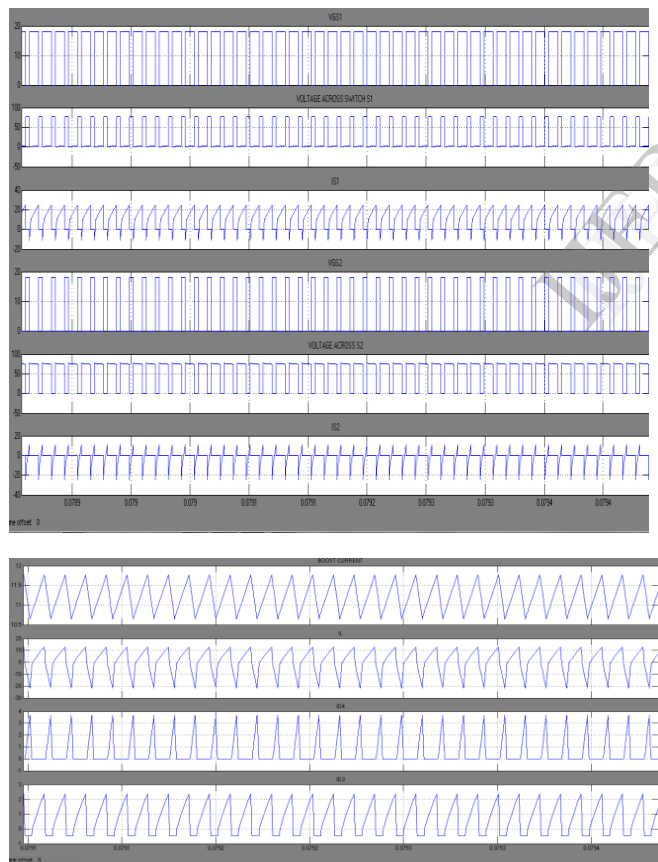
AZVS dc-dc converter with high voltage gain can be suggested. It can achieve ZVS turn-ON of two power switches while maintaining CCM. In addition, the reverse-recovery characteristics of the output diodes were significantly improved by controlling the current changing rate with the use of the leakage inductance of the transformer. The ZVS converter presents a higher efficiency and a wider ZVS region compared to other soft-switching converters due to the ZVS boost converter stage.

IV. Simulation Results

Simulink Model



Simulink Results



V. CONCLUSION

A soft-switching dc/dc converter with high voltage gain has been proposed in this paper. The proposed converter can minimize the voltage stresses of the switching devices and lower the turn ratio of the coupled inductor. It provides a continuous input current, and the ripple components of the

input current can be controlled by using the inductance of the CCM boost cell. Soft switching of power switches and the alleviated reverse-recovery problem of the output rectifiers improve the overall efficiency.

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