A Design of 0.18uM low power full adder

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Abstract

A design of low power full adder circuits, firstly seen the level restorer full adder circuit and novel low power full adder is taken to versus the branch based logic and pass transistor logic in order to overcome the low consumption of the power in the above two methods, a static low power full adder is proposed, transmission gate full adder is designed with low power consumption with 0.18uM technology.

Keywords—level restorer full adder cicuit ,hybrid low power full adder cicuit and static full adder circuits

1. Introduction

The choice of the digital design is to reduce the size of the logic circuits and also the power of the digital logic circuits. In order to reduce the power of the logic circuits we have to reduce the static power as well as the dynamic power of the logic circuits

Although dynamic power is continuously being reduced with technology scaling, static leakage power tends to increase and is expected to become a large contributor to total power in a few technology generations [1]. The Full Adder is the fundamental gate in many arithmetic circuits, such as adders and multipliers. Since

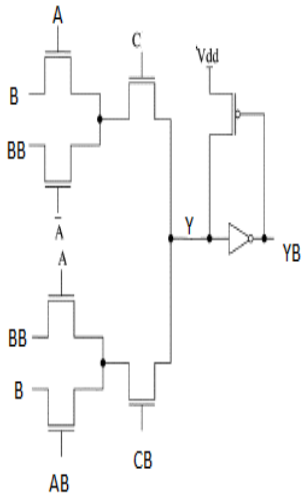
These circuits strongly affect the overall speed performance in current digital integrated circuits [2], their speed optimization is crucial in high-performance applications, and typical applications generally require a tradeoff between power consumption and speed [3]. In addition, as arithmetic circuits significantly contribute to the overall power budget, their power consumption reduction becomes the main objective to pursue in low-power ICs used in portable electronic equipment's. Most of the VLSI applications, such as digital signal processing, image and video processing, and microprocessors, extensively use arithmetic operations. Addition, subtraction, and multiplication are examples of the most commonly used operations. The 1-bit full adder cell is the building block of all these modules. Thus, enhancing its performance is critical for enhancing the overall module performance [4]. Recently, building low-power VLSI systems has emerged as highly in demand because of the fast growing technologies in mobile communication and computation. The battery technology does not advance at the same rate as the microelectronics technology. There is a limited amount of power available for the mobile systems[6]. So designers are faced with more constraints: high. speed, high throughput, small silicon area, and at the same time, low-power consumption. So building low-power, high performance adder cells are of great interest.

A structured approach for designing and analyzing an adder cell is based on decomposing it into smaller modules. Each of these modules is implemented, optimized, and tested separately. Several full adder cells are composed by connecting these modules. The goal of this paper is designing a low-voltage and so low-power full adder This technique that was recently developed and presented in [7], proposes an efficient alternative for logic design in standard CMOS and SOI technologies. With the explosive growth in laptops, portable personal communication systems and the evolution of the shrinking technology, the research effort in low-power microelectronics has been intensified and low-power VLSI systems have emerged as highly in demand. Today, there is an increasing number of portable applications requiring small-area low-power high- throughput circuitry. Therefore, circuits with low power con- assumption become the major candidates for design of microprocessors and system-components[8]. The battery technology does not advance at the same rate as the microelectronics technology and there is a limited amount of power available for the mobile systems. The goal of extending the battery life span of portable electronics is to reduce

the energy consumed per arithmetic operation, but low power consumption does not necessarily imply low energy. To execute an arithmetic operation, a circuit can consume very low power by clocking at extremely low frequency but it may take a very long time to complete the operation. Therefore, designers are faced with more constraints such as high speed, high throughput, small silicon area

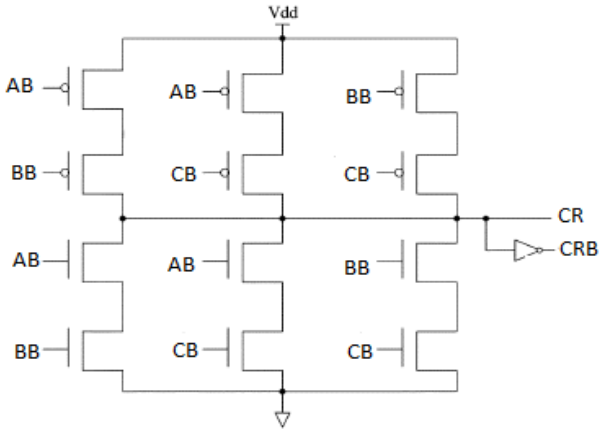
2. Level Restorer Full Adder

A level restore circuit used in MOS logic circuit design provides a voltage swing from a valid low to a valid high logic level in response to an input signal ranging from a degraded voltage high signal to a logic low signal. An input stage receives the degraded logic signal and provides separate gate drive signals to an inverter. An inverter in the intermediate stage receives the separate drive signals and provides an inverted signal output at a valid logic level.



(a)

The disadvantage of this implementation shows the resulting weak high output level in pass transistors used in the sum block of the proposed full adder. We used the feedback realized by the pull-up pMOS transistor [see Fig. 1(a)] in order to restore the weak logic "1" (i.e.,vdd->vtn) caused by the pass transistors, and provide sufficient drive to the successive stages. However, the level restoration implemented this way causes a voltage step at the output node "Sout" during a 0 ->1 transition, as shown in Fig1. This voltage step is due to the threshold voltage drop in the pass transistors and the delay needed by the level restorer to restore the weak logic "1" level.)



(b)

Fig. 1 level restorer full adder circuit

When the input is high passed through nmos network,the output node "y" charged to weak logic 1. When the voltage at node "y"<vdd/2 is , the pull-up pMOS energy is turned off, and the node "y" is charged with an effective drive current that equals the current of the nMOS network. When the voltage at node "y" approaches, the inverter reaches the switching threshold, the pull-up pMOS turns on, and the effective drive current charging the capacitance at node "y" becomes the sum of the current flowing through the nMOS network and the pull-up pMOS current.

3. Static Full Adder Circuit

In the static full adder the table of the full adder can be obtain in the fig of the static full adder,so that the *So* output is equal to the A exor B value when c=0, and it is equal to a exor bar,when c=1. Thus, a multiplexer can be used to obtain the respective value taking the _ input as the selection signal. Following the same criteria.

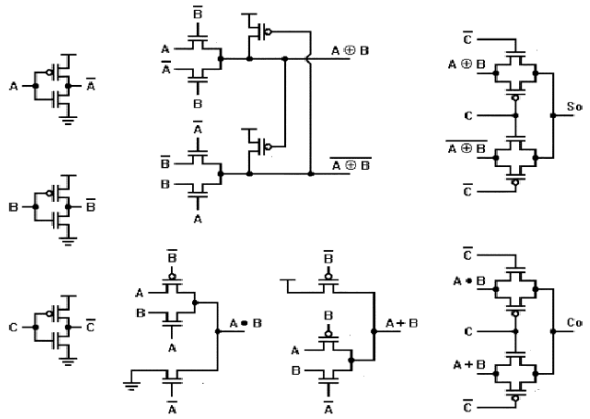


Fig.2 Hybrid full adder circuit

the *Co* output is equal to the A.B value when c=0, and it is equal to A+B value when c=1. Again, C can be used to select the respective value for the required condition, driving a multiplexer. Hence, an alternative logic scheme to design a full-adder cell can be formed by a logic block to obtain the A exor Band A exor B bar signals, another block to obtain the A.B and A+B signals.

The features and advantages of this logic structure are as follows.

• There are not signals generated internally that control the selection of the output multiplexers. Instead, the C input signal, exhibiting a full voltage swing and no extra delay, is used to drive the multiplexers, reducing so the overall propagation delays.

• The capacitive load for the C input has been reduced, as it is connected only to some transistor gates and no longer to some drain or source terminals, where the diffusion capacitance is becoming very large for sub-micrometer technologies. Thus, the overall delay for larger modules where the C signal falls on the critical path can be reduced.

• The propagation delay for the *So* and *Co* outputs can be tuned up individually by adjusting the XOR/XNOR and the AND/OR gates; this feature is advantageous for applications where the skew between arriving signals is critical for a proper operation, and for having well balanced propagation delays at the outputs to reduce the chance of glitches in cascaded applications.

• The inclusion of buffers at the full-adder outputs can be implemented by interchanging the XOR/XNOR signals, and the AND/OR gates to NAND/NORgates at the input of the multiplexers, improving in this way the performance for load-sensitive applications.

4.Proposed Full Adder Circuit

The Majority Function is a logic circuit that performs as a Majority vote to determine the output of the circuit.

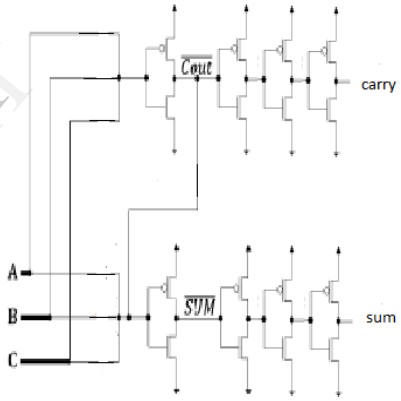


Fig. 3 proposed full adder circuit

This function has only odd numbers of input and its output is equal to ‘1’ when the number of inputs ‘1’ is more than ‘0’. the static CMOS inverter has been used as an inverter gate. Cadence simulation shows The proposed adder can work better with smaller capacitance values which can be made at higher technology such as 0.18micro meter technology it exhibits that the new full-adder cell will achieve more performance in the future with these small sizes. The best values of capacitance at 0.18 micro meter technology.Since the outputs of this adder are sumb and coutb as shown in fig 3. Inverters are attached to the circuit to make it comparable with the seven conventional full-adder cells. The addition of the

inverters is just for comparison. Indeed there are not any general differences in practical environment among the adder cells which produces sum and cout of their output.

5. Simulation And Result Analysis

The full adder circuits are designed and simulated in mentor graphics the results are compared in 0.18 micro meter technology

Table I comparison of full adder circuits

ADDER	TOTAL POWER	STATIC POWER	DYNAMIC POWER
Level restorer	250mW	247.1mW	2.9mW
Static full adder	180mW	175.4mW	4.6mW
Proposed full adder	90mW	87.3mW	2.7mW

Here in the table I shows the proposed full adder circuit

Consumed less power and as well as the number of the

Required transistors are also very less so power consumed is very less.

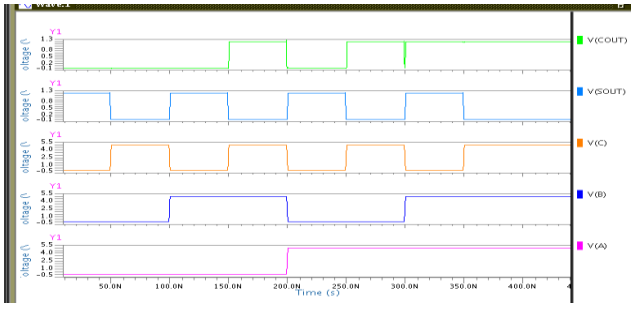


Fig.4 wave form for hybrid full adder

The above wave form as in the figure 4, show the result analysis of hybrid full adder circuit.

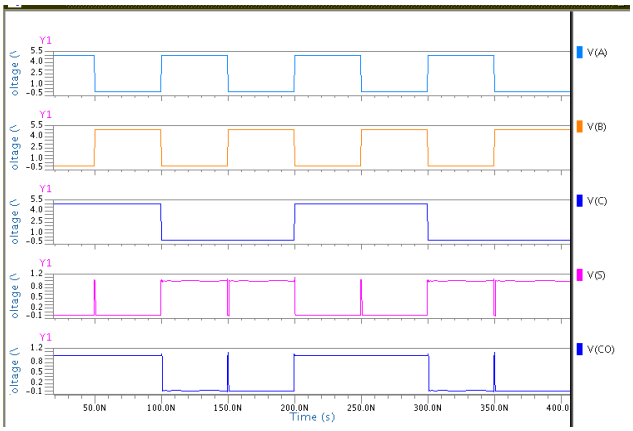


Fig.5 wave form for proposed full adder circuit.

The above fig 5 show the wave form for full adder circuit

6. Conclusion

The full adder circuits are designed and simulated in mentor graphics the results are compared in 0.18 micro meter technology. Here in the table I shows the proposed full adder circuit Consumed less power and as well as the number of the Required transistors are also very less so power consumed is very less. In the level restorer full adder it consumes 247.1mW of power in the circuit. whereas the hybrid full adder circuit consumes the 175.4mW of the power and proposed full adder circuit consumes 90mW of the power in the circuit and also required number of the transistors are also very less.

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