International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 3 Issue 10, October- 2014

A Digital CMOS Parallel Counter Architecture for Frequency Divider Based on Transmission Gate Logic

Anil Kumar Choudhary
(EC) (RGPV BHOPAL)RKDF
Institute of science and technology Bhopal MP India

K. Pitambar Patra
(EC) (RGPV BHOPAL)RKDF
Institute of science and technology Bhopal MP India

***Abstract*— VLSI fabrication technology is still in the process of evolution which is leading to smaller line widths and feature size and to higher packing density of circuitry on a chip. The scaling down of feature size generally leads to improved performance and it is important to understand the effect of scaling. The design of conventional frequency divider requires the large number of flip-flops. The propose counter design is base on CMOS base transmission gate logic to achieve higher operating frequencies, smaller delays and optimized area that can be used in program counter, frequency dividers use in digital integrated circuits.The proposed design is base on a pass transistor logic base counter, which counted through a fixed set of pre assigned count states, of which each next count state represents the next counter value in sequence.**

Keywords*— *Transmission gates ,Counter , Frequency divider

INTRODUCTION

Counters are widely considered as essential building blocks for a variety of circuit operations such as programmable frequency dividers, shifters, code generators, memory select management, and various arithmetic operations. Counters are design by connecting flip-flops in series or together to form a "divide-by-n" binary counter where "n" is the number of counter stages used and which is called the Modulus. The modulus or simply "MOD" of a counter is the number of output states the counter goes through before return back to initial state zero, i.e. one complete cycle. For example a counter with three flip-flops will count from 0 to eight different output states representing the decimal numbers 0 to 7 and is called a Modulo-8 or MOD-8 counter. Similarly a counter with four flip-flops will count from 0 to 15 and is therefore called a Modulo-16 counter and so on.
Figures of merit are-

- Minimum feature size
- Number of gates on one chip
- Power dissipation
- Maximum operational frequency
- Die size.
- Production cost.
- Delay

Many of these figures of merit can be improved by shrinking the dimensions of transistors, interconnections and the separation between features and by adjusting the doping levels and supply voltages. Accordingly, over the past decade, much effort has been directed toward the upgrading of process technology and the resultant scaling down of devices and feature size.

DESIGN COUNTER BLOCKS:

In synchronous counter all of the flip-flops change the state at the same time. The propagation delay of these counters depends on the indeterminate period of all of the flip-flops. whereas in the asynchronous counter, the delay of each flip-flop increases with the number of bits increases. The propagation delay of a 16 bit asynchronous counter is calculated as the combine delay of the 16 flip-flops. The total number of flip-flops require to design is base on the number of counting state, a large number of transistors in the design can be a significant source of static power dissipation. It can therefore be advantageous to keep the size of the transistor as small as possible. But the switching time of MOSFET is inversely proportional to Channel width W to channel length L ratioW/L , thus by reducing the size of the transistor, the delay is increased, then this can negatively affect the amount of energy consumed per cycle. Also the flip-flop device can be use as a frequency divider, i.e. it can divide the input clock frequency by 2 at the output.

IJERT

(This work is licensed under a Creative Commons Attribution 4.0 International License.)

Flip-flops are the basic building blocks of any counter circuit. In our design counter consist of a layout design of transmission gate base latch circuit connected in master slave arrangement to form the edge trigger flip-flop.

TRANSMISSION GATE BASE D LATCH:

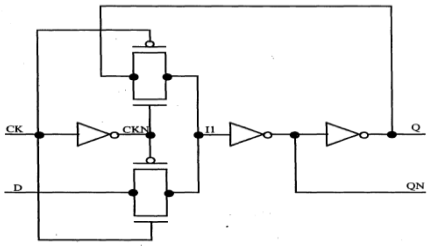

Fig.1 Transmission Gate Base D Latch

The circuit consists of a transmission gate based multiplexer and a series connected inverter. One additional inverter is used to generate the inverse of the clock input signal, required to control the transmission-gates (see fig1).The left-to-right dataflow through the latch when CLK=1 and the feedback loop when CLK=0**.** When the clock input is high, the current value from the data input (D) will propagate through the transmission gate and through the two inverters. The latch is transparent, and the output value Q follows the data input value, while the QN output generates the inverse of the data input value. When the clock signal changes to low (logical 0), the data transmission-gate is switched-off, while the feedback transmission-gate is activated and becomes conducting. As a result, the output value Q of the flip-flop will be fed back into the input of the first-stage inverter. Therefore, the latch stores whatever value it hold when the clock signal changed to low.

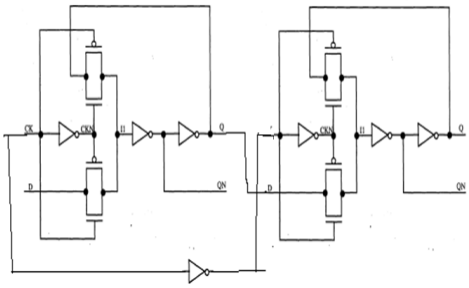

Fig 2 Transmission Gate Base D flip-flop

Here we can use negative edge trigger flip-flop. The negative edge is the edge where the clock signal changes from 1 to 0. Thus any change in input can affect the output on at this negative edge of clock signal. Flip-flops consist of two latches in series as in master slave arrangement controlled by inverted clock signals. During the high level of clock signal the master latch will turn on and slave latch will turn off. The first, called master, changes its state while Clock = 1. The second, called slave, changes its state while Clock = 0. The operation of the circuit is such that when the clock is high, the master tracks the value of the D input signal and the slave does not change. Thus the value of master output follows any changes in D, and the value of slave output remains constant.When the clock signal changes to 0, the master stage stops following the changes in the D input. At the same time, the slave stage responds to the value of the signal master output and changes state accordingly. At this clock phase master latch monitors the input and during the falling edge of clock the slave latch freezes. Thus while the slave latch copies the output of the master latch. It never experiences changes during these half periods as its input, the output of the first latch is frozen. This way changes only occur at the falling edge of the control signal, when the master latch freezes and the slave latch copies its output to the flip-flop's output.

Our design counter circuits can be built using T flip-flops because the toggle feature is naturally suited for the implementation of the counting operation. We can design this flip-fop by connecting the Qn output to the D input of Master slave D flip-flop shown in above figure. Fig shows four bit counter capable of counting from 0 to 15. The clock inputs of the four flip-flops are connected in cascade. The input of each flip-flop will be toggled at each negative edge of its clock. We are assuming that the purpose of this circuit is to count the number of pulses that occur on the primary input called Clock. Thus the clock input of the first flip-flop is connected to the Clock line. The other three flip-flops have their clock inputs driven by the Q output of the preceding flip-flop. Therefore, they toggle their state whenever the preceding flip-flop changes its state from Q = 1 to Q = 0, which results in a positive edge of the Q signal.

Layout simulations of transmission gate base latch, flip-flop, and four bit counter in microwind are conducted to compare the performances of our design. The power dissipation of master slave flip-flop calculate as 9µW at 1.2V power supply at maximum delay of 0.4ns.

BARREL SHIFTER:

A barrel shifter is a combinational circuit consist of multiplexer logic with n data input and n data outputs and a set of control inputs that specify how to shift data between input and output. It shifts in direction left or right. In this paper we use 4 bit barrel shifter design by using transmission gate base multiplexer cell. A barrel shifter is a digital circuit that can shift a data word by a specified number of bits in one clock cycle. It can be implemented as a sequence of multiplexers (mux.), and in such an implementation the output of one mux is connected to the input of the next mux in a way that depends on the shift distance.

(This work is licensed under a Creative Commons Attribution 4.0 International License.)

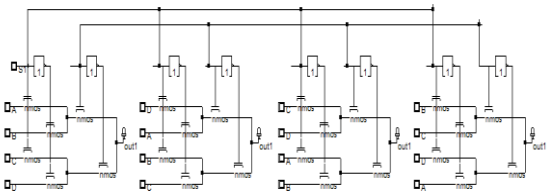

Fig Four Bit Barrel Shift Register.

For example, take a 4-bit barrel shifter, with inputs A, B, C and D. The shifter can cycle the order of the bits ABCD as DABC, CDAB, or BCDA; in this case, no bits are lost. That is, it can shift all of the outputs up to three positions to the right (and thus make any cyclic combination of A, B, C and D). The barrel shifter has a variety of applications, including being a useful component in microprocessors

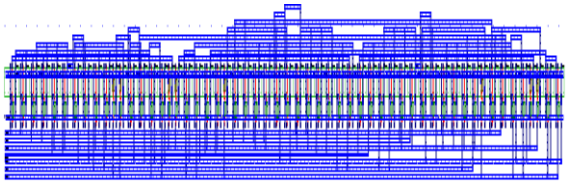

Fig. Layout Design of 4 Bit Barrel Shifter.

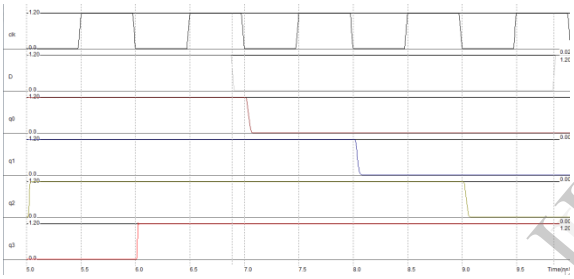

Fig.4 Timing Simulation of 4 Bit Data Shifter.

DIVIDE BY 2 FREQUENCY:

The most straightforward way to implement a divide-by-2 digital frequency divider is to use a toggle flip-flop (TFF). T-FF can be implemented using a D-FF feeding back the negative output Q to the input D. The input clock to be divided is then provided at the CLK input. Therefore, the core of the T-FF is a D-FF, and its maximum operating speed will set the maximum frequency that the T-FF can divide. Standard cells D-FF are usually implemented exploiting a positive feedback memory element, with the additional logic needed for clear, preset, and other functionalities that may be desired. A possible implementation for a T-FF is shown below.

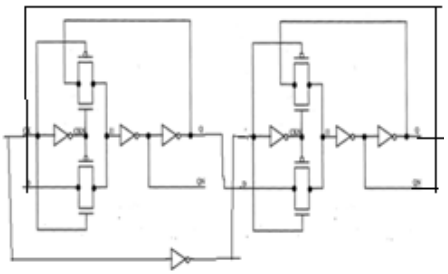

Fig.5 Divide by 2 Counter using D flip-flop

DIVIDE-BY-8 FREQUENCY DIVIDER:

The divide-by-8 frequency divider block is realized by a simply cascading 3 divide-by-2 blocks each consist of a T-FF. The
maximum frequency of operation for this block is the same as for the divide-by-2 block, since the input stage is the one operating at the highest frequency. The final layout of the divide-by-8 block is shown in Fig.

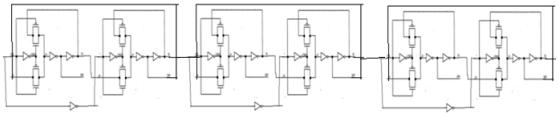

Fig.6Divide by 8 Counter using D flip-flop.

DIVIDE-BY-16 FREQUENCY DIVIDER:

The divide-by-16 frequency divider block is realized by a simply cascading 3 divide-by-2 blocks (each one of them being a T-FF). The maximum frequency of operation for this block is the same as for the divide-by-2 block, since the input stage is the one operating at the highest frequency.

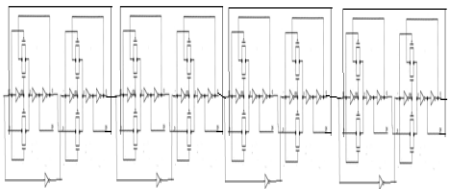

Fig.7Divide-by-8 Frequency Divider:

DIVIDE-BY-16 FREQUENCY DIVIDER:

Fig below shows Cascaded divide by 16 frequency Divider Thus for different divide by n frequency counter requires different flip-flop base circuits. Cascading n T-FF stages, it is possible to divide the input frequency by a factor of 2n. Therefore, the limitation of this approach is that the division ratio will be constrained to be a power of 2. But our propose lookahead a frequency divider digital CMOS parallel counter using pass transistor logic does not require to change the flip-flop base circuit.

IJERT

(This work is licensed under a Creative Commons Attribution 4.0 International License.)

LAYOUT OF TRANSMISSION GATE BASE D FLIP-FLOP:

The transmission gate base D flip-flop and its timing simulation is shown in fig. 10

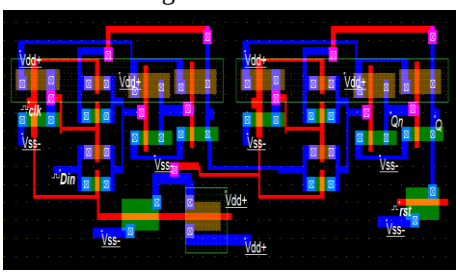

Fig.9 Transmission Gate base D Flip-flop

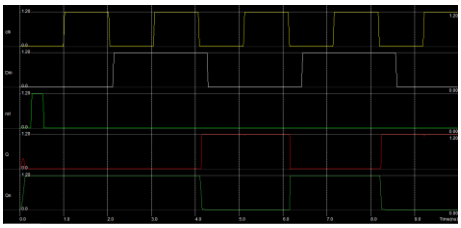

Fig.10 Timing Simulation of Transmission Gate base D Flip-flop

"Data in" is present at the **D** pin of a type **D** FF is transferred from D to output Q at clock time. Since our example shift register uses positive edge sensitive storage elements, the output **Q** follows the **D** input when the clock transitions from low to high as shown by the up arrows on the diagram above. It shows that the circuit can be behaves like a level trigger flip-flop.

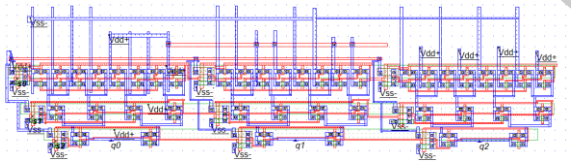

Fig.11 Layout Design For Transmission Gate Based 3 Bit Counter

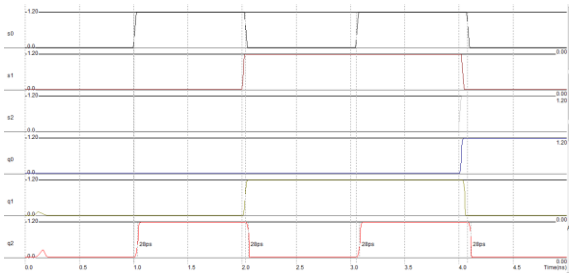

Fig.12 Timing Simulation of Transmission Gate Based 3 Bit Counter.

The back-end design of circuits is supported by MICROWIND 3 version. User can design digital circuits and compile here using Verilog file. MICROWIND automatically generates a error free CMOS layout. Although this place-route is not optimized enough as we do not include in complex place & route algorithms. User can also create CMOS layout of their own using compile one line Verilog syntax or custom build the layouts by manual drawing. The layout of 4 bit asynchronous counter is design by using four D register. A flip-flop is a synchronous version of the latch. To complicate the situation even more, there are several fundamental types of flip-flops. For a positive-edge triggered master–slave D flip-flop, when the clock signal is low (logical 0) the "enable" seen by the first or "master" D latch (the inverted clock signal) is high (logical 1). This allows the "master" latch to store the input value when the clock signal transitions from low to high. As the clock signal goes high (0 to 1) the inverted "enable" of the first latch goes low (1 to 0) and the value seen at the input to the master latch is "locked". Nearly simultaneously, the twice inverted "enable" of the second or "slave" D latch transitions from low to high (0 to 1) with the clock signal. This allows the signal captured at the rising edge of the clock by the now "locked" master latch to pass through the "slave" latch. When the clock signal returns to low (1 to 0), the output of the "slave" latch is "locked", and the value seen at the last rising edge of the clock is held while the "master" latch begins to accept new values in preparation for the next rising clock edge.

This thesis concludes that 4 bit asynchronous counter is best implemented using the 0.12micron technology. In this the required switching delay is minimum i.e. 90ps, power consumption is 2.087mwatt, Max operating frequency is 1.4 GHz, layout size area is 440.6 micro sq. meter. Thus that 4 bit asynchronous counter is best implemented using the 0.12micron technology is preferable over 0.6 micron technologies in maintaining the logic density in fabrication process, power optimization, reducing the propagation delay & surface area. Thus this counter implemented in CMOS chip technology, is the best illustration of VLSI.

Table 1- Comparison of 4 Bit Asynchronous Binary Counter

References	Ref [1,2]	Our design
Power	13.89mW	0.265mW to 0.304Mw
No. of transistor	510	379
Remarks	Large area	1. No biasing 2. Counter size fixed 3. Less no. of Transistor

CONCLUSION:

The 4 bit asynchronous counter has been designed with microwind. The microwind program allows the designer to design and simulate an integrated circuit at physical description level the physical (mask layout) design of cmos logic gates is an iterative process which starts with the circuit topology (to realize the desired logic function) and the initial sizing of the transistors (to realize the desired performance specifications). In this paper we design a frequency divider counter design using pass transistor logic circuit technique.

IJERT

(This work is licensed under a Creative Commons Attribution 4.0 International License.)

The proposed counter is a 4 bit pass transistor base counter, which sequences through a fixed set of pre assigned count states, of which each next count state represents the next counter value in sequence. The counter frequency is greatly improved by reducing the gate count on all timing paths to two gates using pass transistor circuit design techniques. In our work the counter operating frequency is improved by using a parallel counter architecture of pass transistor base flip-flops. This is proceeded to eliminate the carry chain delay and reduce AND gate fan-in and fan-out. The proposed counter is design for low-power and high-speed applications.

ACKNOWLEDGMENT

The work is supported by the Department of Electronics and Communication Engineering, RKDF Institute of Science and Technology Bhopal Madhya Pradesh India.

REFERENCES:

[1]. Saleh Abdel-Hafeez, and Ann Gordon-Ross "A Digital CMOS Parallel Counter Architecture Based on State Look-Ahead Logic" IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 19, No. 6,

[2]. Saleh Abdel-Hafeez · Ann Gordon-Ross "A Gigahertz Digital CMOS Divide-by-N Frequency Divider Based on a State Look-Ahead Structure" Springer Science Business Media, 2 June 2010 / Revised: 3 February 2011.

[3]. Vijaya Bhaskar M, Suparshya Babu Sukhavasi, Susrutha Babu Sukhavasi, G Santhi Swaroop Vemana "Implementation Of Synchronous Up Counter By Using Self Resetting Logic" International Journal of Engineering Research and Applications (IJERA) Vol. 2, Issue 1,Jan-Feb 2012, pp.972-981

[4]. Totok Mujiono "Design Of High Frequency Cmos Fractional-N Frequency Divider" Design Of High Frequency Cmos Fractional-N Frequency Divider" JAVA Journal of Electrical and Electronics Engineering, Vol. 1, No. 1, April 2003 pp. no. 12.

IJERT

(This work is licensed under a Creative Commons Attribution 4.0 International License.)