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A High Speed Parallel Counter Based on Gate Logic Components

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***Abstract*—An 8-bit parallel counter architecture is presented. This architecture includes a counting path and state look-ahead path. The counting path consists of three basic module types and these counting modules are partitioned into 2-bit counter separated by pipelined DFF latches. The state look ahead path anticipates future states and thus prepares the counting path for these future states. The paper also deals with counting section and state anticipation module. The counting section includes three different modules and each module using JK flip-flops. The first and third modules are three bit counting module and second module is a two bit counting module. The 8-bit parallel counter architecture consumes a total equivalent gate count of 266 whereas the same using proposed counter architecture consumes only 164. The delay of the 8-bit parallel counter and proposed counter was found to be 4.952ns and 3.968ns respectively.**

***Keywords*—Counter,parallel counter design, architecture design, pipeline counter design, state anticipation module.**

I. INTRODUCTION

COUNTER is a key element in most of the variety of circuit operations such as frequency dividers, shifters, code generators and various arithmetic operations. Counter architecture design methodologies explore tradeoffs between gate count, delay, power consumption, area requirements and target application specialization.

As the speed of operation is determined by the propagation delay time of the count enable signal from the LSB to the MSB, most of the conventional frequency dividers and counters cannot satisfy the speed requirements. Therefore, the counter's size is considered to be the main limiting factor of the counting rate [I]. Some traditional approaches enhanced the counting speed by improving the circuit implementation of various gates and flip-flops, [2], [3], [4]. But these techniques are not well suited for counters employed in arithmetic circuits. In order to reduce high counter power consumption, Alioto *et al.* [5] presented a low power counter design with a relatively high operating frequency. Alioto's design was based on cascading an analog block such that each counting stage's input frequency was halved compared to the previous counting stage. However, Alioto's counter design's carry chain rippled through all counting stages, resulting in a total critical path delay equal to the sum of all counting stage Alioto's design was not well suited for large counter widths because the carry chain limited operating frequency. Kakarountas *et al.* [6] used a carry look-ahead circuit [7] to replace the carry chain. The carry look-ahead circuit used a prescaler technique with systolic 4-bit counter modules used TFFS, with the cost of an extra detector circuit. The detector circuit detected the assertion of lower order bits to enable counting in the higher order bits. To further improve operating frequency, Kakarountas's design used DFFs be-tween systolic counter modules. However, since the counter design was limited by control signal broadcasting, Kakarountas's design was not practical for large counter widths. To [8] improved counter operating frequency by partitioning large counters into multiple smaller counting modules, such that modules of higher significance were enabled when all bits in all modules of lower significance saturate. Initializations and propagation delays such as AND logic chain decoding and the half incrementer component delays in half adders dictated operating frequency. Further improved counter operating frequency using half adders in the parallel counting modules [9], [10] that enabled carry signals generated at counting modules of lower significance to higher significance. The carry chain cascaded synchronously through intermediate D-type flip-flops. The maximum operating frequency was limited by the half adder module delay, DFF access time, and the detector logic delay. Since the module outputs did not directly represent count state, the detector logic further decoded the module outputs to the output count state value.

The 8-bit Parallel counter architecture [11] consists of four 2-bit modules separated by DFFs. The performance of the counter was found to be attractive, it consumed comparatively higher number of gate count thereby increasing total area required for the circuit realization. Therefore to negate these drawbacks alternative counter design strategies are proposed here. In the proposed counter architecture all the counting blocks are designed by using JK flip-flops which reduces the number of gates required for the overall implementation of the circuit. Also in place for repeating counting blocks of equal width, the counting blocks of variable width is used to reduce the size of the state anticipation module. The remainder of this paper is organized as follows. Section II discusses 8-bit

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parallel counter architecture. Section III discusses about proposed parallel counter architecture. Section IV presents simulation and synthesis results for parallel and proposed counter and finally the conclusion is given in Section V.

II. Parallel Counter Architecture

Fig. 1 shows the functional block diagram of the 8-bit parallel counter architecture. It consists of the state look-ahead path and the counting path. The counter is partitioned into uniform 2-bit synchronous up counting modules. Next state transitions in counting modules of higher significance are enabled on the clock cycle preceding the state transition using stimulus from the state look-ahead path. Therefore, all counting modules concurrently transition to their next states at the rising clock edge. The counting path controls counting operations and the state look-ahead path anticipates future states and thus prepares the counting path for these future states. There are three module types, module-1, module-2, and module-3 S, where S=1, 2, 3, etc. and represents the position of module-3 used to construct both paths.

1) Counting Path: Fig. 2 shows the hardware schematic of Module-1. It is a parallel synchronous binary 2-bit counter, which is responsible for low-order bit counting and generating future states for all module-3 S's in the counting path by pipelining the enable for these future states through the state look-ahead path. Module-1 and module-3 are exclusive to the counting path and each module represents two counter bits. In the counting path, each module-3 is preceded by an associated module-2. The output of module-1 is Q1Q0 and QEN1 connects to the module-2's DIN input.

Module-2 is a conventional positive edge triggered DFF and is present in both paths. In the counting path, it act as a pipeline between the module-1 and module-3 1 and subsequent module-3S. In state look-ahead logic module -2 placement increases counter operating frequency by eliminating the lengthy AND-gate rippling and large AND gate fan-in and fan-out present in large width parallel counters. Instead of the modules of higher significance are enabled by the module-3S and state look-ahead logic. Then the coupling of module-2 with module-3 1introduces an extra cycle delay before module-3 1 is enabled. Thus the module-2s in the counting path provide a 1-cycle look-ahead mechanism for triggering the module-3S's, and enabling the module-2s to maintain a constant delay for all stages.

Module-3S's serve two main purposes. Their first purpose is to generate all counter bits associated with their ordered position and the second purpose is to enable future states in module-3S's in conjunction with stimulus from the state look-ahead path. Fig. 3 shows the hardware schematic of module-3S. It is a parallel binary 2-bit counter whose count is enabled by INS. INS connects to the Q output of the preceding module-2. It also provides one-cycle look ahead mechanism.

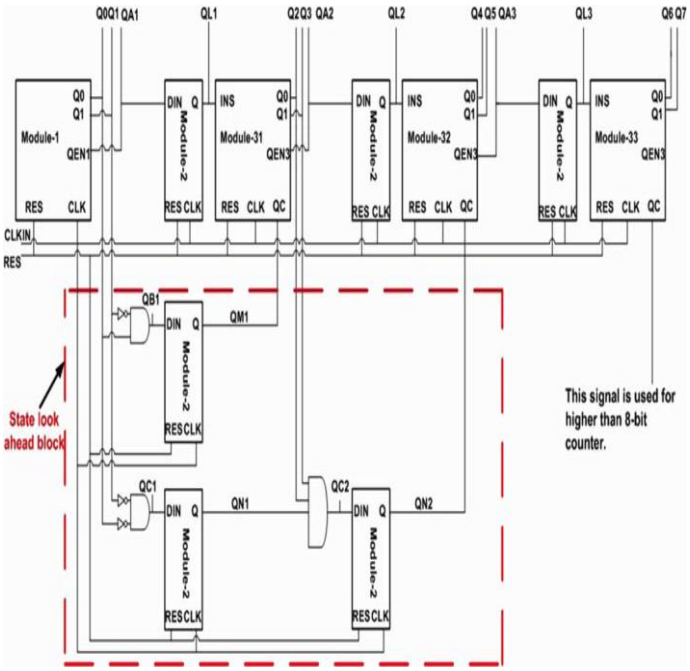

Fig. 1 Block diagram of 8-bit parallel counter

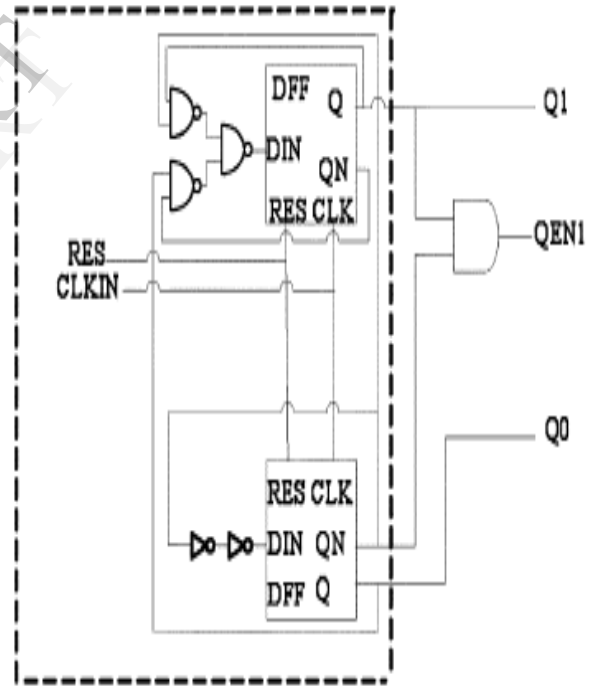

Fig.2 Hardware schematic of module-1

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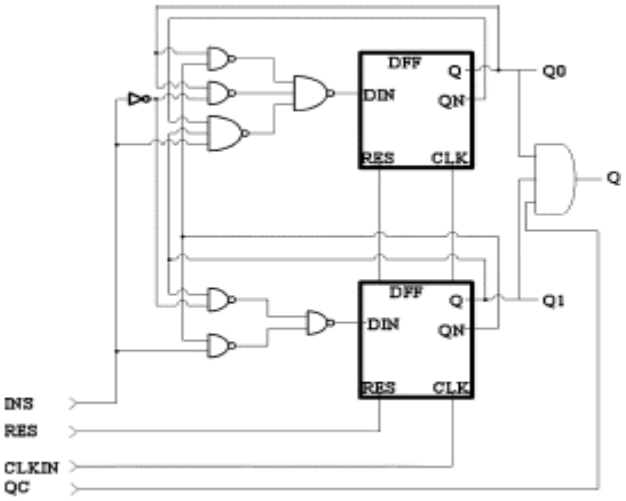

Fig. 3 Hardware schematic of module-3S

2) State Look-Ahead Path: The state look-ahead logic operation avoids the use of an overhead delay detector circuit that decodes the low order modules to generate the enable signals for higher order modules, and enables all modules to be triggered concurrently on the clock edge, thus avoiding delay and rippling. The state look-ahead logic is principally equivalent to the one-cycle look-ahead mechanism in the counting path. To enabling the next state's high order bits depends on early overflow pipelining across clock cycles through the module-2S in the state look-ahead path.

Fig. 4 shows a generalized counter topology for an N-bit counter state look-ahead path details. Module-2s in the state look-ahead logic are responsible for propagating the early overflow detection to the appropriate module-3S. Early overflow is initiated by the module-1 through the left-most column of decoders state-2, state-3, etc. Each module-2S early overflow pipelining chain is preceded by a small logic block state-X, where X denotes the number of clock cycles that the early overflow pipelining must carry through. Each State-X block consists of simple two input AND logic that decodes the module-1's output. Fig. 1. shows the internal logic for State-2 and State-3 respectively, and whose outputs QB1 and QC1 are connected to the module-2s DIN input, thus starting the early overflow pipelining exactly X clock cycles before the overflow must be detected to enable counting in a module-3S.

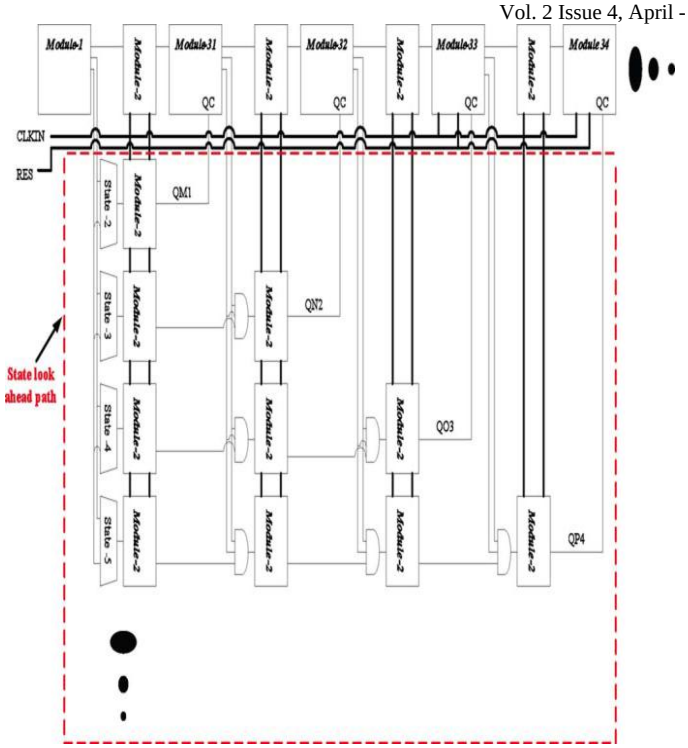

Fig. 4 Generalized N-bit counter showing state look-ahead path details

III. PROPOSED PARALLEL COUNTER ARCHITECTURE

The proposed high speed parallel counter consists of two sections- counting section and state anticipation module. The counting section consists of three different modules. They are BCM, SCM1, and SCM2. The module BCM represents the Basic Counting Module. SCM1 and SCM2 represent the first and second Subsequent Counting Modules respectively.

The basic module *BCM* is a parallel synchronous 3-bit up counter using JK flip-flops. The module *BCM* is responsible for the three low-order bit counting and these three LSBs generate future states for counting modules SCM1 and SCM2 in the counting section. SCM1 is a two bit counting module and SCM2 is a three bit counting module. Similar to module BCM, JK flip-flops are used to realize the circuits of modules SCM1 and SCM2.

The State Anticipation Module(SAM) consists of three D flip-flops, three 3-input AND gates and two inverters. It decodes the count states of basic counting module BCM. This decoding is carried over two clock cycles through two DFFs to trigger the second subsequent module, SCM2.

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IV. RESULTS

1) *Simulation Results*

The performance analysis of the 8-bit parallel counter architecture is analyzed and it is simulated using ModelSim simulator in Fig. 5. Also proposed 8-bit parallel counter is analyzed as shown in Fig. 6.

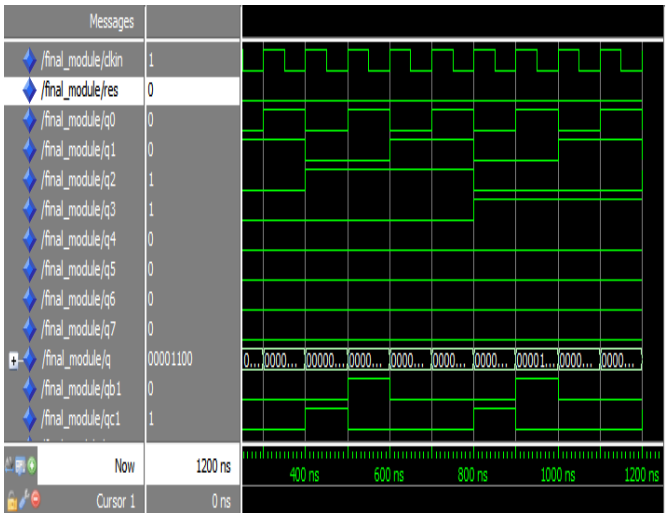

Fig. 5 Measured waveforms of 8-bit parallel counter using Modelsim

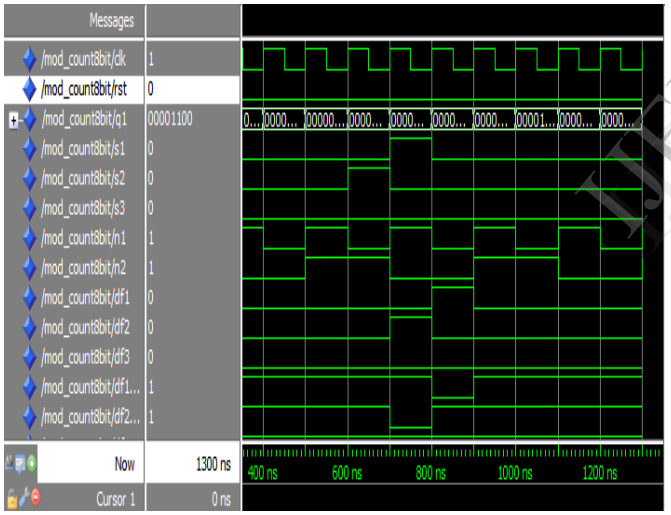

Fig. 6 Measured waveforms of proposed parallel counter using Modelsim

2) *Synthesis Results*

Using Xilinx ISE 8.1i synthesis is done and analyzed which is shown in Fig. 7. The synthesis report shows the number of flip-flops and IOBs (input-output blocks) used is very less. Also gives the parameters enhanced like power dissipation, delay and gate count for design.

Logic Distribution			
Number of occupied Slices	13	1,200	1%
Number of Slices containing only related logic	13	13	100%
Number of Slices containing unrelated logic	0	13	0%
Total Number of 4 input LUTs	26	2,400	1%
Number of bonded IOBs	9	92	9%
Number of GCLKs	1	4	25%
Number of GCLKIOBs	1	4	25%
Total equivalent gate count for design	266		
Additional JTAG gate count for IOBs	480		

Fig. 7 Synthesis report of 8-bit parallel counter

Logic Distribution			
Number of occupied Slices	8	1,200	1%
Number of Slices containing only related logic	8	8	100%
Number of Slices containing unrelated logic	0	8	0%
Total Number of 4 input LUTs	10	2,400	1%
Number of bonded IOBs	9	92	9%
IOB Flip Flops	1		
Number of GCLKs	1	4	25%
Number of GCLKIOBs	1	4	25%
Total equivalent gate count for design	164		
Additional JTAG gate count for IOBs	480		

Fig. 8 Synthesis report of proposed parallel counter

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3) Comparison Results

TABLE I
COMPARISON OF 8-BIT COUNTER, PARALLEL COUNTER, PROPOSED COUNTER

Parameter	Power(mW)	Delay(ns)	Gate count
8-bit normal counter	14	6.033	368
8-bit parallel counter	12	4.952	266
8-bit proposed parallel counter	9	3.968	164

V. CONCLUSIONS

A high speed parallel counter using digital CMOS gate logic components is presented. An 8-bit parallel counter is comprised of only 2-bit counting modules and three input AND gates. The main structures are a counting path and a state look ahead path which activates all modules concurrently at the system's clock edge and also avoids using a long chain detector circuit required for large counter widths. The paper also presented an 8-bit proposed parallel counter architecture. The AND gate rippling results in reduction in speed in parallel counters has been eliminated by the proposed counter methodology. The tabulated results demonstrate the better performance of the proposed counter in terms of delay and gate count compared to parallel counter. This suggests its suitability for high speed arithmetic applications. The 8-bit parallel counter architecture consumes a total equivalent gate count of 266 whereas the same using proposed counter architecture consumes only 164. The delay of the 8-bit parallel counter and proposed counter was found to be 4.952ns and 3.968ns respectively.

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