

A Low Power Digitally Controlled Oscillator Using 0.18 μ m Technology

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ABSTRACT

This paper presents a low-power digitally controlled oscillator (DCO). The coarse-fine architecture with binary-weighted delay stages is applied for the delay range and resolution optimization. The coarse-tuning stage of the DCO uses the interlaced hysteresis delay cell, which is power and area efficient, as compared with conventional delay cells. The glitch protection synchronous circuit makes the DCO easily controllable without generating glitches. All-digital phase-locked loop using the DCO is fabricated in a 180-nm CMOS process. The measured output frequency range is 60–420 MHz at the supply of 1.8V.

Keywords—All-digital phase-locked loop (ADPLL), digitally controlled oscillator (DCO), interlaced hysteresis delay cell (IHDC), low power.

I. INTRODUCTION

ALL-DIGITAL phase-locked loops (ADPLLs) have been widely used in integrated circuits for clock generation. The basic architecture of the ADPLL is composed of a digitally controlled oscillator (DCO), a frequency divider (DIV), a phase frequency detector (PFD), and a controller (CTRL), as shown in Fig. 1. Benefiting from the digital implementation, the functional blocks are easily manipulated with well-defined digital values. As process technology scales down, the delay timing, area, and power consumption of the functional blocks are substantially reduced. Therefore, the ADPLL acquires overall performance improvements in a nanometer CMOS technology.

The DCO, which dominates the ADPLL performance, tends to generate high-frequency output with fine-resolution delay units as process technology scales down. However, in applications operating at a middle-to-low or wide frequency range, the total delay time of the delay units in the DCO may not cover a large period. A straightforward approach of extending the period is to add more delay units, which

results in significant area and leakage current. An alternative approach of dividing the frequency output from the high-frequency source is area efficient but restricted in the adjustable resolution. Accordingly, the coarse-fine DCO architectures are commonly adopted to satisfy the frequency range and resolution requirements.

With the coarse-fine DCO architecture, large coarse-tuning delay units can effectively extend the period range. The cascaded hysteresis delay cells (CHDC) are proposed for a huge delay of the single coarse-tuning unit with extremely low power consumption in a small area. Compared with conventional buffer or logic gate approaches, the power and area are greatly reduced in the coarse-tuning stage. However, the process, voltage, and temperature (PVT) variations of the CHDC delay is high due to some weak driven internal nodes. The fine-tuning stage must cover a wider range to ensure a continuous period change and hence consumes more power and area.

In this brief, a DCO using the interlaced hysteresis delay cells (IHDCs) is proposed to achieve a large delay and low power in a small area. The IHDC interlaces the signal transitions in two series of cascaded transistors. It prevents the short-circuit current and saves the leakage current in the shared current path. All the internal nodes are rail-to-rail driven to avoid high PVT variations. Also, the glitch protection circuit using a control code resampling synchronous cells is applied for better control of the DCO. This DCO is implemented with a simple demonstrative ADPLL, which generates the output clock from 60 to 420 MHz

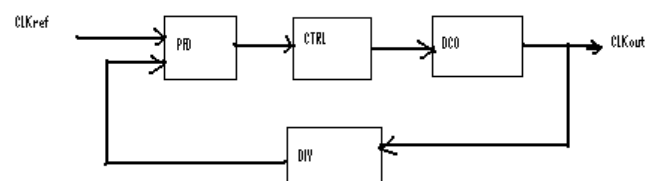


Fig. 1. Block diagram of an ADPLL.

II. PROPOSED DCO AND IHDCS

A. Architecture of the Proposed DCO

Fig. 2 shows the block diagram of the proposed DCO. The DCO applies the coarse–fine architecture with the 11-bit period

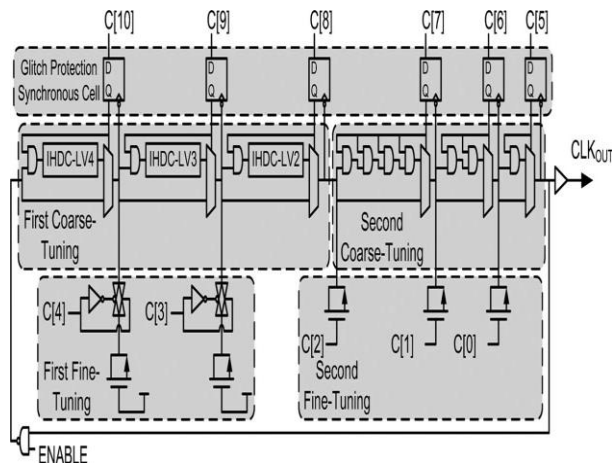


Fig. 2. Architecture of the proposed DCO.

B. Coarse-tuning stages

The coarse-tuning stages are arranged as delay-selective paths, and each bit of the six segments, i.e., C[10]–C[5], decides which path is taken. The first coarse-tuning stage is composed of three segments. The main delay units in the segments are implemented using IHDC delay cells of different levels (IHDC-LV4, IHDC-LV3, and IHDC-LV2), which cover most of the operating period range. The IHDC can provide a larger delay with lower power consumption and smaller area occupation, as compared with conventional delay cells. The detailed cell architecture will be explained in the next discussion. The second coarse-tuning stage selects the path from zero delay to seven AND gates delay by the combinations of four, two, and one AND gates.

C. Fine-tuning stages

The fine-tuning stages are mainly composed of digitally controlled varactors (DCVs) and attached on the delay path of the coarse-tuning stages. For a fine-tuning code selection, the equivalent load on the delay path can be slightly changed and delay the clock signal transition in a picosecond resolution. The binary-weighted delay is designed for all the bits so that the period control code

can be directly applied to the path selection and the DCV without a decoder. In addition, the unselected delay paths are gated by the AND gates to save power consumption.

D. The glitch protection circuit

The glitch protection circuit is designed to update the coarse-tuning code synchronously to the DCO clock signal. The clock signal passes each segment before updating the input code. Thus, the temporal instable signals in the segments are eliminated.

E. IHDC

Fig. 3(a) shows the IHDC-LV2 circuit configuration. Two series of cascaded pMOS and nMOS, i.e., M1–M8, are the main delay elements. M9–M12 are for some floating-node charges/discharges. The nodes with the same name, e.g., *a*, *b*, *c*, *d*, and *e*, are connected without drawing the lines. The operating timing diagram is illustrated in Fig. 3(b). Assuming *IN* is initially high and goes low, M1 is then turned on, and *a* goes high. M8 is subsequently turned on, which is followed by *b* going low. After that, M2 is turned on, which is followed by *c* going high. *c* turns on M7 and discharges *OUT* to ground. In summary, the falling transition of the *IN* signal propagates through M1, M8, M2, and M7 to *OUT*. Similarly, the rising transition of the *IN* signal propagates through M4, M5, M3 and M6 to *OUT*. The delay path is interlaced between these two series of cascaded transistors. Although the other four transistors, i.e., M9–M12, do not contribute the delay time, those transistors connect the temporal floating nodes to a stable state. When *IN* goes from high to low, M4 is immediately turned off. Meanwhile, a weak low voltage will be sustained in node *e*. With the connection of M9, *e* will be subsequently charged to high. Similarly, M10, M11, and M12 keep the nodes *a*, *b*, and *d* to a stable state, respectively.

During the signal transition in this structure, the short-circuit path does not exist since pMOS and nMOS are turned on and off one by one in different paths. In particular, the short-circuit current dominates the power consumption in the inverter based delay cells with the input signal of a long transition time. Therefore, the total power is largely reduced, as compared with conventional delay cells. In addition, only two current paths are connected between the supply and the ground. The charge is shared by the transistors on the same path. Therefore, the leakage charge is saved by the amount that is proportional to the number of the transistors cascaded in the path. With this kind of interlaced signal pass, the transistor number in a path can be extended to enable more shared charges and a larger

delay. Fig. 4(a) and (b) shows the IHDC-LV3 and the IHDC-LV4, respectively.

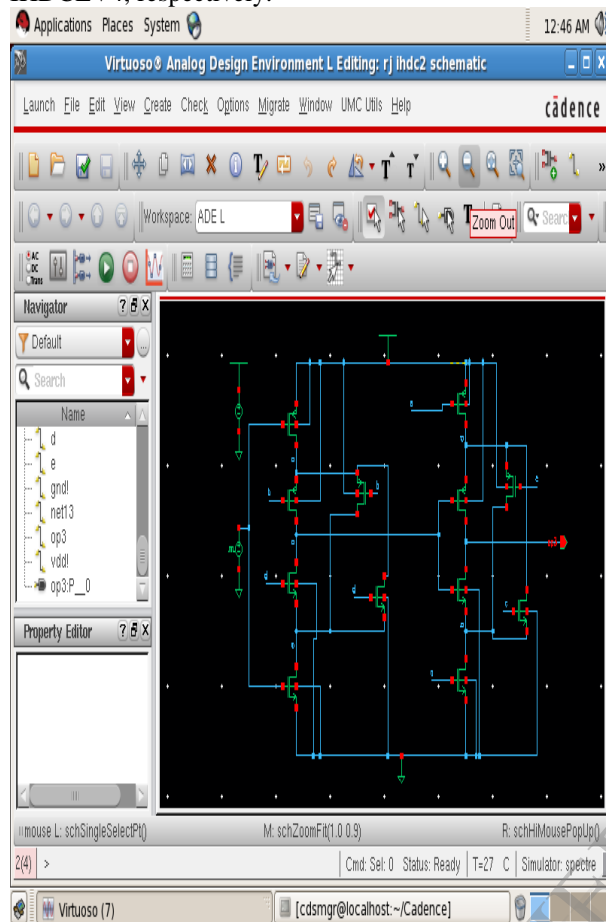


Fig. 3(a) shows the IHDC-LV2 circuit configuration

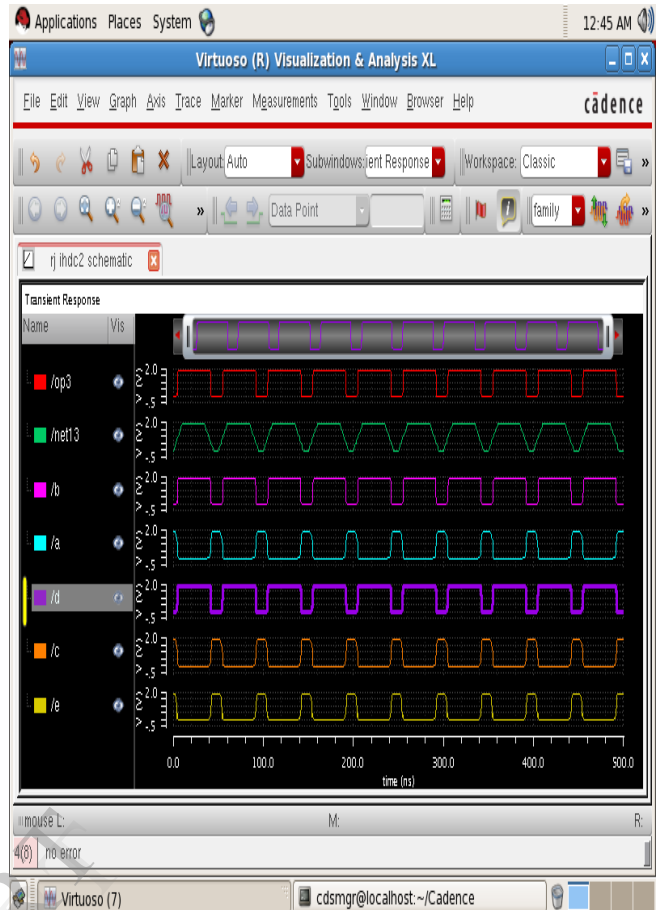


Fig. 3(b).Output Waveform of the IHDC-LV2

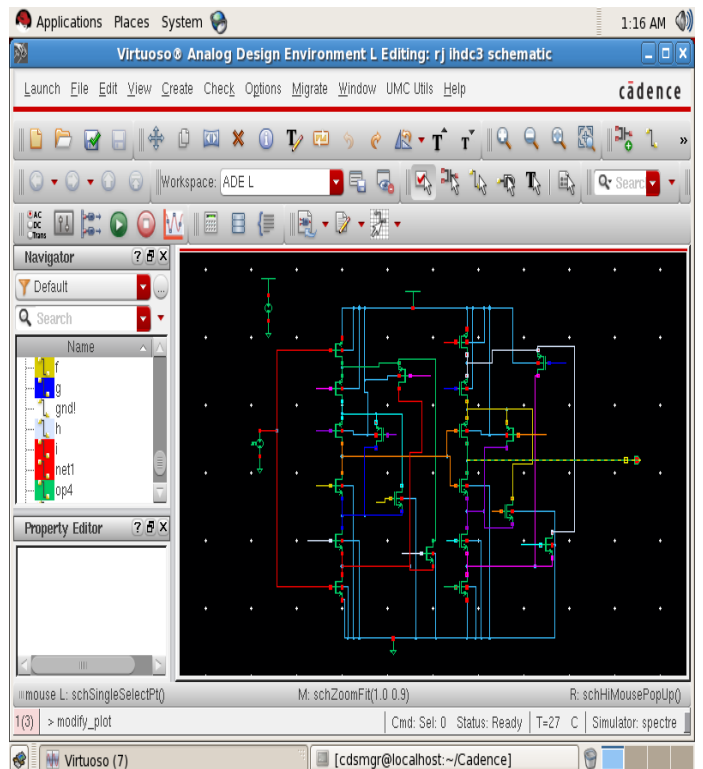


Fig. 4(a) shows the IHDC-LV3 circuit configuration

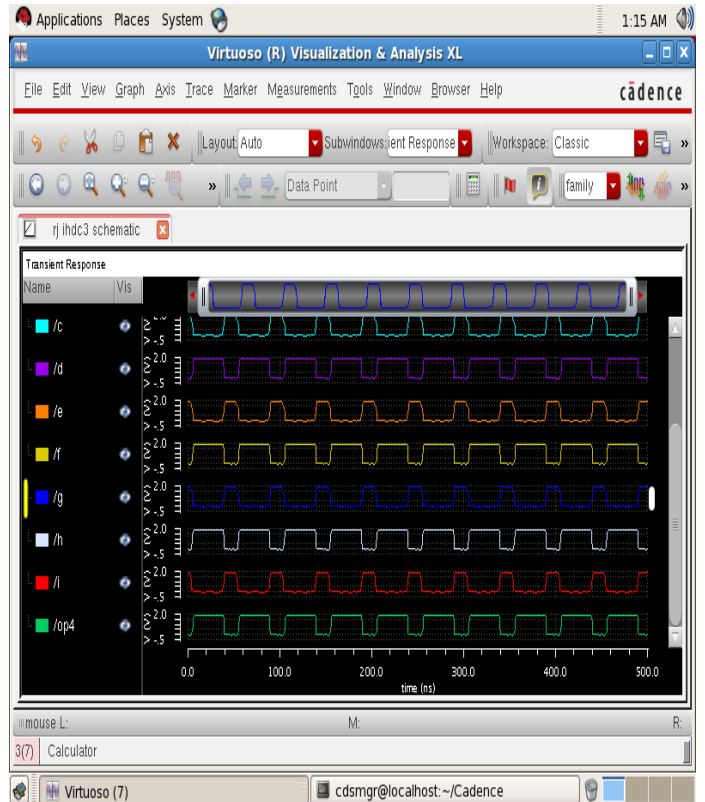
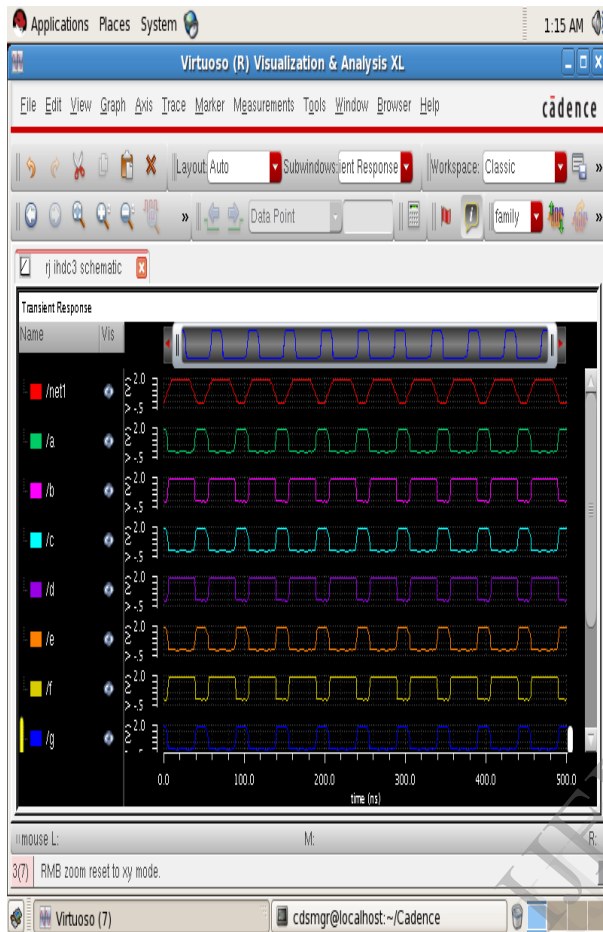


Fig. Output Waveforms of the IHDC-LV3

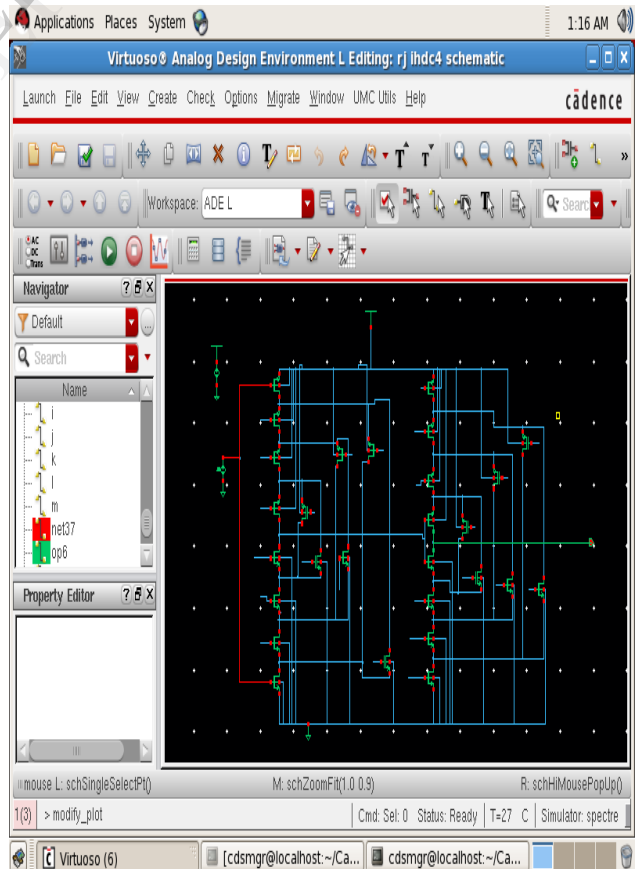


Fig. 4(b) shows the IHDC-LV4 circuit configuration

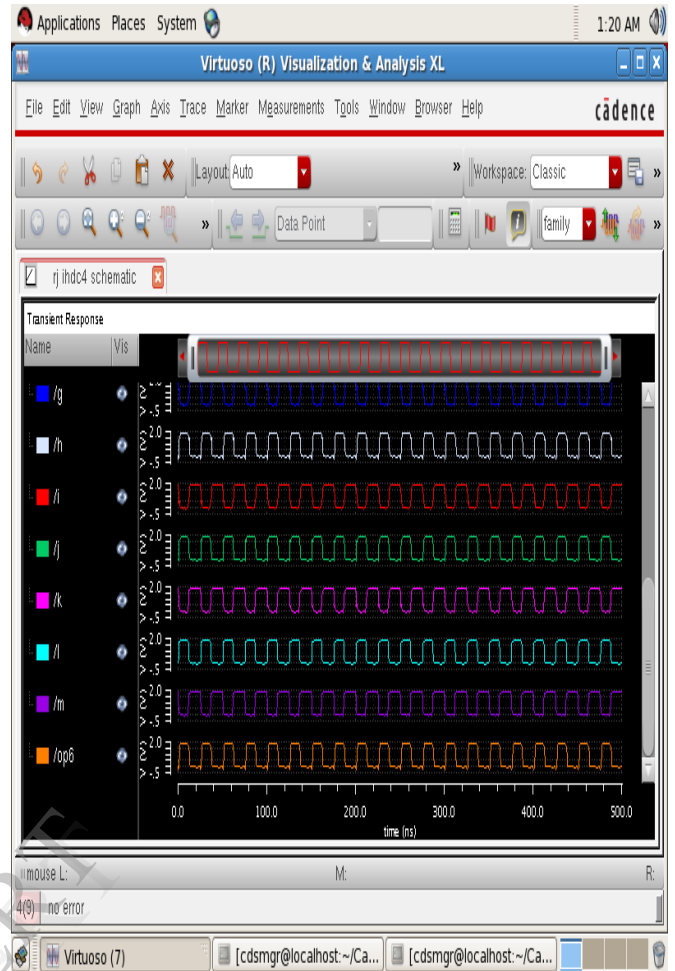
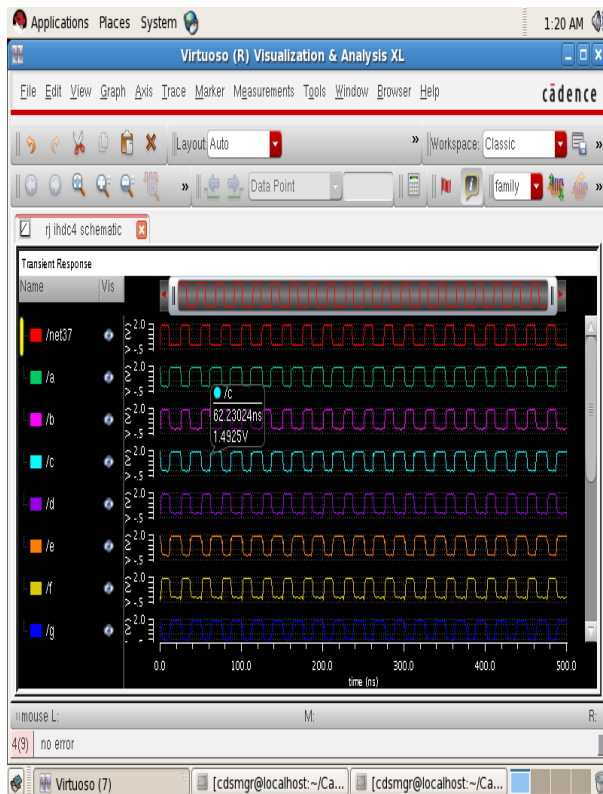


Fig. Output Waveform (1) of the IHDC-LV4

Fig. Output Waveform (2) of the IHDC-LV4

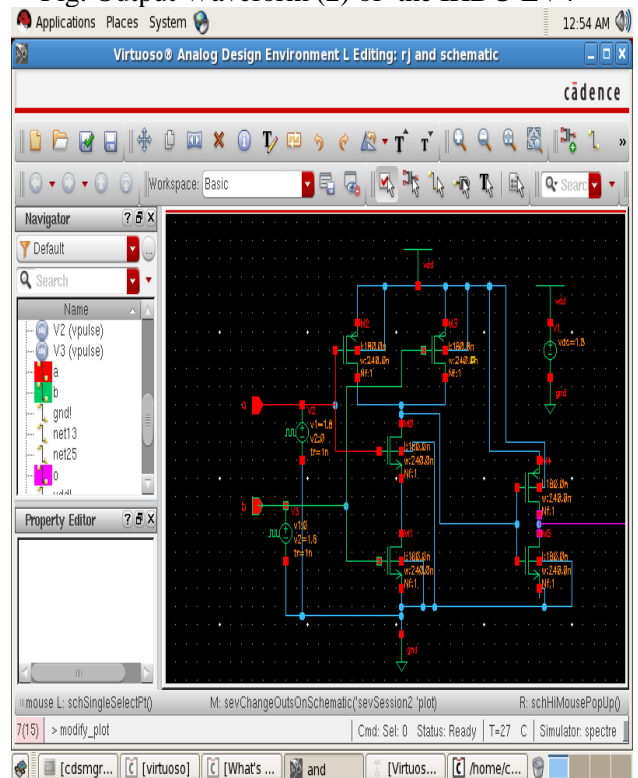


Fig. 5 shows the AND circuit configuration

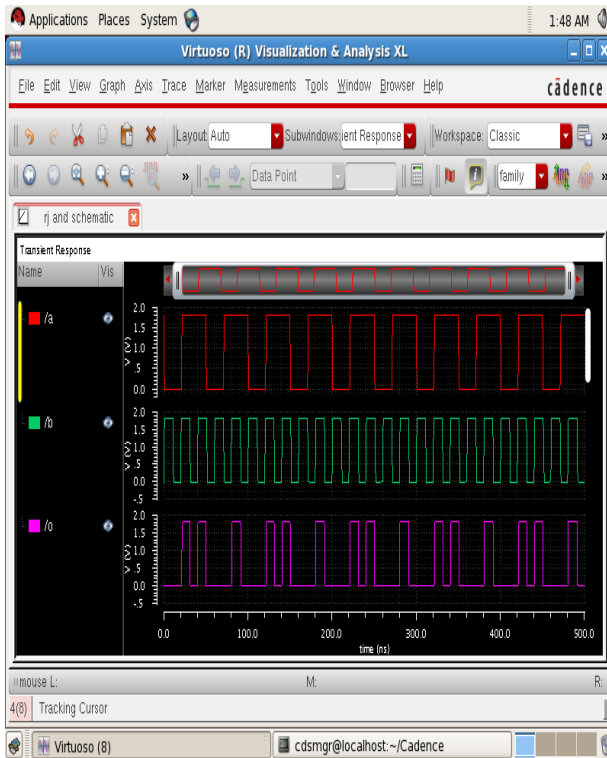


Fig. Output Waveform of the AND circuit

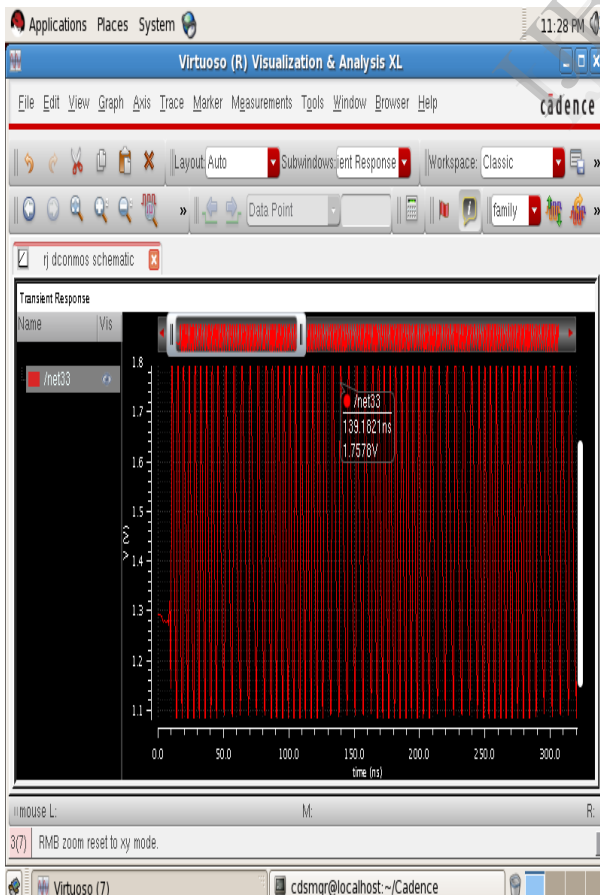


Fig. Output Waveform of the proposed DCO circuit

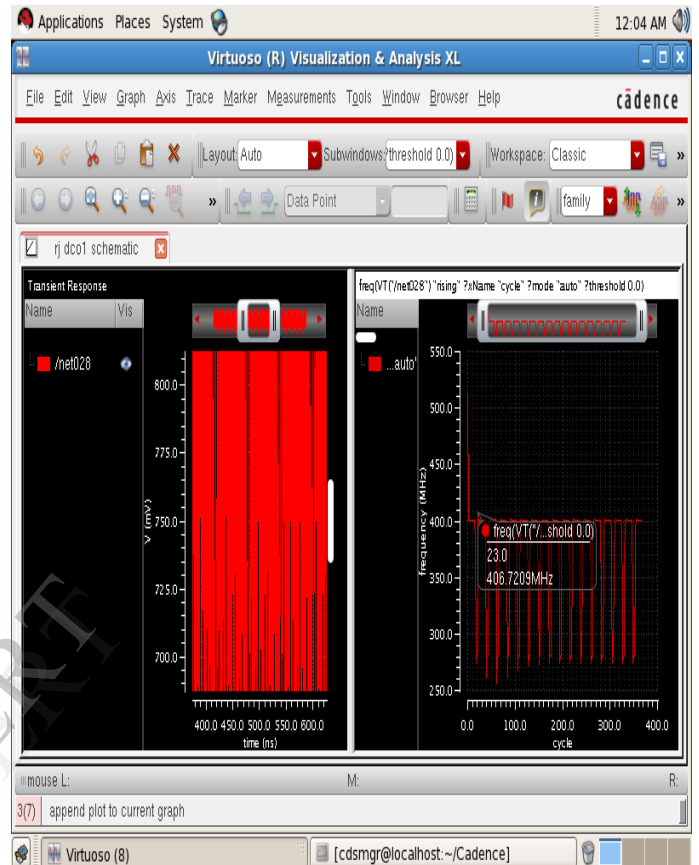


Fig. Frequency response of proposed DCO

III. CONCLUSION

A low-power and area-efficient DCO has been presented in this paper. The proposed IHDC is applied to replace the conventional delay cells for power and area reduction. The binary weighted stages with the coarse-fine architecture are designed with the glitch protection synchronous cells. The demonstrative ADPLL is implemented in a 180-nm CMOS technology using Cadence tool.

IV. ACKNOWLEDGEMENT

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V. REFERENCES

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