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A Low to High Voltage Tolerant Level Shifter for Low Voltage Applications

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***Abstract* – Efforts are underway to develop CMOS integrated circuits that operate at supply voltages well under 0.5V. For a variety of reasons it is often desirable to interface these low voltage devices to conventional electronics operating with nominal supply voltages of 5 V or 3.3 V. In this proposed work, a new construction of level shifter for low power application has been presented. Circuits have been simulated in Spice with TSMC 0.05 process technology. Output level of 1.2V has been obtained with input pulse of 0.8V. In view of power and delay, the new proposed level shifter outperforms conventional level shifter by over 67% and 55%, respectively. Simulation results show that proposed circuit is able to shift 0.8V to 1.2V with reduced power consumption with little pacification in delay.**

Keywords - CMOS, level shifter (LS), power consumption, delay.

I. INTRODUCTION

Level shifters are the core elements in various electronic systems and these are used to convert the logic signal from one voltage level to other. These are also important circuit component in multi voltage systems and have been used between core circuits and I/O circuit of integrated circuits.

In the past few decades, scaling of geometrical dimensions of VLSI chips has led to great success of Micro Electronics Industry. The voltage scaling can be applied at circuit level by designing multi V_{DD} circuits and further extended to the architectural level. Supply voltage scaling has advanced to design of ASICs and other VLSI chips at architectural level using Multi Supply Voltage (MSV) domains. The high speed circuits are designed using higher V_{DD} compared to other circuits where speed and computation is not a criterion.

With the wide applications of battery supplying devices, such as portable PC, cellar phones and PDA, power consumption has become a critical design concern in today's VLSI circuit and system designs. In addition, approximately millions of transistors have been packed into a single chip in nanometer technologies. So the heat dissipation caused by huge power consumption becomes a problem that can adversely affect reliability and packaging cost of a design. These factors have attracted much attention on low power design of CMOS circuits and driven numerous research efforts to address various kinds of power reduction techniques [13]. Multiple supply voltages techniques have been proposed for low power design. With the use of two different supply voltages, it is possible that a low voltage gate is made to drive a high-voltage one. This leads to the high output of the low-voltage gate cannot fully turn off the PMOS part of the high-voltage gate, so it forms a DC leakage path from the power source to ground. The DC leakage can lead to substantial power loss [8]. To solve this problem, a level shifter is used at the interface of a low-voltage and high-voltage gates. The level shifter is a key circuit component in multi-voltage circuits and has important implementation [15]. For a chip-level DVS system, level Shifters are required between core circuits and I/O circuits interface where low voltage logic signals from chip core are shifted to high voltage level at which pad Ring is working. Since the level shifter circuit consumes power and has a considerable delay, how to optimize the performance to gain low power and small delay and how to minimize the number of level shifters are important in the voltage scaling technique. In this paper, we study different types of level shifter and also proposed level shifter circuit.

Driven by the need to reduce power consumption and maintain high reliability in leading edge integrated circuits, the nominal operating supply voltage for these devices is falling steadily [1–3]. Complex integrated circuits operating with supply voltages as low as 0.5 V. In order to test these devices or insert them into existing systems it is usually necessary to provide interfaces from the low voltage logic to conventional logic devices operating at 5 V or 3.3 V. Commercially available logic interfaces [5] do not support these very low logic levels, and solutions based on discrete components or analog circuits tend to be large and slow.

II. RELATED WORKS

A. Conventional Level Shifter (CLS)

A conventional DCVS level shifter is shown in Fig. 1, where inputs low supply voltage VDDL and the output high supply voltage VDDH are used. The two PMOS transistors MP2 and MP3 act as a cross-coupled load. Thick gate oxide is used to build the transistors MP2, MP3, MN2, and MN3 to overcome high voltage stress. Assuming that when the input signals (IN) is at VSS, MN2 turns ON and MN3 turns OFF. Because of the positive feedback action of cross-coupled MP2 and MP3, node NL is pulled down to VSS and node NH goes to VDDH. No leakage current path exists between VDDH and VSS. Similarly, the operation reverses if input signal (IN) switches to VDDL, the following procedure is take place. MN2 turns OFF and MN2 turns ON. MN1 pulls down NL to VDDH and NH goes to vss. Finally the transition time from low voltage to high voltage is decided by the current driving capability of MP2. Pull down NMOS has to overcome the PMOS latch action before the output change state, so the size of MN2 and MN3 are much larger than MP2 and MP3 [11].

Fig. 2 shows a multi VDD system where four modules are interacting with each other using CLS. A voltage level conversion at the input of a particular voltage domain will require all the supply voltages of signals coming to this

voltage domain from other voltage domains whose voltage level is lower than its own voltage level [10]. This may result in routing congestion, excessive area utilization and also may pose restrictions on module placement.

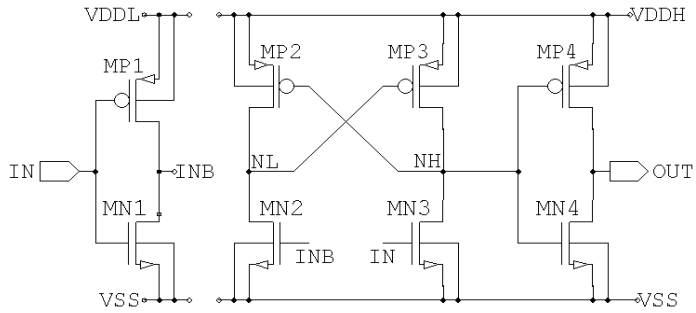

Fig. 1. Conventional DCVS level shifter.

From the schematic diagram of the CVLS shown in Fig. 1, we can observe that the routing of additional supply voltages can be avoided by sending a signal (which is going to a different voltage domain) in both polarities (i.e., IN and INB). However, this strategy would require one additional wire per signal and hence could lead to routing congestion. This problem is further aggravated by the increasing number of voltage domains in SoCs and multi-core architectures.

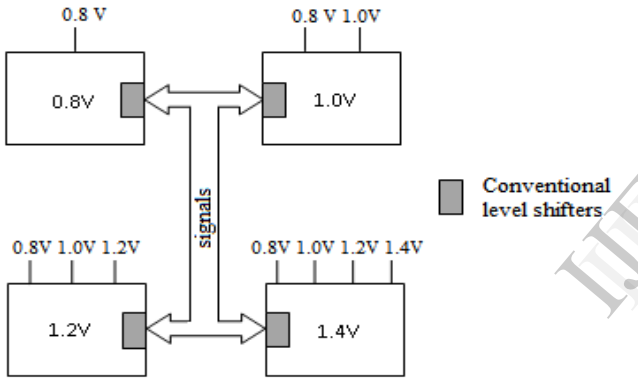

Fig. 2. Multi V_{DD} system using CLS.

B. Single Supply level shifter (SS-LS)

The needs for two voltage supply limit the physical placement of such level shifter to the boundary of high and low voltage designs which restricts the physical design flexibility. To address this, a novel level shifter which requires only one supply VDDH to convert the low Voltage signal to the higher voltage has been proposed. It makes the placement much more flexible in the entire high voltage regions. Fig. 3 shows the schematic diagram of single supply level shifter. The threshold drop (Vtn) across the NMOS MN1 provides a virtual VDDL to the input inverter (MP2, MN2). The output stage is a half latch which pulls up the input of the inverter (MP3, MN3) to VDDH in order to avoid leakage. When input signal (IN) is HIGH, the voltage at node T1 is (VDDH-Vtn) with the purpose of reducing gate to source voltage of MP2 to turn it OFF. When the input signal (IN) is LOW, the feedback transistor MP4 turns ON so that charges node T1 to VDDH to compensate the threshold drop. Hence the supply voltage of inverter (MP2-MN2) is dynamically switched between VDDH-Vtn and VDDH depending upon the input state.

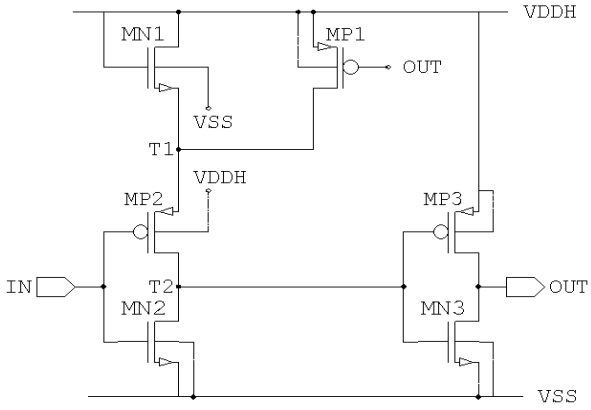

Fig. 3. Single supply level shifter.

Fig. 4 shows a multi V_{DD} system, where four modules interact with each other using SS-LS.

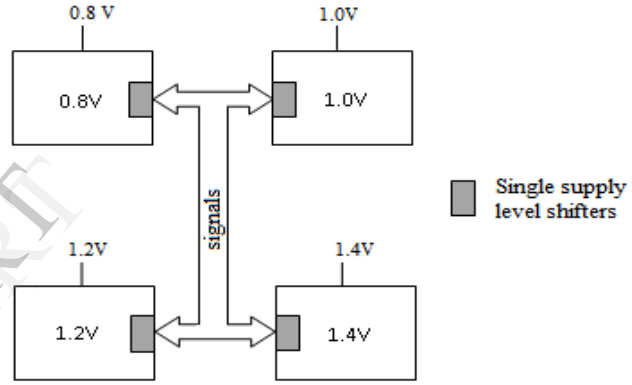

Fig. 4. Multi V_{DD} system using SS-LS.

III. PROPOSED LS

Leakage power results from leakage currents that arise from substrate injection and sub-threshold [6]. Leakage power depends on the total number of transistors and their operating condition in spite of their switching activity. Power consumption can be reduced by scaling supply voltage and capacitance. Problems of small voltage swing, insufficient noise margin and leakage currents start to originate with the scaling the power supply voltage. Other methods for power saving include body biasing, power down strategies, minimization of effective switching capacitances etc. A low to high voltage level shifter is required along with the some mechanism of preventing the MOSFET leakages. A high voltage tolerant level shifter [9] is one of the configurations which solve these issues.

The proposed high voltage level shifter (HV-LS) is shown in Fig.5. The proposed LS was designed using the commercial 50-nm CMOS Microelectronics Technology. The proposed LS circuit converts the input signal 1.8V into the output signal of 3.6V with little pacification in delay. In the

LS circuit PMOS transistors MP2 and MP2 are cross-coupled, while NMOS transistors MN4 and MN5 receive input signals IN and INB respectively. The differences include that thick gate-oxide MOS transistors are used except for the input NMOS transistors MN4, MN5 and that the gates of MP4, MP5, MN2 and MN3 are supplied with the input signal instead of dc voltage [7].

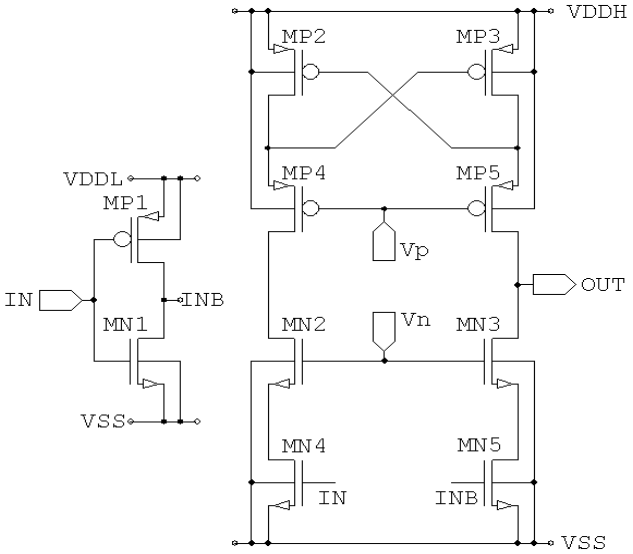

Fig. 5. Proposed high voltage level shifter.

IV. SIMULATION RESULTS AND DISCUSSIONS

A logic swinging between 0.8V and 0V is applied at input signal and the level shifted signals swinging between 1.2V and 0V are obtained at output signal. For schematic design, a W/L ratio of 4:1 is used circuits have been simulated in HSpice with TSMC 50nm CMOS process technology. The values of threshold voltages (V_{TH}) for NMOS and PMOS are taken 0.22V and –0.22V respectively. The values for the dual voltage supplies are used as VDDH = 1.2V and VDDL = 0.8V.

Proposed and existing level shifter circuits have been simulated in 50nm technology using TSMC005 model file with same set of input parameters and comparisons have been made. Table 1 show the results of power consumption and delay for proposed level shifter design for voltage level conversion from 0.8V to 1.2V at a temperature of 27^0C. Column 1 reports the performance parameter under consideration. Column 2 reports the results obtained for the conventional level shifter (CLS). Column 3 reports the results obtained for the single-supply level shifter (SS-LS). Column 4 reports the results obtained for the proposed high voltage level shifter. From table I, proposed HV-LS was properly designed to limit power consumption and the propagation delay.

Fig. 6 shows measured waveforms for this circuit implemented in a commercial 50nm process technology. Power, performance and delay are all captured in Fig. 7, which illustrates a bar graph representation for all three downshifter circuits. From this graph and with an emphasis on the performance and power consumption, we consider the high voltage level shifter as the superior circuit for level shifting.

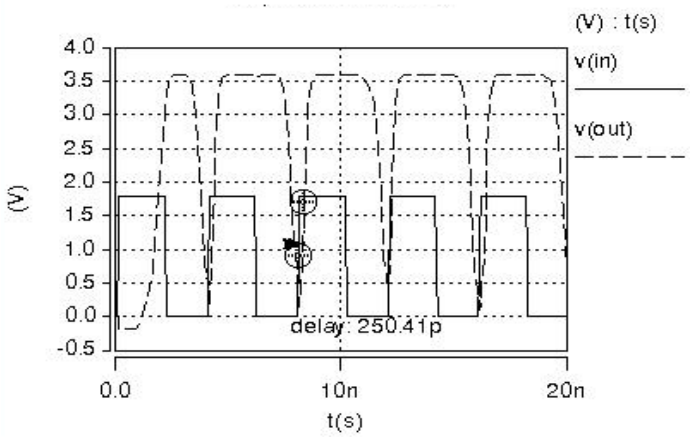

Fig. 6. HSpice simulation Waveforms

TABLE I. SUMMARY OF SIMULATION RESULTS

	Level Shifter Designs		
Performance Parameter	**CLS**	**SS-LS**	**HV-LS**
Average power (nW)	146.28	59.49	54.32
Rising delay (ps)	68.12	79.37	87.79
Falling delay(ps)	59.86	122.52	63.22
Delay (ps)	450.75	65.07	35.41

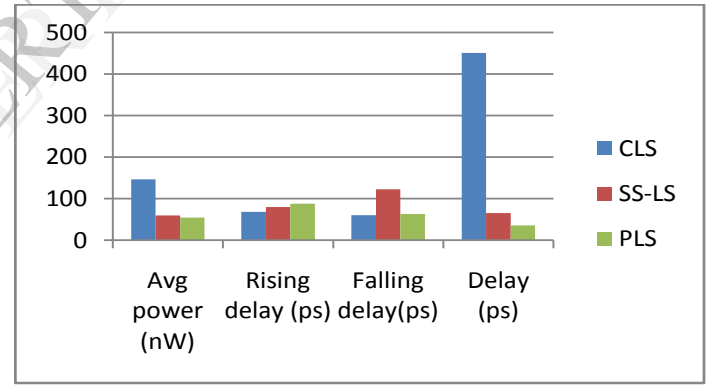

Fig.7. Bar chart comparison of level shifters

V. CONCLUSION

Modern ICs often have several voltage domains. Whenever a signal traverses voltage domains, a level shifter is required. Moreover, these ICs often employ dynamic voltage scaling, due to which it may not be possible to know apriori if a high to low or low to high voltage level conversion is required.

In this paper we have presented several level shifters (which can handle low to high transactions) for simultaneously improving switching speed and power consumption to traditional CMOS levels. We have used HSpice to simulate the operation of the new low power level shifter circuit. The proposed circuit exploits proper design

approach to limit power consumption and the propagation delay. The proposed level shifter design outperforms conventional level shifter by over 67% and 55%, respectively. Simulation results show that proposed circuit is able to shift 0.8V to 1.2V with reduced power consumption with little pacification in delay. Moreover, even though the proposed LS is minimized for low power consumption, it also attained high speed of operation.

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