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A Neural Network-Designed Multilevel Inverter with Reduced Switches and THD

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Abstract
Residential and industrial medium-voltage conversion uses multilevel inverters. Harmonics from non-linear loads in the power supply can damage apparatus. Eliminating losses improves efficiency. This study presents an asymmetric multilevel inverter construction with 31 levels for solar photovoltaic systems. The 31-stage cascaded H-bridge asymmetrical multilevel inverter lowers overall harmonic distortion, loss, switching, and electromagnetic noise. PV voltage is increased above DC connection voltage via a flyback converter system between solar modules and the inverter. For the aforementioned configuration to supply driven pulse signals for power electronics switches, MC pulse width modulation is necessary. The DC voltage sources that are bitwise input are 6, 12, 24, and 48 Vdc. MATLAB and Simulink are used to demonstrate this multilayer inverter. It is demonstrated that the recommended architecture is beneficial because of its lower accessory count, uniformity, and value-effectiveness after analysing switches, sources, diodes, and capacitors. With a THD of 2.75%, this topology satisfies IEEE harmonic standards.

Keywords: **Multilevel inverter, DC voltage, Fuzzy logic control, THD and modulation technique**

1. INTRODUCTION

Recent powerful applications have used multilevel inverter topology. When converting power, the majority of active semiconductor connectors should be utilised to vary a basic voltage. Multilevel inverters are used in solar systems, FACTS, and other forms of energy. Most inverters are NPC, T-type, or CHB multilevel inverters. Multilevel inverters need cascaded inverters with multiple DC sources. Cascaded inverters can be symmetrical or asymmetrical. A hybrid converter topology and modulation approach enhanced efficiency, enhancement factor, and THD in a recent study.

Here we present a brand-new multi-level single-phase hybrid inverter with exceptional performance. Because it provides excellent gain and efficiency in a tiny package with low voltage and current. Solar applications frequently employ impedance-based enhancement converters. This design is advantageous because of its high [1], low power consumption, and multilayer o/p voltage and V gain characteristics. The time-domain optimization techniques used to build the single-phase multilevel inverter architecture are aimed at decreasing the total harmonic distortion (THD) of the out. V & I for any R-L load. As an optimization constraint, this is utilized to determine the inverter's switching angle. [2]

For both standalone and interconnected software, other methods have been proposed. With a minimal number of components in the output stage, a novel 1- DC -AC multilevel modular converter has been presented. To get 19 volts at the out. devices in a single ϕ, 3 full-bridge ckts. are equivalently connected to a source, and then three one combined convertors are connected in series. Each 1- modifier has a unique turns relation, and each circuit is accurate to a specific switching frequency [3]. The switching method and its various phases of operation are shown using a five-level single ϕ converter. To find the lowest possible conduction and switching costs [4], rigorous calculations are provided given that only 3 operating switches create each voltage level in different mode of process.

Additionally, the closest modulation technique is used to improve overall efficiency by decreasing the switching activity of the power converter. Multilevel inverters for grid integration have a minimal number of switch elements and DC sources. A system stability and sensitivity analysis are carried out to assess the controller's efficacy. Multi resonant proportional resonant controllers and proportional integral controllers with multi-inverters are used in this method of distributed generation to lessen the utility power's harmonic content and the impact of fixed disturbances. Power injection fault state [5]

The research process took a single step. Multi-level inverters for renewable uses are now feasible because to the introduction of decreased units. Dual-DC-source multilevel symmetrical inverters are used. A single-phase H-bridge converter is used in the key circuit to regulate the polarity of the out. Vol. ckt. By altering the no. of DC i/p units before the key line, the auxiliary network controls the voltage on the dc Input bus. Two pulse width modulation (PWM) methods have been studied to regulate the out. of MLI with minimal power loss and distortion [6]. One novel strategy is a recent examination of a multi-level single-phase inverter. Low-voltage and distributed-power

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applications are seeing increased adoption of single-stage multilevel inverters. The inverter's features are stable and modulable [7].

A lot of attention has been paid to MLIs (multilevel inverters) recently. In order to improve voltage quality and reduce thd, this research suggests employing the Particle swarm optimization to locate optimized DC sources. The optimum rotational displacements are calculated using the PSO method [8]. Since there are fewer DC sources, power supplies, and components in this design, the overall harmonic distortion is reduced, making this design more cost-effective and efficient than conventional multi-level inverters. In grid-connected renewable applications like FACTS, these multi-level inverters are built for reliability even under non-linear loads. [9]

Recent years have seen a rise in the use of multi-level inverters (MLIs) due to their superior "voltage drop" and "total harmonic distortion (THD)" qualities. While MLI is a practical solution for integrating renewable energy sources, increasing the number of power switches can destabilize the circuit. The dependability of a circuit can be enhanced by the incorporation of features like reduced device count (RD) and fault tolerance (FT). For example, the "Modified single-phase fault-tolerant MLI topology" illustrates function's tolerance of OCFs. Diode, s/w, D-C sources, capacitor, driver, & total block voltage are all reduced in comparison to alternative MLI topologies [10]. This research grants 2 novel projects for one-phase, multi stage double inverters that can be used to operate and regulate electrical devices and connect renewable energy sources. With this design, the capacitor voltage is always equalised regardless of the operating conditions, load characteristics, or modulation index. Additionally, the suggested architecture can be scaled in a cascade to significantly reduce complexity and improve performance. Enhanced performance was demonstrated in respect to the total number of switches and DC resources with the help of a newly created topology [11]. The high needs in multi-level inverter topology layouts, along with the significant amount of semi. conductive devices & capacitors that fail, contribute to the low reliability of inverters. The other goals of fault-tolerant network design, such as using fewer components, sustaining power output in the event of a burden, allowing exposed and S/C breaker failures at any fault location, managing single switch faults, and more, are significantly hampered by capacitors. The end result is an architecture built on regular inverters that can withstand faults.[12]

To minimize energy waste, PE transformers used in medium- and high-voltage applications switch at low base frequencies. The new method relies on combining these two control systems in such a way that certain degrees of freedom are used to eliminate certain harmonics while other degrees of freedom are utilized to decrease the residual total harmonic distortion. For example, in this generalized formulation, we have a mini. THD and problem [13]. This research suggests a novel project for a multilayer inverter based on a revised capacity design. The topology alters the charge/discharge characteristics of the cap. to increase the o/p voltage without the need of magnetic components. Compared to conventional equivalent topologies, the planned ckt requires less components, such as s/w, vol. sources, and capacitor. [14]

In order to reduce the number of power switches, [15] presented a variety of high-voltage inverters. A full-bridge converter (FBC) changes the DC phase output from these inverters into the AC phase input.

This offers a switch capacitance multilayer inverter-based large enhancing ratios inverter described in [16]. To provide MPPT control in the solar cell, a simplified low-pass detector based on fuzzy logic is created.

There are a total of 25 o/p stages in this 3-source 15-level architecture, which is comprised of 40 vol. sources and twelve switches. A variety of load conditions and load and MI changes were studied by the researchers. [17]. Using fewer components than traditional switching capacitor topologies, [18] designed a 1 source driven square increase. This controller, along by the accompanying control logic, regulates the voltage across the two capacitors. Medium and high motor driven applications, such as the mining & construction industries, drive systems, power generation and show, and many more. [19]

Based on unbiased point size pairing, dynamic response, and a steady-state performance comparisons [20], the suggested modified predictive control model (MPC) technique for T-type 3- 3-level inverters have an unchanged switch frequency and is less complex. In [21], several inverters capable of outputting greater voltages were introduced. Cascading inverter designs use multiple independent Power sources, in contrast to traditional multi-level topologies like the FC and NPC, which rely on a single primary source [22]. The modular setup and adaptability of the cascaded multi-level inverter architecture led to its selection. [23]

In symmetrically constructed CHBs, all DC ideals are equivalent; nevertheless, in unevenly created CHBs, the DC-voltage source values are not equal to attain the required developed levels. Unlike other topologies, where it is difficult to balance and distribute developed volume, CHB techniques are used for medium and developed vol. levels [24]. The Entire Harmonic Distortion (THD) is decreased by this Pulse Modulated SCHM-bridge Multilevel Inverter. APF is used to make a counteracting correction to the magnitude of harmonic current. The intended SCHM system employs a pulse modulation strategy for component arrangement. employing a (LQR) [25]

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2. INVERTER TOPOLOGY WITH A MODIFIED CASCADE

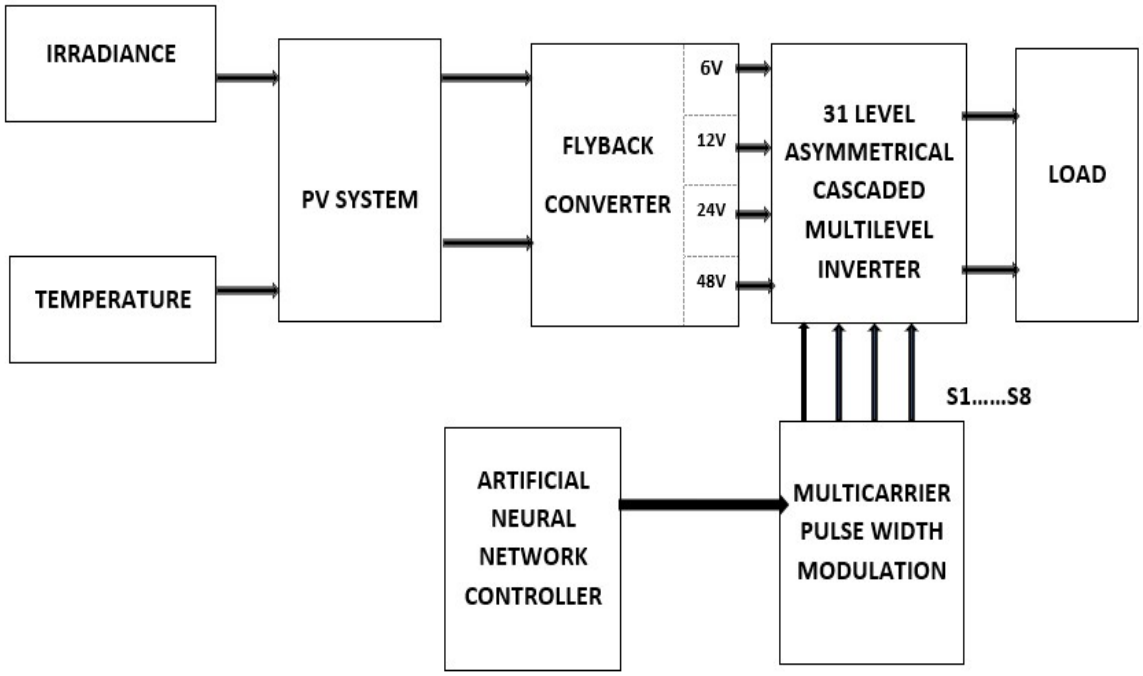

Fig. 1 Block Diagram of Proposed System.

The 31- inverter relies on an additional 8 switches and a D-C voltage to produce the required out. They employ a MC offset P-W-M method to generate the gate triggering pulse. The proposed layout is used to produce several voltage levels from a small number of DC voltage sources and switches. A D-C vol. source and 8 uni-directional power s/w are required for the proposed design. S1, H1, S2, H2, S3, H3, and S4 were picked to symbolize the power switches; VDC was used to denote the DC voltage source. Using an input voltage of 15 volts, the fly back converter produces the D-C vol source (Vdc1 - Vdc4). To generate the necessary output voltage, the multi-carrier offset modulation method sequentially generates pulses and feeds them to the switches. The switches receive pulses that have been produced independently using a method called multi-carrier offset modulation. Several vol. out. level is created regardless of the s/w's on or off position. In this figure (Fig. 1), the source vol. is set at 6V, 12V, 24V & 48V to obtain the maximum amplitude. The 100-ohm resistor and 175-mH inductor are used in this case.

2.1 PV MODULE

An essential part of learning about a solar PV system is designing solar cells. In Fig. 2, the solar cells, the flyback converter, and the 31level multi-level inverter that make up the proposed circuit are laid bare. A proposed ckt. having (IV) and (PV) attributes; the result of solar irradiance and temp. as the fundamental sorts that might be utilized to model solar P-V. The designed solar P-V system is capable of adapting its out. to the current conditions.

Solar Module Fill Factor

Maximum power (Pm = VmxIm) separated by the product of open ckt. Vol. and short ckt. current (Io) is the formula for a solar module's fill factor.

$$Fill\ Factor = \frac{\text{Pm}}{\text{Voc}\times\text{Isc}} \quad (1)$$

When the FF of a solar module is greater, its performance improves. The efficacy of a solar module is distinct as the relation of its max. power output under standard test conditions to its input power out. Power i/p. to a solar module is measured in watts-per sq. meter. Therefore, a thousand A W (A is the noticeable part of the solar unit) is the nominal input power for the cell.

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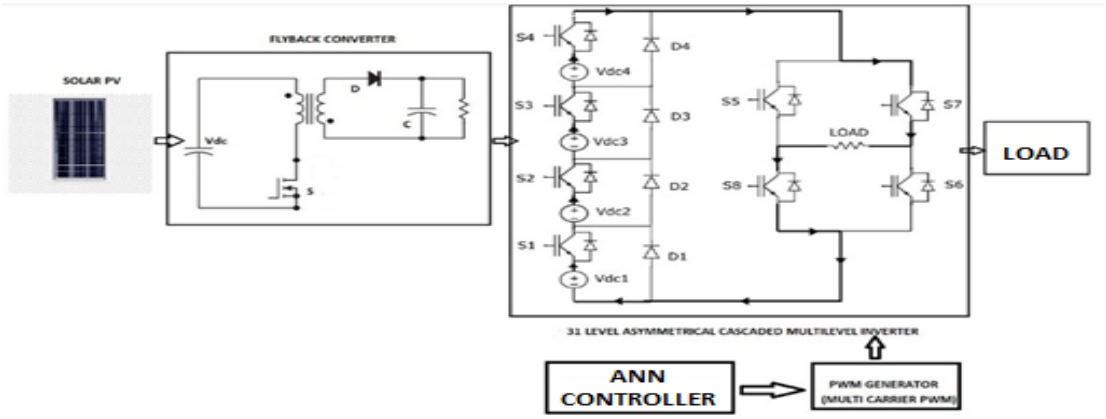

Fig. 2 Fly-back solar P-V conv. for the planned 31-level M-L-I.

1.1 FLYBACK CONVERTER

The flyback converter is shown in Fig. 3 connected to a R load. The FBC was the first of its kind; it achieved electrical isolation between the input/output terminals by slicing the inductor in half. Its size is rather small when compared to the primary transformer. Even 5 or 12 volts are plenty to power it.

This setup calls for a 15-V D-C input and 4 AC outputs. One that operates at very high frequencies. It is controlled by a MOSFET switch. We can't use an IGBT here because its highest operational frequency is only 25 kHz, but the flyback converter needs at least 100 kHz to perform.

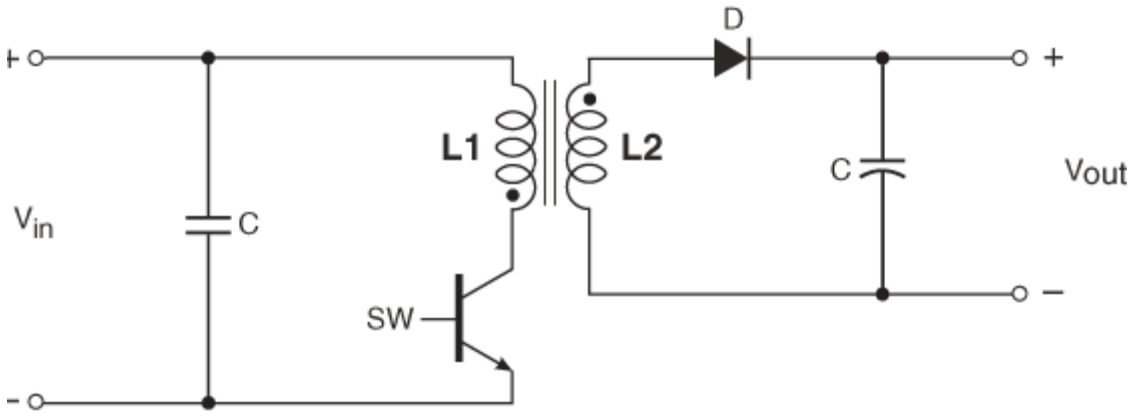

Fig. 3 DC to DC Flyback converter

(DC-DC) Flyback - Converter with Several D-C Out. Vol. Power supply for high-voltage electronics like televisions and computer displays typically utilize flyback converters, which typically have an output power of 50 to 100W. Its modular design and high-performance flexibility are its main selling points. You can boost the output by, say, installing extra windings, diodes, and capacitors. Add the d-c reference voltage Vg. to the simulated load voltage to get the voltage across the transistor. Sometimes, sounds associated with the leakage inductance of the transformer present produce the extra volume. For this clear volt. to be inside the t/r's safe operating range, a trigger circuit may be necessary. When utilizing the mean-shift strategy, a flyback converter can be specified in two different ways. The first option includes moving the stack back to the safety side, where the diodes and MOSFETs are swapped out for P-W-M s/w and direct analogue.

3. MC P-W-M TECHNIQUE

The asymmetric cascade inverter topology of the system is depicted in Fig. 4. A hybrid of the H-bridge with a modular layout. To get a variable output with a segmental project, the D-C source vol. and the no. of s/w must be altered.

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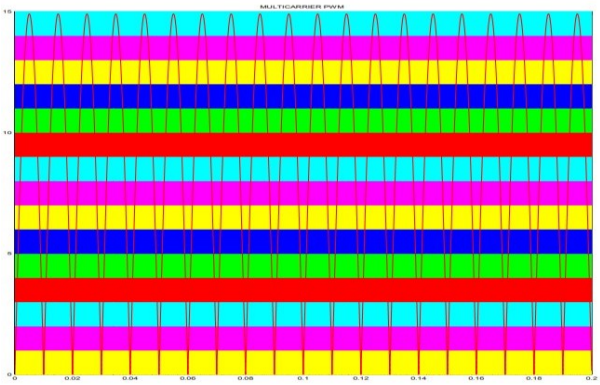

Fig. 4 MC P-W-M

Increasing the D-C source and switch voltage increases the out. Volt. level in a linked architecture. An asymmetric cascaded converter at the 31st level is analyzed. Multi-carrier (PWM) is used to make the control signs for the inverter ckt. in this setup. This PWM technology allows multi-stage inverters to self-balance. Here we show off an asymmetric cascade inverter with 31 stages. Fewer schematic components are needed in the suggested topology, which has several benefits. These benefits contribute to the production of low levels of stress and anxiety. The proposed method in multilevel inverters has applications in both conventional manufacturing and renewable power generation.

An inverter is said to be asymmetrical cascade if the DC source voltages are not of equal amplitude. Growing the D-C volume level and the number of s/w in the sectional plan is a simple way to boost the o/p volume. By altering the topology, we may generate many constant voltage sources and switch between them at will. For an uneven formation, you can use this formula to get the o/p volume.

$$L = (2^{n+1} - 1)$$

3.1 ARTIFICIAL NEURAL NETWORK CONTROLLER METHOD FOR MULTILEVEL INVERTER

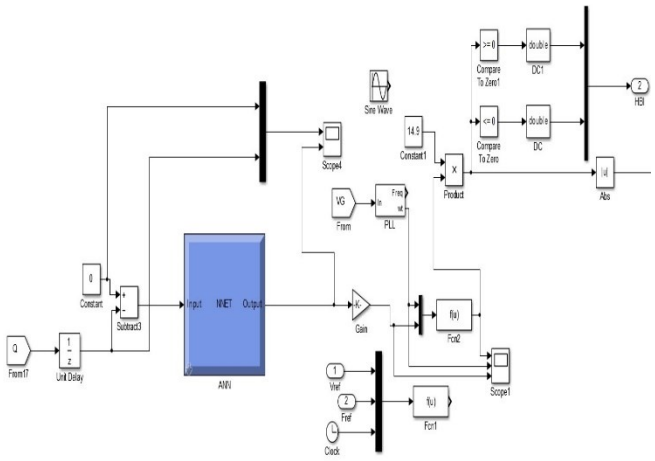

Fig. 5 Architecture of ANN Controller

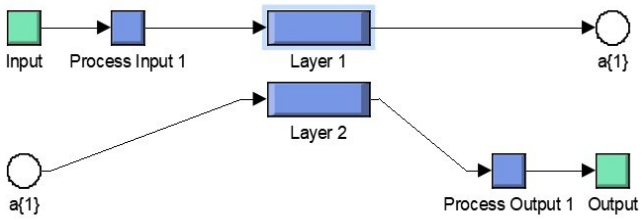

Fig. 6 Flow of ANN Controller

Non-linear operations are what set Artificial Neural Networks (ANNs) apart as a digital/signal processing device. The amazing capacity to draw meaning from imperfect data has been a primary focus of neural networks. Figure 5 & 6 shows the full ANN controller architecture.

$$e_v = V_{ref} - V_{meas} \qquad (2)$$

With two controller outputs taken into account, the designed controller consists of many layers and neural schemes. The selection process in the ANN-based controller is predicated on taking into account the 2-layer efficacy in order to compute the power mistake and RMS. Equation (3) provides the basis for building the second layer, which takes into account the network's increased capacity for prediction along with its increased nonlinear functionality.

$$ep = Pref - Pmeas \qquad (3)$$

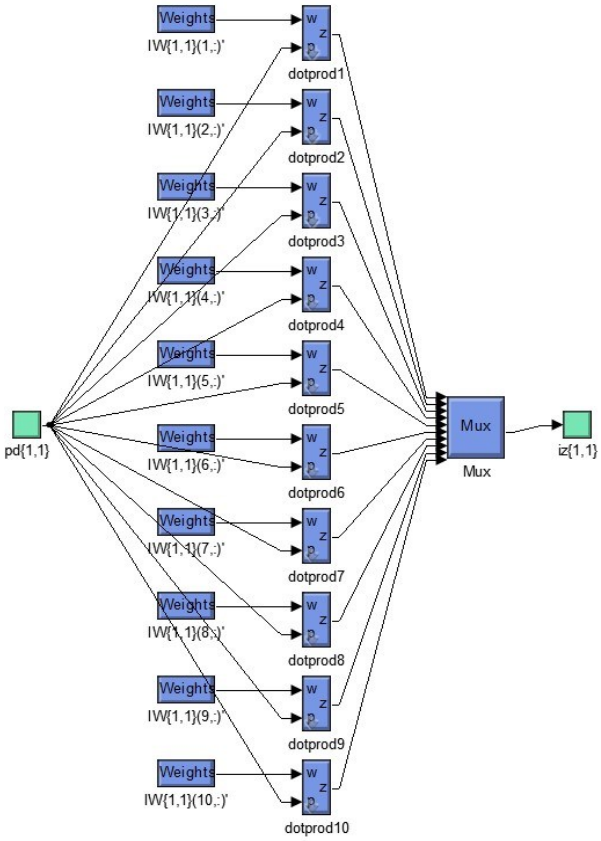

Fig. 7 ANN Controller

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The stages applied in the ANN procedure scheme are presented as follows

1. Initialization of weights
2. Pretraining of data through scaled input and outputs
3. Selection of network structure based on two layers with weights 5*5
4. Evaluation of the training pair with training set
5. The weight and input set is calculated based on the output of the network
6. The error in voltage and power is calculated as ev and ep
7. The computation of error propagation is computed based on backward and weights for minimization.
   Repeat step 5 until the error is minimized for achieving the desire value.

3.4 Modes of operation

For the thirty-one level, we take into account the four input source voltages shown in Fig. 1 as Vdc1, Vdc2, Vdc3, and Vdc4. The i/p voltages of the four different sources are as follows: 6V, 12V, 24V & 48V. An uneven inverter guarantees the lasting viability of both the positive and negative groups. The (+ve) faction sends out positive signals, whereas the (-ve) faction produces negative ones. The methods of process at all values, +ve and -ve, including 0, are depicted in Fig. 8 (a-p). The operational modes are outlined in Table 2's switching pattern.

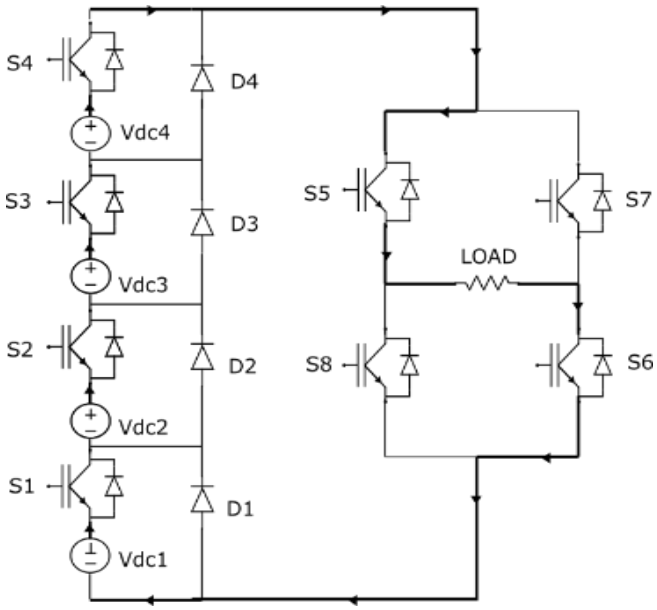

Fig. 8 Switching Diagram of Proposed circuit

4. RESULTS AND DISCUSSION

The Multi-carrier (MCPWM) technique was used to model an enhanced 31-level asymmetric cascaded converter.

Trace analysis employs the usage of fuzzy logic. Matlab/Simulink's MCPWM-based cascaded converter corrects skew at 31 levels. This Resistive load has been simulated with the following parameters: • Inp. Volt. (D-C) = 90v (6v, 12v, 24v, 48v). Switching Frequency = 2kHz Car. Freq.

• R.L. = 100Ω = Resistance. The loading domain's open-circuit voltage is 90 V (or 63.63 V RMS). The o/p volume is displayed for reference. A current of 1.5 A is flowing through the load.

Cur. through the load is depicted graphically in the graph. An FFT analysis of a 31-stage asymmetric cascaded converter is showed in the fig. 3.06% is the value of the FFT THD.

4.1. A) Simulation Ckt.

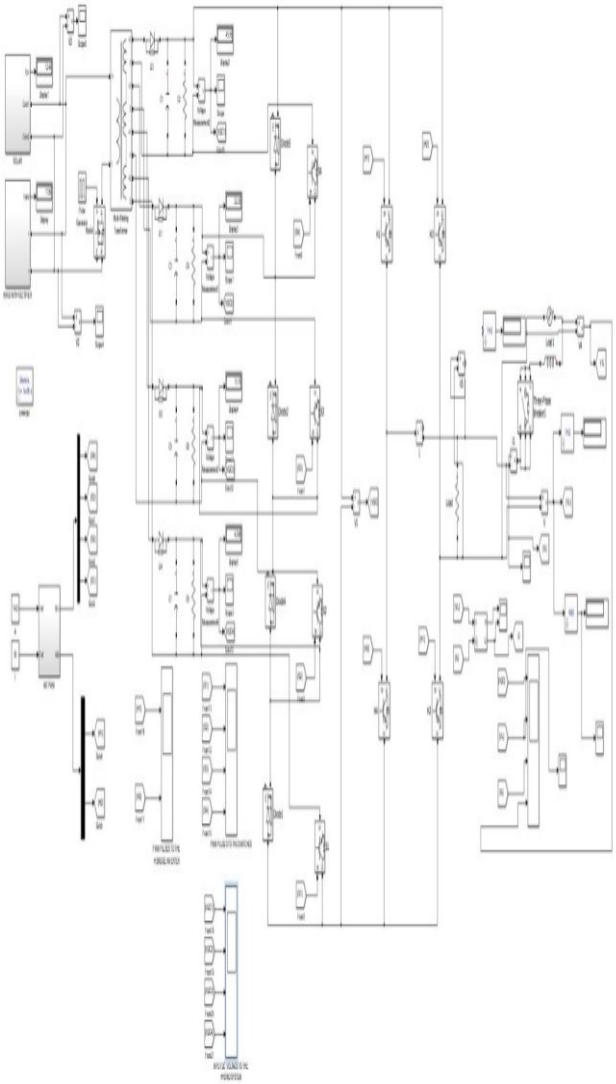

Fig. 9 Simulation Ckt. of Planned circuit

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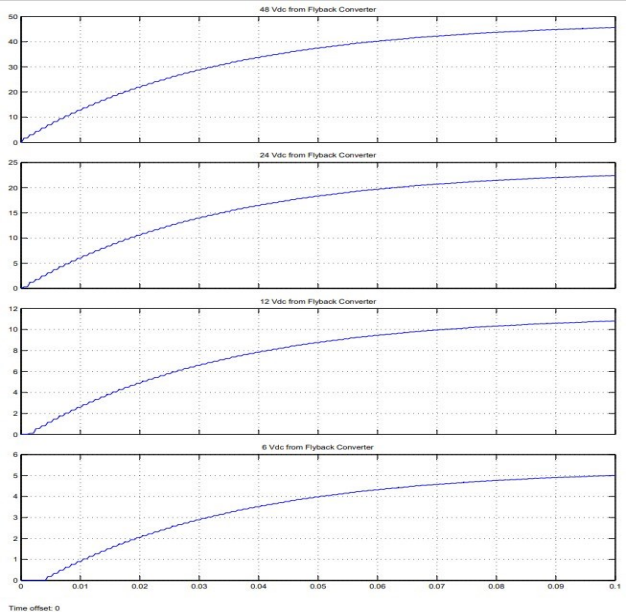

Fig. 10 Different Volt. from Flyback-converter

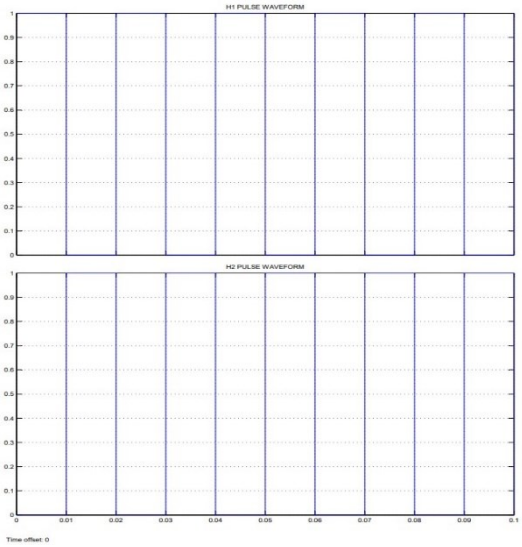

Fig.11: P-W-M PULSES TO H1 & H2

4.1.B. PWM TECHNIQUE:

A pulse width modulator (PWM) converts digital data into analogue form. To put it simply, it's a square wave that alternates between on and off. In this implementation of PWM, we employ the multicarrier offset method. In this case, we are comparing a carrier signal to a reference signal as a means of controlling the system.

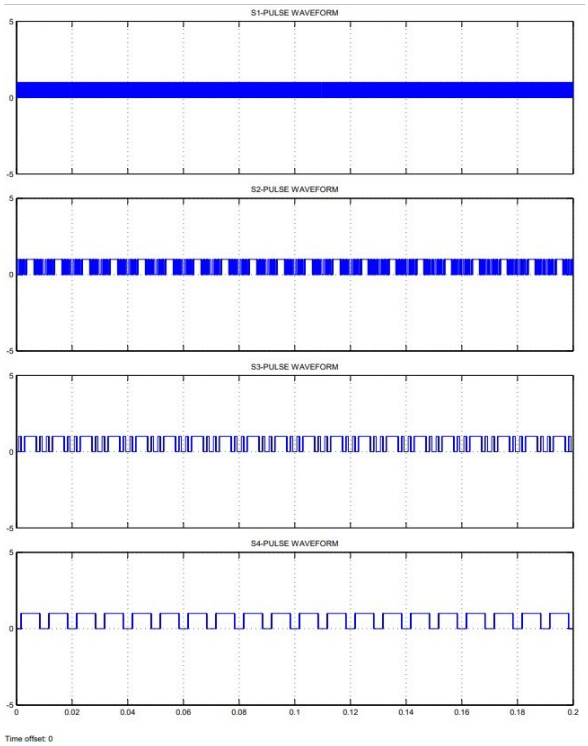

Fig. 12 P-W-M Pulses to S1 To S4

4.1.C. SIIMULATION O/P VOLTAGE & C/T

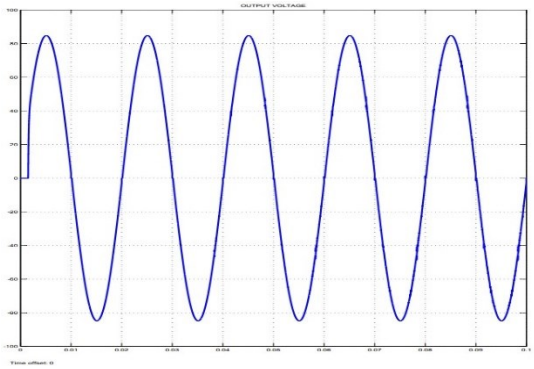

Fig. 13 O/P Voltage of 31 MLI

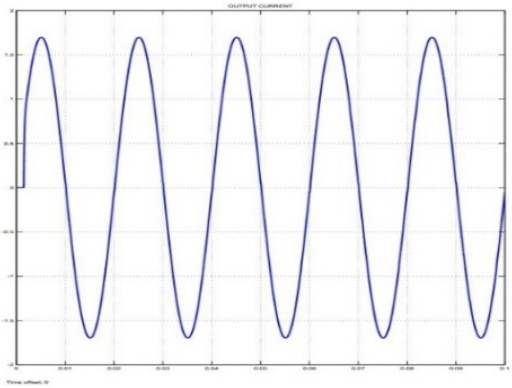

Fig. 14 Output Current of 31 MLI

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4.1.D. FFT ANALYSIS

Fig.15 displays the results of the FFT analysis performed on the 31st level. THD is calculated to be 2.75% using FFT.

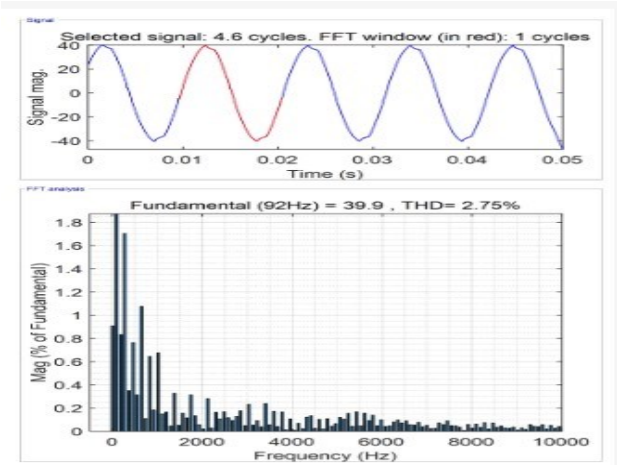

Fig. 15 FFT Analysis of 31 MLI

4.1.E. COMPARATIVE ANALYSIS OF THD

Table 1 Comparative analysis of T-H-D

S. No	Ref. papers	P-W-M technique	Cont.	THD
1	Fuzzy controller using superimposed carrier PWM	Super imposed carrier PWM	Fuzzy logic controller	8.7%
2	Asymmetric cascaded MLI	Low frequenc y PWM	PIC controller	10.2%
3	Harmonic minimization technique	Harmoni c minimiz ation	High speed multivaria ble digital controller (DS1104)	4.36%
4	MLI design with reduced switches	MC PWM	Fuzzy-Logic	3.06%
4	Proposed paper	MC PWM	ANN	2.75%

In Table 3, THD percentage, controller used and PWM technique implemented is compared with some reference papers. In which we came to a conclusion that THD % in the proposed paper is less compared to the reference papers and also within the IEEE standard (< 5%).

4.1.F. COMPARISON OF DESIGN PARAMETERS

Table 2 Comparison of parameters

ITEMS	DCMLI	FCM LI	CHB MLI	Ref paper	Propose d MLI
No. of S/w	60	60	60	10	8
No. of Sources	1	1	15	4	1
Out. Volt. Level	31	31	31	31	31
Diodes	56	0	0	0	4
Capacitors	0	28	0	0	4
% THD	-	-	-	3.06	2.75

Table 4 compares several MLI types, including the ones previously mentioned with our suggested work, based on characteristics like capacitance, semiconductor diode, no. of s/ws, no. of sources, out volt. level, and % THD. Table 4 shows that the suggested paper's parameters are real and have a lower total harmonic distortion.

5.CONCLUSION

Any desired number of o/p vol. levels can be generated by this simulated cascaded H-bridge asymmetrical multilevel inverter. The primary advantage of this design is its basic construction, which reduces the size of the multilayer inverter and simplifies the driving circuit. The MATLAB/SIMULINK platform was used for the simulation. A flyback converter's primary side can provide four different D-C output voltages: 6V, 12V, 24V & 48V. Asymmetrical MLI takes input from many voltage sources and generates an o/p volume level with 31 steps using just 8 switching transistors. The output power from the multilayer inverter is linked to the power grid. The THD is calculated to be 2.75% via simulation. The T-H-D value in our suggested study is fewer and within the IEEE standard (5%), as confirmed by a comparison with a number of reference works. This document demonstrates the simulation's results.

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