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A New Cascaded Multilevel Inverter Fed Permanent Magnet Synchronous Motor By Using Sinusoidal Pulse Width Modulation

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ABSTRACT-Multilevel inverter (MLI) is a new breed of power converter that is suited for high power applications. In recent years, multilevel inverters are becoming increasingly popular for high-power applications due to their improved harmonic profile and increased power ratings. Several studies have been reported in the literature on multilevel inverters topologies, control techniques, and applications. However, there are few studies that actually discuss or evaluate the performance of Permanent Magnet Synchronous motor(PMSM) drives associated with three-phase multilevel inverter. This paper presents a study of asymmetrical cascaded H-bridge multilevel with Sinusoidal pulse width modulation(SPWM) fed Permanent Magnet Synchronous motor drive. In this case, asymmetrical arrangements of seven- and nine-level H-bridge inverters are compared in order to find an optimum arrangement with lower switching losses, with less no of switching devices and optimized output voltage quality In this paper simulation of SPWM are applied for performance analysis of PMSM using voltage source inverter. The THD and speed torque analysis for PMSM are simulated using MATLAB simulink. The carried out MATLAB simulation results show that the voltages are nearly sinusoidal with very low distortion, using less switching devices and torque ripples are greatly reduced.

Keywords: Cascaded H-bridge Multilevel Invrter, Multicarrier sinsoidal pulse width modulation (MCSPWM), Permanent Magnet Synchronous Motor(PMSM)

I. INTRODUCTION

MULTILEVEL voltage-source inverters are intensively studied for high-power applications and standard drives for medium-voltage industrial applications have become available Solutions with a higher number of output voltage levels have the capability to synthesize waveforms with a better harmonic spectrum and to limit the motor winding insulation stress. Many studies have been conducted toward improving multilevel inverter. Among the various topologies, asymmetric cascaded MLI is employed as it requires two unequal dc sources for producing a seven- and nine- level output [3]. In symmetrical multilevel inverter, all H-bridge cells are fed by equal voltages, and hence all the arm cells produce similar output voltage steps. However, if all the cells are not fed by equal voltages, the inverter becomes an asymmetrical one. In addition, this topology provides low switching losses and high conversion efficiency. The modulation strategy employed in this paper is the phase disposition (PD) sine PWM (SPWM) technique. In this method, triangular wave is used as carrier. In order to produce a m-level output, generally(m-1) carriers are needed [4]. The SPWM technique has a better spectral quality and a higher fundamental component also, there is a reduction in the total harmonic distortion (THD) and switching losses.

This paper focuses on step by step development of SPWM implemented on PMSM. The model of a three-phase voltage source inverter is discussed based on SPWM technique. Simulation results are obtained using MATLAB/Simulink environment for effectiveness of the study.

II. CASCADED H-BRIDGE MULTULEVEL INVERTER

The cascaded H-bridge inverter consists of power conversion cells, each supplied by an isolated dc source on the dc side, which can be obtained from batteries, fuel cells, or ultra capacitors, and series-connected on the ac side. The advantage of this topology is that the modulation, control, and protection requirements of each bridge are modular. It should b pointed out that, unlike the diode-clamped and flying-capacitor topologies, isolated dc sources are required for each cell in each phase. Fig. 1 shows topology of a cascade inverter with isolated dc-voltage sources. An output phase-voltage waveform is obtained by summing the bridges output voltages

$$v_o(t) = v_{o,1}(t) + v_{o,2}(t) + \cdots + v_{o,N}(t) \quad (1)$$

where *N* is the number of cascaded bridges.

The inverter output voltage $v_o(t)$ may be determined from the individual cells switching states

$$v_o(t) = \Sigma(\mu_j - 1)V_{dc,j}, \quad \mu_j = 0,1,\ldots \tag{2}$$

If all dc-voltage sources in Fig. 1 are equal to V_{dc}, the inverter is then known as a symmetric multilevel one. The effective number of output voltage levels *n* in symmetric multilevel inverter
is related to the cells number by

$$n = 1+2N$$

The maximum output voltage $V_{o,Max}$ is then

$$V_{o,MAX} = NV_{dc}. \tag{3}$$

To provide a large number of output levels without increasing the number of inverters, symmetric multilevel inverters can be used. In [18] and [19], it is proposed to chose the dc-voltages sources according to a geometric progression with a factor of 2 or 3. For *N* of such cascade inverters, one can achieve the following distinct voltage levels

$$\begin{aligned} n &= 2^{N+1} - 1, \quad \text{if } V_{dc,j} = 2^{j-1}V_{dc}, \quad j = 1, 2, \ldots, N \\ n &= 3^N, \quad \text{if } V_{dc,j} = 3^{j-1}V_{dc}, \quad j = 1, 2, \ldots, N. \end{aligned} \tag{4}$$

For example, Figs. 1structure of bridge arrangement for one phase with seven level. Two dc sources V_{dc} and $2V_{dc}$ for seven-levels output (output waveform for seven level shown in Fig.2) and two dc sources V_{dc} and $3V_{dc}$ for nine-levels output(output waveform for nine level shown in Fig.3).

	Symmetrical inverter	Asymmetrical inverter	
		Binary	Ternary
N	$2N+1$	$2^{N+1}-1$	3^N
DC sources number	N	N	N
Switches number	$4N$	$4N$	$4N$
$V_{o.MAX}$ [pu]	N	2^N-1	$(3^N-1)/2$

Table.1 Comparison of Multilevel inverters

The maximum output voltage of these *N* cascaded multilevel inverters is

$$V_{0,MAX} = \sum_{j=i}^{N} V_{dc,j} \tag{5}$$

The above Equation (5) can be rewritten as

$$\begin{aligned} V_{0,MAX} &= (2^N - 1)V_{dc} \quad \text{if } V_{dc,j} = 2^{j-1}V_{dc} \quad j = 1, 2, \ldots, N \\ V_{0,MAX} &= \left(\frac{3^N-1}{2}\right)V_{dc} \quad \text{if } V_{dc,j} = 3^{j-1}V_{dc} \quad j = 1, 2, \ldots, N \end{aligned} \tag{6}$$

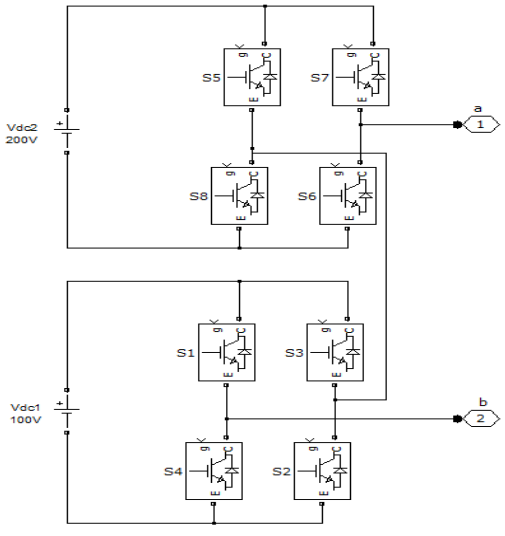

Fig.1 Structure of two-cells cascaded multilevel Cascaded MLI with unequal dc sources for seven level output voltage

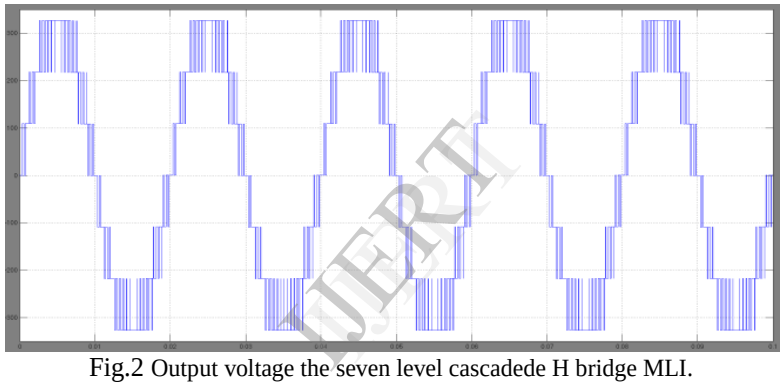

Fig.2 Output voltage the seven level cascadede H bridge MLI.

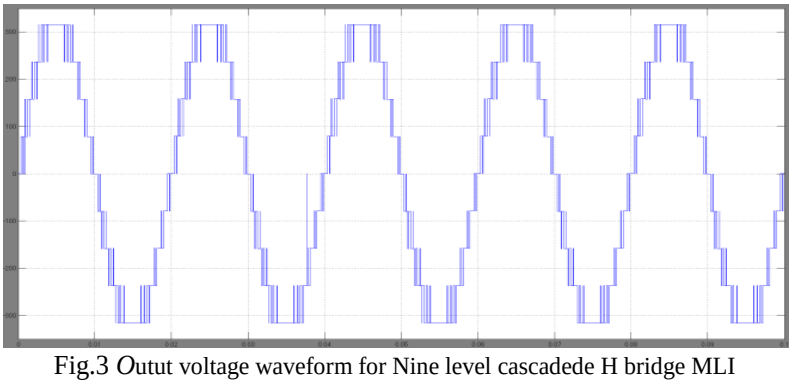

Fig.3 *O*utut voltage waveform for Nine level cascadede H bridge MLI

It can be seen that asymmetrical multilevel inverters can generate more voltage levels and higher maximum output voltage with the same number of bridges. Table I summarizes the number of levels, switches, dc sources, and maximum available output voltages for classical cascaded multilevel inverters. Increasing the number of levels provides more steps; hence, the output voltage

will be of higher resolution and the reference sinusoidal output voltage can be better achieved. Among the n_3 switching states of *n*-level inverter, there is *n* zero states, where zero output voltages are produced.

An example phase voltage waveform for an 11-level cascaded H-bridge inverter with 5 SDCSs and 5 full bridges is shown in Figure 4. An output phase-voltage waveform is obtained by summing the bridges output voltages

$$V_{an} = Va1 + Va2 + Va3 + Va4 + Va5.$$

For a stepped waveform such as the one depicted in Fig. 4 with s steps, the Fourier Transform for this waveform follows.

$$V(wt) = \frac{4V_{dc}}{\pi}\Sigma[\cos(n\theta_1) + \cos(n\theta_2) + \cdots \quad \ldots + \cos(n\theta_s)]\frac{\sin(n\omega t)}{n} \tag{7}$$

$$where\ n = 1,3,5,7\ldots$$

where s is the number of separate dc sources.

From equation (6), the magnitudes of the Fourier coefficients when normalized with respect to Vdc are as follows:

$$H(n) = \frac{4}{\pi n}[\cos(n\theta_1) + \cos(n\theta_2) + \quad \ldots\ldots + \cos(n\theta_s)] \tag{8}$$

$$where\ n = 1,3,5,7\ldots$$

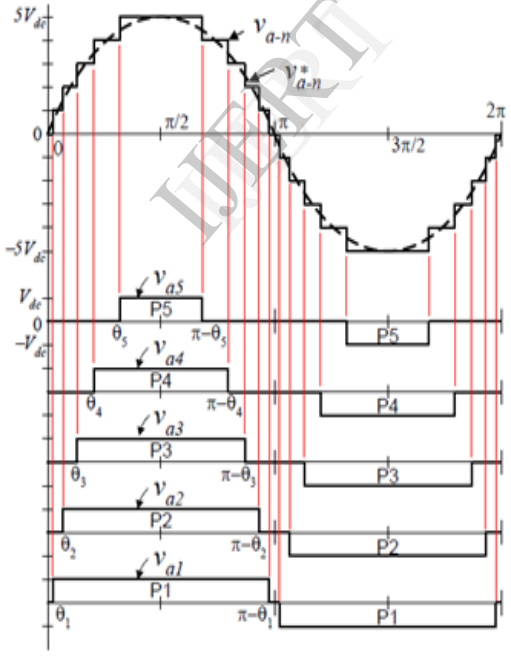

Fig.4 Output phase voltage waveform of an 11-level cascade inverter with 5 separate dc sources.

The conducting angles, θ1, θ2... θs, can be chosen such that the voltage total harmonic distortion is a minimum. Generally, these angles are chosen so that predominant lower frequency harmonics, 5th, 7th, 11th, and 13th, harmonics are eliminated.

Multilevel cascaded inverters have been proposed for such applications as static var generation, an interface with renewable energy sources, and for battery-based applications.

III. PWM TECHNIQUES

Output voltage from an inverter can also be adjusted by exercising a control within the inverter itself. The most efficient method of doing this is by pulse-width modulation control used within an inverter. In this method, a fixed dc input voltage is given to the inverter and a controlled ac output voltage is obtained by adjusting the on and off periods of the inverter components. This is the most popular method of controlling the output voltage and this method is termed as Pulse-Width Modulation (PWM) Control. PWM techniques are characterized by constant amplitude pulses. The width of these pulses is however modulated to obtain inverter output voltage control and to reduce its harmonic content.

The different PWM techniques are as under:

a) Single-pulse modulation
b) Multiple pulse modulations
c) Sinusoidal pulse width modulation.

Here we studied about Multicarrier based Pulse Width Modulation.

Multicarrier SPWM Technique

The multicarrier PWM method uses several triangular carrier signals, keeping only one modulating sinusoidal signal. If an 'n' level inverter is employed, 'n-1' carriers will be needed. The carriers will have the same frequency and the same peak to peak amplitude and are disposed so that the bands they occupy are contiguous. The zero reference is placed in the middle of the carrier set. The modulating signal is a sinusoid of frequency 50 Hz. At every instant each carrier is compared with the modulating signal. Each comparison gives one if the modulating signal is greater than the triangular carrier, zero otherwise. The results are added to give the voltage level, which is required at the output terminal of the inverter. Multicarrier PWM method can be categorized into 2 groups. 1) Carrier disposition methods (CD) where the reference waveform is sampled through a number of carrier waveforms displaced by contiguous increments of the reference waveform amplitude, 2) Phase shifted PWM method, where the multiple carriers are phase shifted accordingly.3) Alternate Phase Opposition Disposition PWM strategy (APODWM) In APOD strategy the carriers of same amplitude are phase displaced from each other by 180 degrees alternately. 4)Variable frequency PWM strategy (VFPWM) The number of switching for upper and lower devices of chosen MLI is much more than that of intermediate switches in other PWM using constant frequency carriers. In order to equalize the number of switching for all the switches, variable frequency PWM strategy is used.

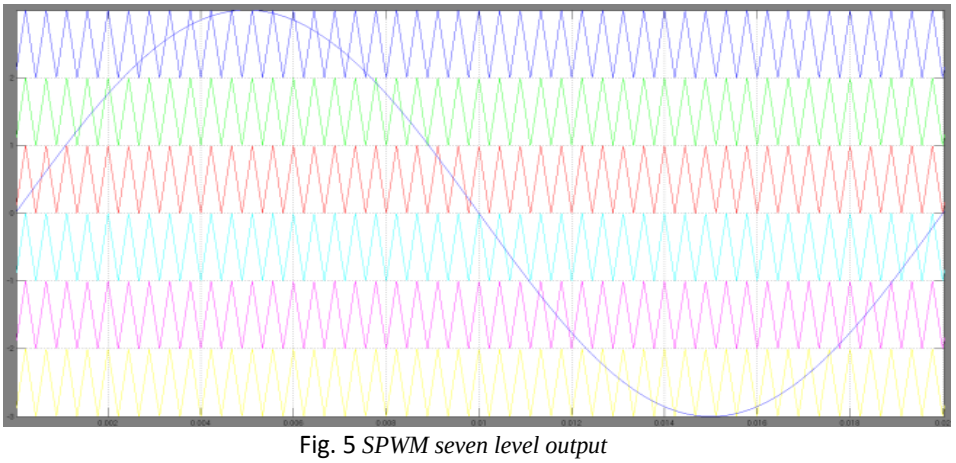

Fig. 5 *SPWM seven level output*

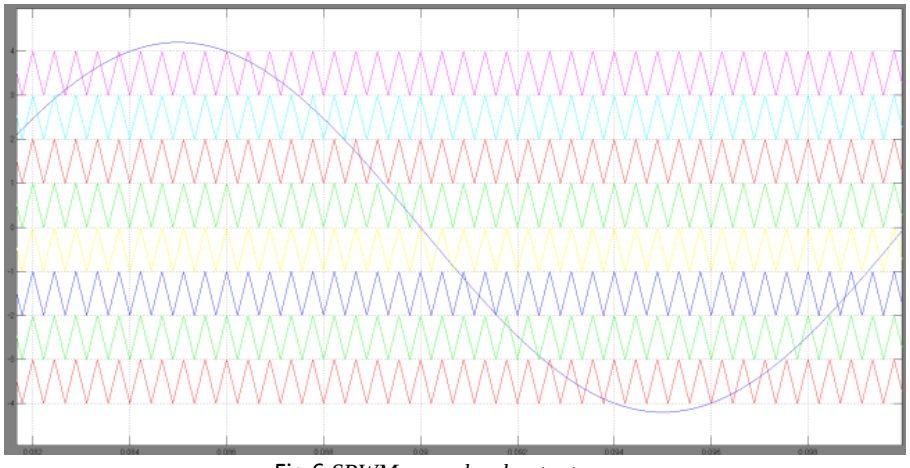

Fig.6 *SPWM seven level output*

Among these classifications, the phase disposition method is more commonly is employed in this paper as it gives least total harmonic distortion.

IV. PERMANENT MAGNET SYNCHRONOUS MACHINES

Permanent magnet synchronous motors are increasing applied in several areas such as traction, automobiles, robotics and aerospace technology. The power density of permanent magnet synchronous motor is higher than one of induction motor with the same ratings due to the no stator power dedicated to the magnetic field production. Nowadays, permanent magnet synchronous motor is designed not only to be more powerful but also with lower mass and lower moment of inertia.

The Permanent Magnet Synchronous Machine (PMSM) Is Primarily Associated With High-performance Applications and Is Normally Fed by a Voltage Source Inverter (VSI). The machine is of the Synchronous Type and the Rotor Field Is Created by Permanent Magnets attached To the Rotor. The Material of the Permanent Magnets can differ but the Best materials Are of Rare Earth Type, Such As Samarium-Cobalt (Sm-Co) Or Neodymium-Iron-Boron (Nefeb). The Nefeb Magnets Combine a High Flux Density with a Large Coercive force. Unfortunately, they are still quite expensive but the price has dropped during the last decade. The advantage of using permanent magnets in the rotor circuit is that the design of the machine is simplified and that there are virtually no losses in the rotor circuit since the rotor is (ideally) free of currents. The stator winding can be wound in several ways. Machines with trapezoidal wound stator windings are called brushless dc machines and should be fed by trapezoidal currents to produce a smooth torque. Another winding method is to wound the stator sinusoidal. The combination of a sinusoidal wound stator and a permanent magnet rotor design is the basis of the permanent magnet synchronous machine. The distribution of the magnets in the rotor can vary significantly. Methods for controlling PMSM drives, connected to different types of converters, have been developed both for steady state operation and high performance servo control. This paper discusses the Torque ripple control of the PMSM using SPWM technique in Asymmetrical cascaded inverter .

Torque ripple produced by a PMSM comes from two different sources. The first ones were known as cogging torque. Cogging torque is generated by the interaction of the rotor magnetic flux and angular variations in the stator magnetic reluctance. Different methods for reducing cogging torque exist and they mostly rely on changes in the design of the machine. One usual design method is known as skewing, which can be done on both the rotor and stator. Skewing can reduce the cogging torque very effectively manufacturing procedure is complicated, which increases the price of the machine. The other method for reducing torque ripple in an existing machine is to use control schemes that reduce torque ripple. The basic goal of these control schemes is to control the currents that the ripple is cancelled out (this is known as harmonic injection). In this increasing the no of output voltage levels to Nine level, voltage quality is improved and total harmonic distortion is reduced so that the torque ripples are greatly reduced.

V. SIMULATION RESULTS

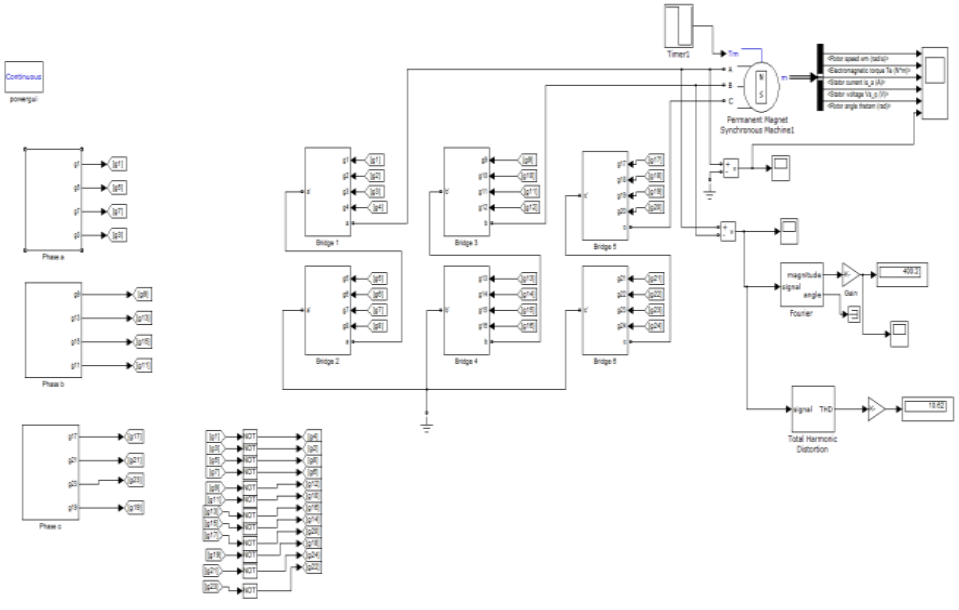

Fig.7 Simulink Block diagram

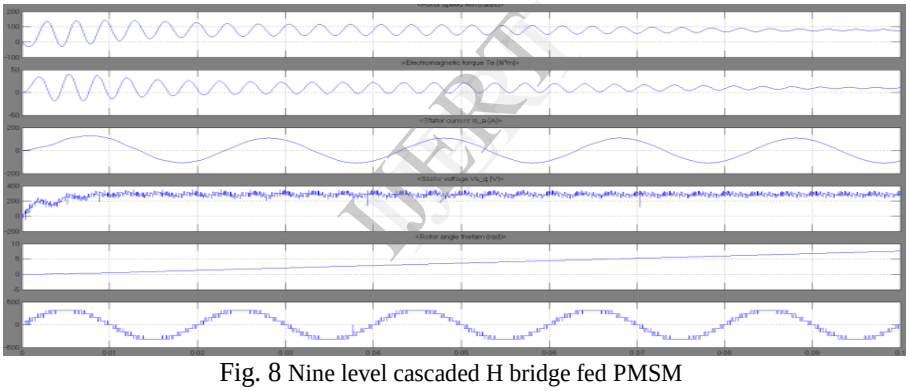

Fig. 8 Nine level cascaded H bridge fed PMSM

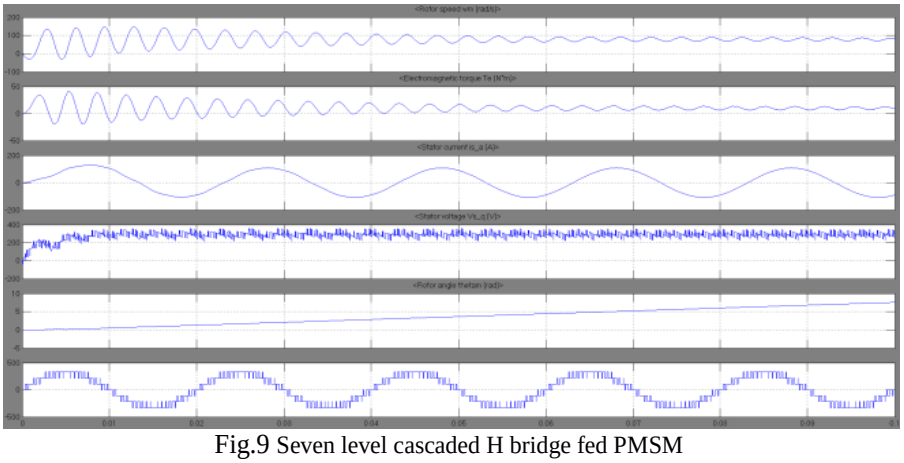

Fig.9 Seven level cascaded H bridge fed PMSM

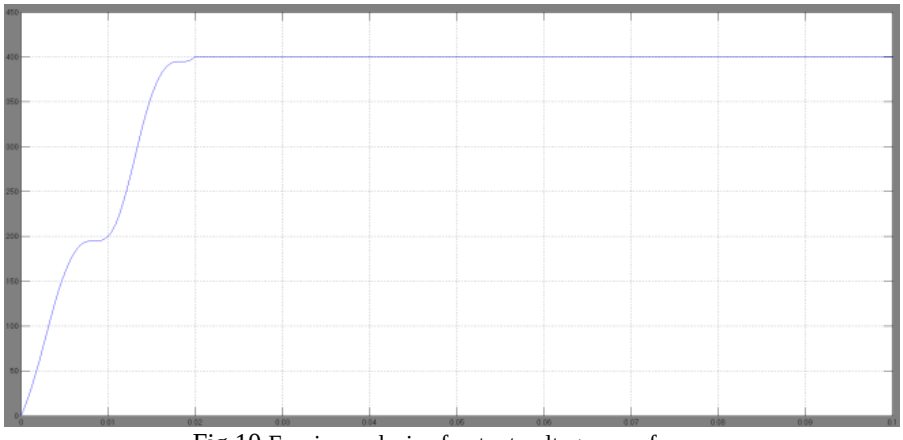

Fig.10 Fourier analysis of output voltage waveforms

MATLAB Simulation result of seven-and Nine-level fed PMSM for output Rotor speed, Electromagnetic torque, stator voltage, stator current, Rotor angle, Phase voltage are shown in Fig.8 and Fig.9. The THD is 10.1for Seven level and 7.2 for Nine level hence input voltage quality of PMSM is improved and Torque ripples are reduced it can be observed in above figures.

VI. CONCLUSION

Using MCSPWM, three phase AC waveform is obtained from single phase AC supply. The output voltage is about 600 V with minimum THD. The output voltage is having less THD, improved voltage quality and less Torque ripple with Nine-level is comparing to seven-level asymmetric cascaded H bridge inverter .

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