A New Reverse Voltage (RV) Topology for Multi Level Inverters Fed to Induction Motor Drive

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***Abstract*— In this paper A new topology with a reversing-voltage component is proposed which will improve the multilevel performance by compensating the disadvantages of increased number of components, complex pulse width modulation control method, and voltage-balancing problem. This topology requires fewer components compared to existing inverter Topologies (particularly in higher levels) and requires fewer carrier signals and gate drives. Therefore, the overall cost and complexity are greatly reduced particularly for higher output voltage levels. The simulation results are provided for 7-level and 9-level RV-Topology with In-Phase Disposition (IPD) and Alternate Phase Opposition Disposition (APOD) Sinusoidal Pulse Width Modulation (SPWM) Schemes, three phase induction motor employing nine level reverse voltage multilevel inverter is also presented and the THD performance of 7-level RV-Topology is compared with Two popular Multi Level Inverter Topologies Diode Clamped(DC) and Cascaded H-Bridge (CHB) Inverter by using Multi Carrier SPWM Techniques.**

Keywords- Multi Level Invertr (MLI), Cascaded H-Bridge (CHB) Inverter, Diode Clamped MLI, Multi Carrier Sine PWM, Reverse Voltage Topology, Multi carrier Sine PWM Techniques.

1. INTRODUCTION

In recent years, industry has begun to demand higher power conversion equipment, which now reaches the megawatt level. Controlled ac drives in the megawatt range are usually connected to the medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids (2.3, 3.3, 4.16, or 6.9 kV). For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels.

Several topologies of multi-level inverter system have been introduced in the recent past [1]. The main topologies are diode clamped inverter system [3], flying capacitor inverter system [4], [5] and Cascaded H-bridge inverter system [7], [8] in order to generate a high voltage waveform using low voltage devices. Each of these topologies has a different mechanism for providing the required voltage levels. But the number of main switches of each topology is equal. Comparing with respect to the other components, for instance, DC-link capacitors having the same capacity per unit, diode clamped inverter has the least number of capacitors among the various multi-level inverter system topologies but requires additional clamping diodes. Flying capacitor inverters have the largest number of capacitors required but need no clamping diode. H bridge inverters require isolated voltage sources but need no clamping diodes. The most attractive features of multilevel inverters are as follows.

1) They can generate output voltages with extremely low distortion and lower dv/dt.

2) They draw input current with very low distortion.

3) They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated.

4) They can operate with a lower switching frequency.

One clear disadvantage of the multilevel power conversion is higher number of semiconductor switches are required. It should be pointed out that lower voltage rated switches can be used in the multilevel converter and, therefore, the active semiconductor cost is not appreciably increased when compared with the two level cases. However, each active semiconductor added requires associated gate drive circuits and adds further complexity to the converter mechanical layout. Another disadvantage of multilevel power converters is that the small voltage steps are typically produced by isolated voltage sources or a bank of series capacitors. Isolated voltage sources may not always be readily available, and series capacitors require voltage balancing. To some extent, the voltage balancing can be addressed by using redundant switching states, which exist due to the high number of semiconductor devices. However, for a complete solution to the voltage-balancing problem, another multilevel converter may be required.

The Reversing Voltage is proposed to improve the multi-level performance by compensating the above mentioned disadvantages. Especially at higher levels this topology requires less number of components as compared to available inverters. This topology requires less carrier signals and does not need balancing of the voltages.

This paper describes the general multilevel inverter schematic. A general method of multilevel modulation phase disposition (PD) SPWM is utilized to drive the inverter and can be extended to any number of voltage levels. The

simulation and experimental results of the proposed topology are also presented.

I. NEW RV TOPOLOGY

A. General Description

In conventional multilevel inverters, the power semiconductor switches are combined to produce a high-frequency waveform in positive and negative polarities. However, there is no need to utilize all the switches for generating bipolar levels. This idea has been put into practice by the new topology.

This topology is a hybrid multilevel topology which separates the output voltage into two parts. One part is named **level generation** part and is responsible for level generating in positive polarity. This part requires high-frequency switches to generate the required levels. The switches in this part should have high-switching-frequency capability.

The other part is called **polarity generation** part and is responsible for generating the polarity of the output voltage, which is the low-frequency part operating at line frequency.

The topology combines the two parts (high frequency and low frequency) to generate the multilevel voltage output. In order to generate a complete multilevel output, the positive levels are generated by the high-frequency part (level generation), and then, this part is fed to a full-bridge inverter (polarity generation), which will generate the required polarity for the output. This will eliminate many of the semiconductor switches which were responsible to generate the output voltage levels in positive and negative polarities with high switching frequency.

The schematic block diagram of Reversing Voltage topology for multi-level inverter is depicted in fig. 1. The principle idea of this topology as a multi-level inverter is that the left side stage in fig. 2 (i.e., positive level generator of fig. 2) generates the required positive levels and the right side circuit of fig. 2 (i.e., full bridge converter of fig. 2) reverses the voltage direction when the voltage polarity requires to be changed for negative polarity (negative half cycle of the fundamental output voltage).

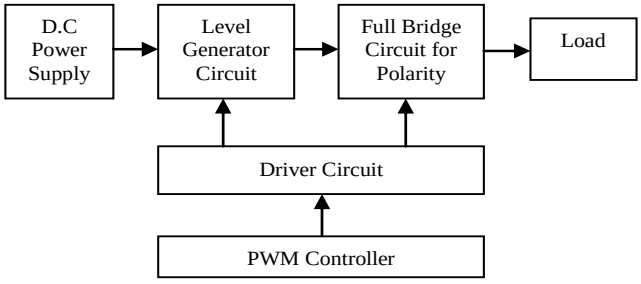


Fig. 1. Block diagram of multi level inverter using RV Topology

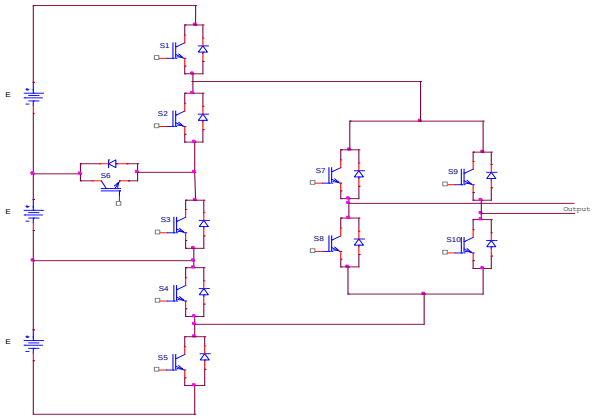


Fig. 2. Schematic of single phase 7-level inverter with RV Topology

This topology easily extends to higher voltage levels by duplicating the middle stage as shown in Fig. 2. Therefore, this topology is modular and can be easily implemented to higher voltage levels by adding the middle stage in Fig. 2. The Schematic of single phase 9-level inverter is shown in Fig. 3.

This topology requires fewer components in comparison to conventional inverters. Another advantage of the topology is that it just requires half of the conventional carriers for SPWM controller. SPWM for seven-level conventional converters consists of six carriers, but in this topology, three carriers are sufficient.

The reason is that, according to Fig. 2, the multilevel converter works only in positive polarity and does not generate negative polarities.

Therefore, it implements the multilevel inverter with a reduced number of carriers, which is a great achievement for inverter control. It is also comparable to single-carrier modulation, while this topology requires the same number of signals for PWM. However, this topology needs one modulation signal which is easier to generate as opposed to the single-carrier modulation method which needs several modulation signals. Another disadvantage of this topology is that all switches should be selected from fast switches, while the proposed topology does not need fast switches for the polarity generation part.

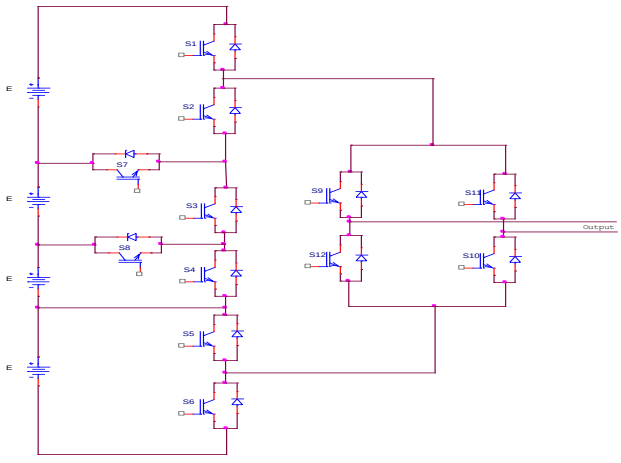


Fig. 3. Schematic of single phase 9-level inverter with RV Topology

B. Switching Sequences

Switching sequences in this converter are easier than its counter parts. According to its inherent advantages, it does not need to generate negative pulses for negative cycle control. Thus, there is no need for extra conditions for controlling the negative voltage. Instead, the reversing full-bridge converter performs this task, and the required level is produced by the high-switching-frequency component of the inverter. Then, this level is translated to negative or positive according to output voltage requirements.

This topology is redundant and flexible in the switching sequence. Different switching modes in generating the required levels for a seven-level RV inverter are shown in Table I.

TABLE I

SWITCHING SEQUENCES FOR EACH LEVEL

Levels / Mode	0	E	2E	3E
Mode 1	2,3,4	2,3,5	1,4	1,5
Mode 2		2,4,6	2,6,5	

In Table I, the numbers show the switch according to Fig. 2 which should be turned on to generate the required voltage level. According to the table, there are six possible switching patterns to control the inverter. It shows the great redundancy of the topology. However, as the dc sources are externally adjustable sources (dc power supplies), there is no need for voltage balancing for this work.

In order to avoid unwanted voltage levels during switching cycles, the switching modes should be selected so that the switching transitions become minimal during each mode transfer. This will also help to decrease switching power dissipation.

According to the aforementioned suggestions, the sequences of switches (2–3-4), (2-3-5), (2-6-5), and (1, 5) are chosen for levels 0 up to 3, respectively.

In order to produce seven levels by SPWM, three saw-tooth waveforms for carrier and a sinusoidal reference signal for modulator are required as shown in Fig. 4 and Fig. 9.

In this paper, In-Phase Disposition (IPD) and Alternate Phase Opposition (APOD) SPWM Schemes are adopted. Carriers in Phase Disposition Sine PWM methods do not have any coincidence, and they have definite offset from each other, and in IPD-SPWM Scheme Carriers are in phase with each other and in APOD-SPWM Scheme carrier are out off phase with each other. The modulator and three carriers for Seven-Level Sine PWM Schemes are shown in Fig. 4 and Fig. 9 for IPD and APOD SPWM Schemes respectively. The carriers for 9-level RV Topology and the corresponding pulses are shown in Fig.12 and Fig.13 respectively.

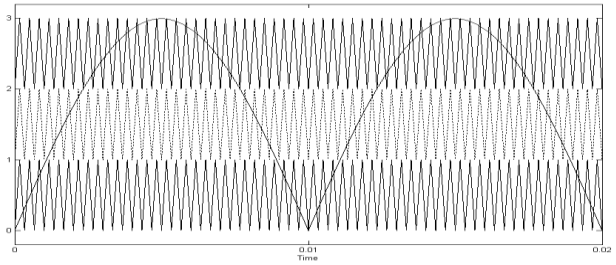


Fig. 4. PD-SPWM carrier and modulator for RV topology

According to Fig. 4 and Fig. 9, three states are considered. The first state is when the modulator signal is within the lowest carrier. The second state is when it is within the middle carrier. Finally, the third one is when it is within the highest carrier. In each state, certain switching patterns are adopted to cover the voltage requirements. According to this definition, the switching states and switching modes are described in Table II.

TABLE II

SWITCHING CASES IN EACH STATE ACCORDING TO RELATED COMPARATOR OUTPUT

States	One		Two		Three	
Compare	+	-	+	-	+	-
Mode	2,3,5	2,3,4	2,5,6	2,3,5	1,5	2,5,6

Table II shows the relation between the right comparator output according to the current state and required states for switching to meet the voltage requirements. The right comparator here refers to the comparator output of the current state. As illustrated in Table II, the transition between modes in each state requires minimum commutation of switches to improve the efficiency of the inverter during switching states.

The number of switches in the path of conducting current also plays an important role in the efficiency of overall converter.

For example, a seven-level cascade topology [8], [9] has 12 switches, and half of them, i.e., six switches, conduct the inverter current in each instance. However, the number of switches which conduct current in the proposed topology ranges from four switches (for generating level 3) to five switches conducting for other levels, while two of the switches are from the low-frequency (polarity generation) component of the inverter.

Therefore, the number of switches in the proposed topology that conduct the circuit current is lower than that of the cascade [8] inverter, and hence, it has a better efficiency.

These switching sequences can be implemented by logic gates or DSP. The signal stage should be isolated from the power stage by opto couplers for control circuit protection.

The drive circuit is also responsible to generate the dead time between each successive switching cycle across the dc source.

The gating signal for the output stage, which changes the polarity of the voltage, is simple. Low-frequency output stage is an H-bridge inverter and works in two modes: forward and reverse modes. In the forward mode, switches 7 and 10 as in Fig. 2 conduct, and the output voltage polarity is positive.

However, switches 8 and 9 conduct in reverse mode, which will lead to negative voltage polarity in the output. Thus, the low-frequency polarity generation stage only determines the output polarity and is synchronous with the line frequency.

The resulting PWM waveforms for driving the high frequency switches in the level generation part are illustrated for one complete cycle in Fig. 6 for 7-Level Inverter, and are shown in Fig. 13 for 9-level Inverter by using IPD-SPWM. According to Fig. 6 and Fig. 13, high frequency switches can be adopted in this stage based on the required frequency and voltage level.

However, low-frequency polarity generation part drive signals are generated with the line frequency (50 Hz), and they only change at zero-voltage crossings.

The level generator output voltage waveform with IPD-SPWM is shown in Fig. 7, and the simulated phase and line voltages and respective Harmonic Spectrum of RV-topology with IPD-SPWM is shown in Fig. 8 and with APOD-SPWM is shown in Fig.10 for seven levels, and The level generator output voltage waveform with IPD-SPWM is shown in Fig. 14 , Simulated Waveforms for a nine-level Inverter using IPD-PWM (RV-Topology) in Fig. 15 and with APOD-SPWM for 9-level Inverters is shown in Fig.16.

III.MATLAB MODELING AND SIMULATION RESULTS

Case1: Proposed Single Phase Multilevel Inverter Topology (seven level):

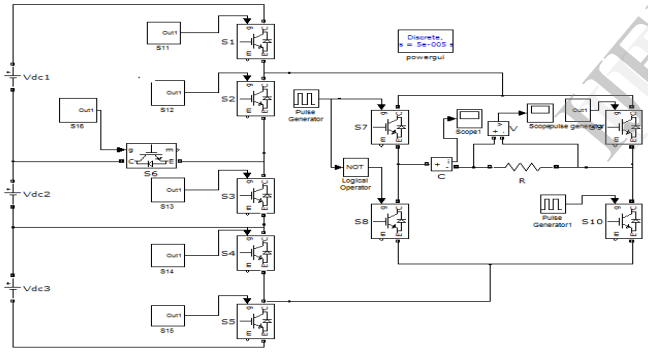


Fig. 5. Matlab/Simulink model for a seven-level RV Topology

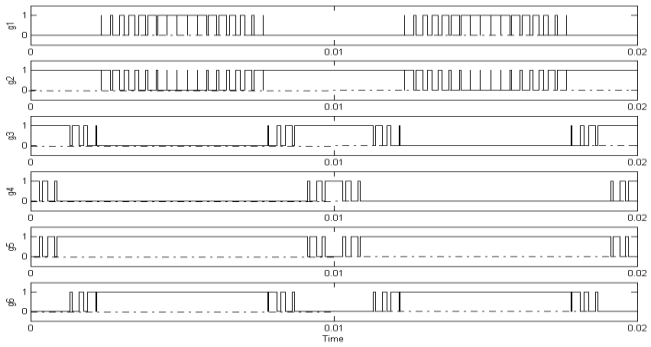


Fig. 6. Gate signals for Level generation part using IPD-PWM

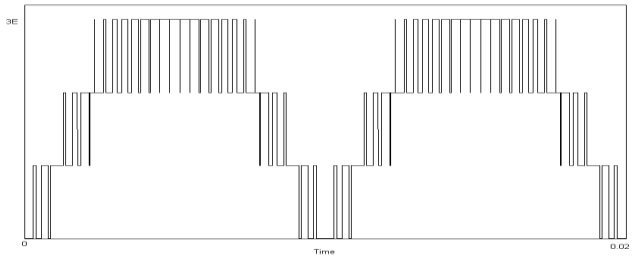
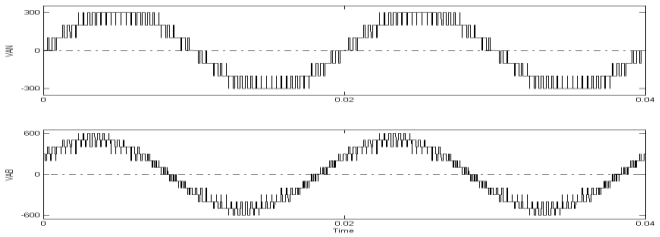
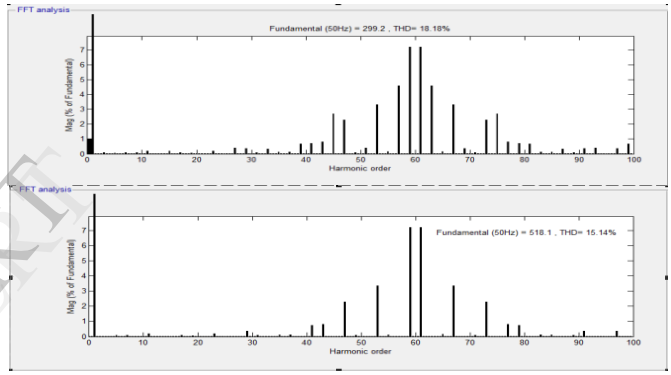


Fig.7. Level generator output voltage waveform using IPD-PWM



a) Waveforms



b) Harmonic Spectrum

Fig. 8. Simulated Waveforms for a seven-level Inverter using IPD-PWM (RV-Topology)

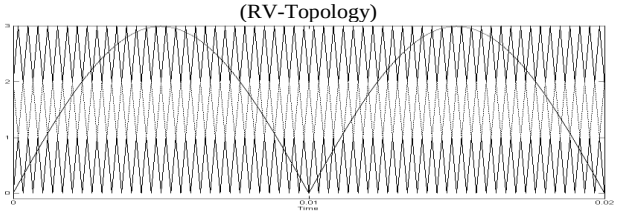
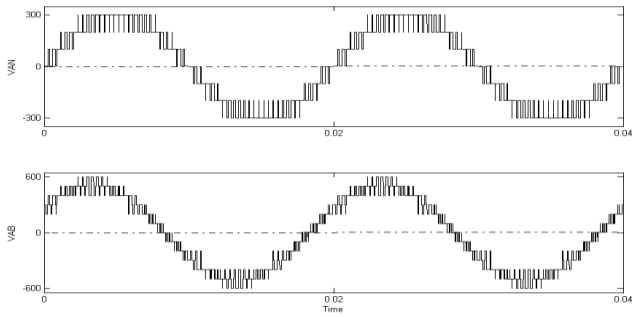
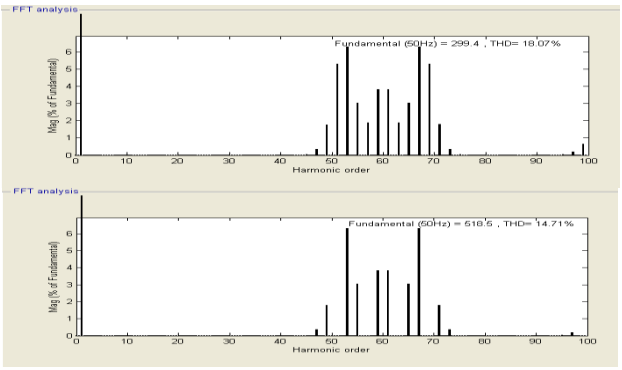


Fig. 9. APOD-SPWM carrier and modulator for seven levels



a).Waveforms



b).Harmonic Spectrum

Fig. 10. Simulated Waveforms for a seven-level Inverter using APOD-PWM (RV-Topology)

Case2: proposed Single Phase Multilevel Inverter Topology (nine levels):

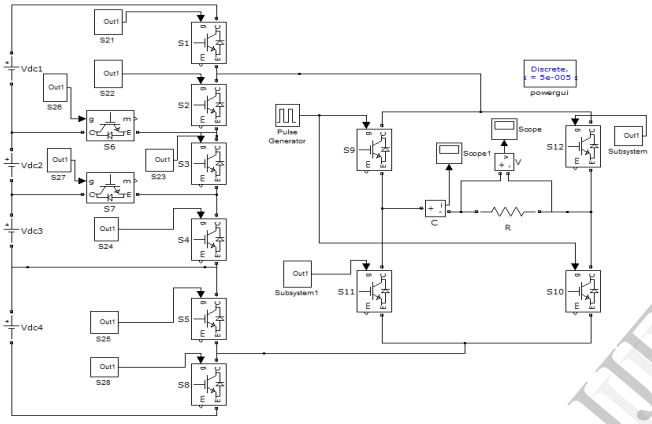


Fig. 11. Matlab/Simulink model for a nine-level RV Topology

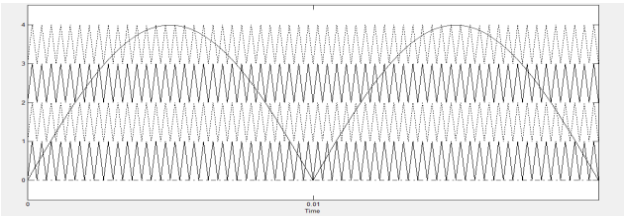


Fig. 12. IPD-SPWM carrier and modulator for RV topology for 9-level Inverter

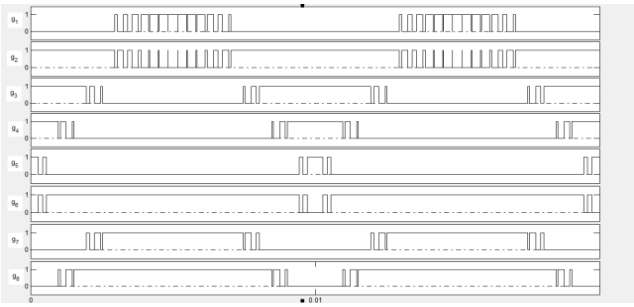


Fig. 13. Gate signals for Level generation part using IPD-PWM for 9-Level Inverter

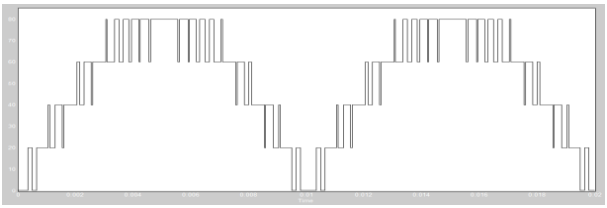
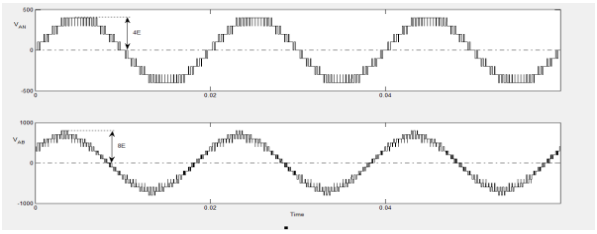
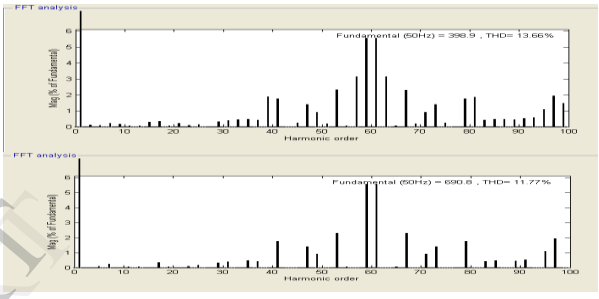


Fig. 14. Level generator output voltage waveform (nine-levels) using IPD-PWM

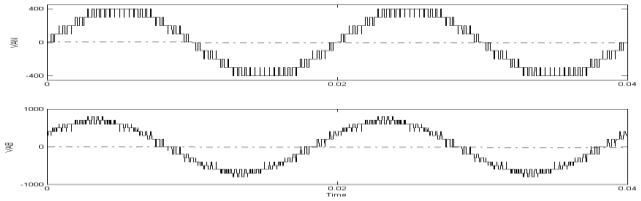


a) Waveforms

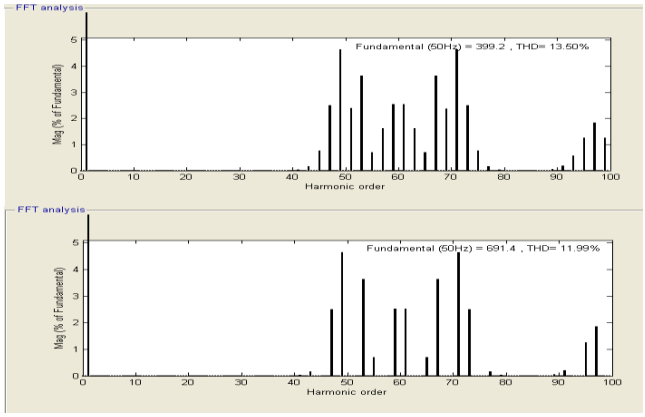


b) Harmonic Spectrum

Fig. 15. Simulated Waveforms for a nine-level Inverter using IPD-PWM (RV-Topology)



a) waveforms



b) Harmonic Spectrum

Fig. 16. Simulated Waveforms for a 9-level Inverter using APOD-PWM (RV-Topology)

Case 3: Proposed Three Phase Multilevel Inverter Topology applied to R-load (nine levels):

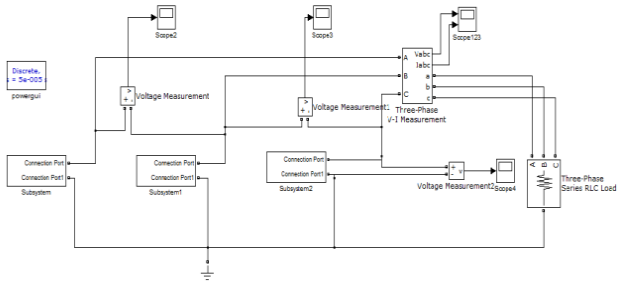


Fig. 17. Matlab/Simulink model of Three Phase RV Topology based Multilevel Inverter with R-load.

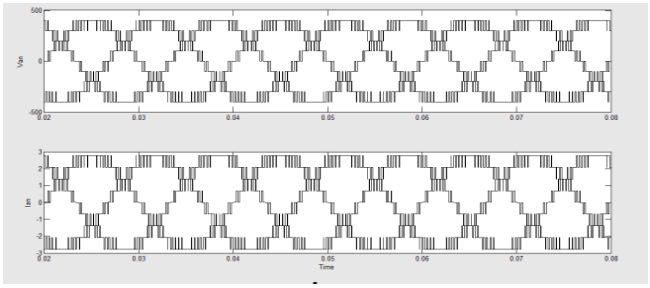


Fig. 18. Output phase voltage and current for R-load

Case 4: Proposed Three Phase Multilevel Inverter Topology applied to induction motor drive (nine levels):

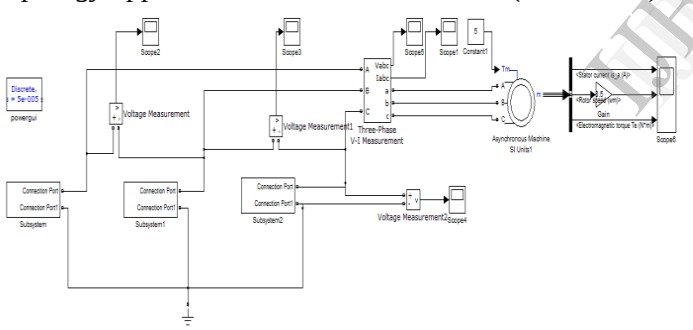


Fig. 19. Matlab/Simulink model for a three phase nine-level RV Topology with Induction Motor

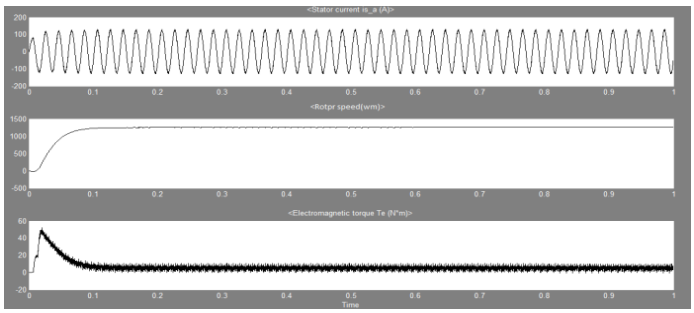


Fig. 20. Output stator current, Speed and Electromagnetic Torque waveforms

C. *Number of Components*

As mentioned earlier, one of the promising advantages of the topology is that it requires less high-switching-frequency components. High-frequency switches and diodes are expensive and are more prone to be damaged than low-frequency switches.

According to the MIL-HDBK-217F standard, the reliability of a system is indirectly proportional to the number of its components. Therefore, as the number of high-frequency switches is increased, the reliability of the converter is decreased. In the proposed converter, as can be seen, half of the switches in the full-bridge converter will not require to be switched on rapidly since they are only switched at zero crossings operating at line frequency (50 Hz). Thus, in this case, the reliability of the converter and also related expenses are highly improved.

The number of required three-phase components according to output voltage levels (N) is illustrated in Table III. It can clearly be inferred that the number of components of the proposed topology is lower than that of other topologies even more so as the voltage levels increase and it will decrease tremendously with higher voltage levels.

Fig.21 shows the required components versus different voltage levels as mentioned in Table III.

As the most important part in multilevel inverters is the power semiconductor switches which define the reliability and control complexity, the number of required switches against the required voltage levels is shown in Fig.22 for the new topology as well as other topologies.

TABLE III

NUMBER OF COMPONENTS FOR THREE PHASE INVERTERS

Inverter Type	NPC	Flying capacitor	Cascade	RV
Main Switches	$6(N-1)$	$6(N-1)$	$6(N-1)$	$3((N-1)+4)$
Main diodes	$6(N-1)$	$6(N-1)$	$6(N-1)$	$3((N-1)+4)$
Clamping Diodes	$3(N-1)(N-2)$	0	0	0
D.C bus Capacitors/ Isolated power Supplies	$3(N-1)$	$3(N-1)$	$3(N-1)/2$	$(N-1)/2$
Flying Capacitors	0	$3(N-1)(N-2)/2$	0	0
Total Numbers	$3(N-1)(N+3)$	$3(N-1)(N+8)/2$	$27(N-1)/2$	$(13N+35)/2$

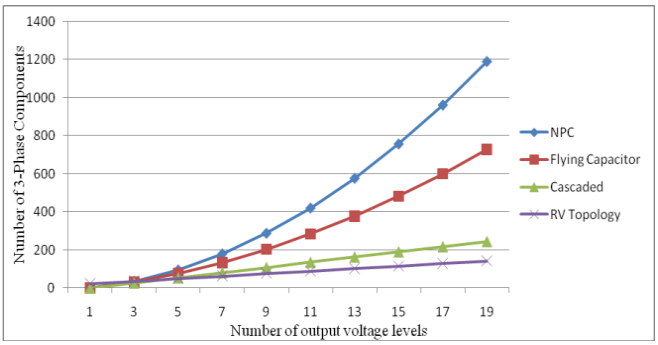


Fig. 21. Required components for Multi-Level inverters in different topologies

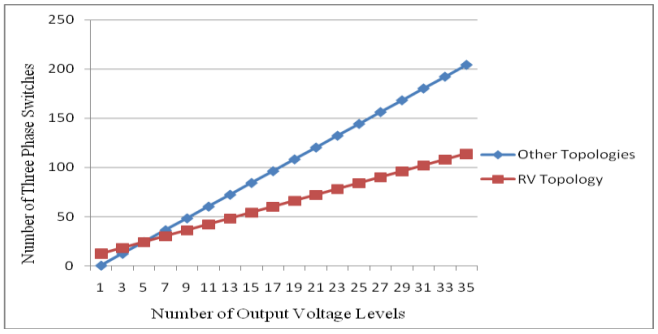


Fig. 22. Required Switches for Multi- Level Inverter in Different Topologies

TABLE IV

COMPARISON OF DC, CHB AND RV TOPOLOGIES FOR 7-LEVEL INVERTERS BY USING MULTICARRIER SINE PWM TECHNIQUES ($f_{sw,dev} = 500Hz$)

	Cascaded H-Bridge (CHB) Topology		Diode Clamped (DC)Topology		Reverse Voltage (RV) Topology	
	IPD PWM	APOD PWM	IPD PWM	APOD PWM	IPD PWM	APOD PWM
Number of Carriers	$(N-1)$	$(N-1)$	$(N-1)$	$(N-1)$	$\frac{(N-1)}{2}$	$\frac{(N-1)}{2}$
Phase Voltage THD	18.13%	17.96%	18.26%	18.13%	18.18%	18.07%
Line Voltage THD	10.68%	14.63%	10.71%	14.64%	15.14%	14.71%
Even Harmonics	Yes	No	Yes	No	No	No

II. CONCLUSIONS

In this paper, a Reversing Voltage topology is implemented, which has superior characteristics over traditional topologies in terms of required components as switches, control requirements and reliability. From Table IV it can be observed that the THD performance of Proposed Strategy is comparable to two popular MLI Inverter Topogies (DC and CHB), and the output of proposed RV topology does not contain any even harmonics in output phase and line voltages. The proposed topology is easily extended to higher level by duplicating the middle switch, and the implementation of this method is very simple. It is shown that this topology can be a good candidate for converters used in power applications such as FACTS, HVDC, PV systems, UPS, etc. In the mentioned topology, the switching operation is separated into high- and low- frequency parts. This will add up to the efficiency of the converter as well as reducing the size and cost of the final prototype. The IPD-SPWM and APOD-SPWM control methods are used to drive the inverter. The PWM for this topology has fewer complexities since it only generates positive carriers for PWM control.

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