A New Topology of Single Phase Multi-Levelinverter with Less Number of Switches

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Keywords **-** Multilevel inverter, multilevel converter, asymmetrical dc sources, bi-directional switch**,** harmonic cancellation, more output levels.

Abstract **-** Multilevel inverters have drawn tremendous interest in the power industry. It is easier to produce a high power, high voltage inverter with the multilevel structure because of the way in which device voltage stresses are controlled in the structure. Increasing the number of voltage levels in the inverter without requiring higher ratings on individual devices can increase the power rating with low harmonics. Conventional multilevel inverters, including diode-clamped, flying-capacitor, and cascaded H-bridge are well defined but become clumsy for higher levels. This paper proposes a new single phase full-bridge multilevel topology, which requires less split-rail dc sources and significantly reduced semiconductor switch devices.Cascading basic five-level cells provides another structure to build higher level inverters with separate dc sources. The proposed multilevel inverters can be potential for solar photovoltaic, energy storage applications and to run the single phase induction motor.

1. INTRODUCTION

Currently power industry has entered anew age with more and more renewable energy and highefficiencypower generations, transmissions, anddistributions, where multilevel power electronics canassume significant roles [1]. Multilevel power convertersemerged from the fact that single power semiconductorcannot meet the voltage requirements in medium-voltagepower conversion. The first multilevel power converterwas introduced by Nabae*et al*[2]. Since then, multilevelpower conversion has been rapidly growing in thefield of power engineering for the applications ofmedium-voltage ac drive, flexible ac transmission system(FACTS) devices, medium-voltage dc transmission(MVDC), and high-voltage dc transmission (HVDC)systems. Even when today's high power semiconductortechnology has reached around 6.5 kV and 2.5 kA powerrating, multilevel inverters with many advantages over the conventional two-level converters, due to their ability to synthesizewaveforms with lower distortion and better harmoniccancellation, smaller dv/dtand low switching frequency operation, and to attainhigher voltages using semiconductor devices with smaller with smaller voltage ratings.

Multilevel inverter is a large voltage synthesizer and requires multiple equal DC sources. The fundamental idea of multilevel inverters is to provide an ac output waveform that exhibits multiple steps at several voltage levels. More levels of output will generate more sinusoidal waveform and reduce the output filters. By optimizing the angles and heights of steps, lower order harmonics can be cancelled [3].

The well-known topologies are diode-clamped [4], capacitor clamped and cascaded H-bridge with separate dc inputs [5]. The other upcoming topologies include replacing the H-bridge with five-level inverters in a cascaded topology to reduce the number of dc sources, cascading two-terminal sub-modules without separate dc sources to form a modular structure as in Fig.1. The topology is well defined but cumbersome to implement for levels beyond five. So, we need to simplify the circuit topology to facilitate a higher level realization. This paper proposes a full bridge approach with bi-directional switching interconnections as shown in Fig.2. With the proposed change, conventional single- phase bridge inverter will become five-level inverter.

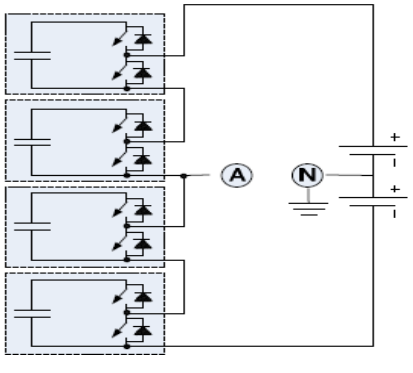


Fig.1. Modular five-level inverter topology

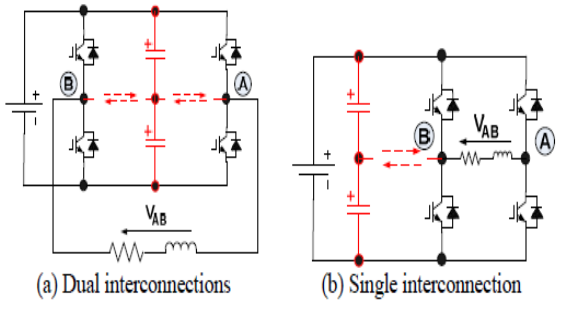


Fig.2. Proposed concept with bidirectional switching interconnections

The proposed paper will first present the topology and operation principle of a five-level inverter, and derive the topology with reduced number of switches. The seven and nine-level topologies are proposed and the method to minimize semiconductor devices is given.

2. PROPOSED SINGLE-PHASE FIVE-LEVEL INVERTER

Will take five-level full-bridge inverter, which is the lowest multilevel topology in the proposed concept.

(i) Topology Derivation

Consider the diode-clamped three-level inverter in Fig.3. Switch 1 and 2 is complementalto switch 3 and 4. Table.1. tells the basic switching scheme of three-level inverter. If we change the positions of the switches the rules are not violated.

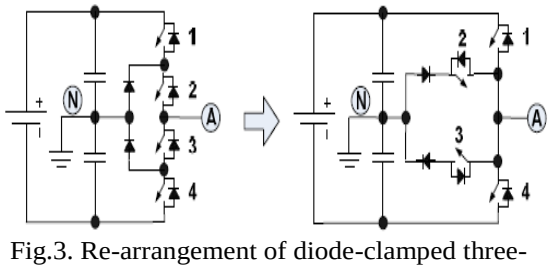


Fig.3. Re-arrangement of diode-clamped three-level inverter.

TABLE 1
BASIC SWITCHING SCHEME OFTHREE-LEVEL INVERTER

S_1	S_2	S_3	S_4	VAN
1	1	0	0	+½V
0	1	1	0	0
0	0	1	1	-½V

Now if add the other half bridge it will form a full-bridge topology and we should replace the paths with bidirectional switches 5 and 6 as shown in Fig.4. The so obtained topology becomes a five-level inverter with ac output at A and B terminals.

The proposed topology consists of four bi-directional switches and two bi-directional switches. The number of semiconductor devices used is same as the conventional method except the grounding point, because zero level is obtained not by clamping the neutral.

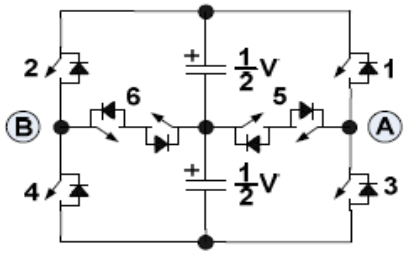


Fig.4. Proposed single-phase five-level inverter topology

(ii) Principle of operation

Some precautions to be taken to avoid short circuit of split-rail dc sources, the following conditions to be imposed into the power switching scheme:

$S_1$and S_3 cannot be turned on simultaneously;
S_1 and S_5 cannot be turned on simultaneously;
S_3 and S_5 cannot be turned on simultaneously;
S_2 and S_4 cannot be turned on simultaneously;
S_2 and S_6 cannot be turned on simultaneously;
S_4 and S_6 cannot be turned on simultaneously;

Table.2. Gives switching table of the five-level inverter topology.

TABLE 2
POWER SWITCHING OF FIVE-LEVEL INVETER TOPOLOGY

V_A	V	V_{AB}	S_1	S_2	S_3	S_4	S_5	S_6
+½V	-½V	+V	1	0	0	1	0	0
+½V	0	+½V	1	0	0	0	0	1
0	-½V		0	0	0	1	1	0
+½V	+½V	0	1	1	0	0	0	0
0	0		0	0	0	0	1	1
-½V	-½V		0	0	1	1	0	0
-½V	0	-½V	0	1	0	0	1	0
0	+½V		0	0	1	0	0	1
-½V	+½V	-V	0	1	1	0	0	0

It can be observed from the table that at any given instant only two switches are required to close to get a required voltage level.

(iii) Reduction of switches

If we reduce the switches from Fig.3. We can build a five-level inverter with less count of switches as shown in the Fig.5. The new five-level topology now has only six semiconductor switches. By removing one bi-directional switch we can still achieve the same level output. The corresponding table for reduced number of switches is given in the Table.3.

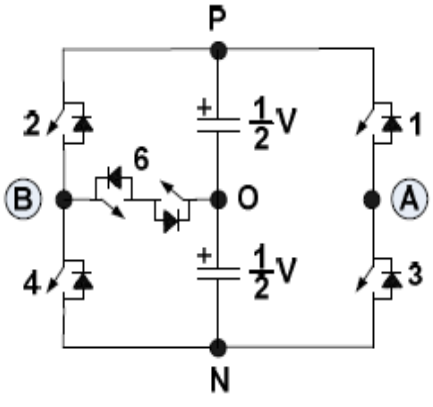


Fig.5. Proposed single-phase five-level inverter with reduced switches

TABLE 3

REDUCED SWITCHING OPTIONSFOR FIVE-LEVEL INVERTER

State	VAB	ON-State Switches
1	+V	1&4
2	+½V	1&6
3&4	0	1&2 or 3&4
5	-½V	3&6
6	-V	3&2

The switching schemes for the reduced number of switches are demonstrated in the Fig.6.

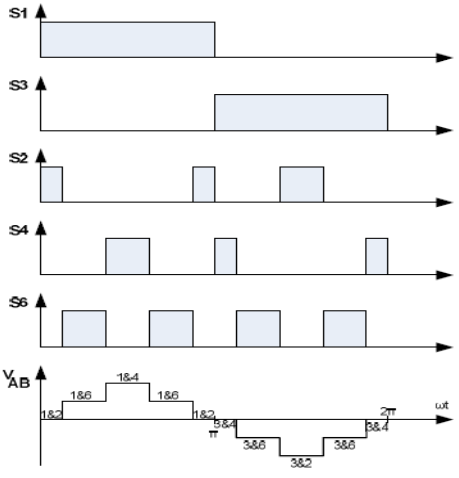


Fig.6. Switching scheme of reduced switches

(iv) Method used to generate the ac waveform

The method used to generate the required ac waveform is by taking the pulses generated by each switch and giving those pulses to the switches considering the delay of each switch. Table.4. tells the full detailed explanation of the pulse generation:

TABLE 4

PULSE GENERATION OF THE SWITCHES

Switches	No. of PG	Delay	Pulse Width
S1	PG1	0	(100/8)*5
S2	PG1	0	(100/8)*1
	PG2	(0.02/8)*4	(100/8)*1
	PG3	(0.02/8)*6	(100/8)*1
S3	PG	(0.02/8)*5	(100/8)*3
S4	PG	(0.02/8)*2	(100/8)*1
S5	PG1	(0.02/8)*1	(100/8)*1
	PG2	(0.02/8)*3	(100/8)*1
	PG3	(0.02/8)*5	(100/8)*1
	PG4	(0.02/8)*7	(100/8)*1
S6	PG1	(0.02/8)*1	(100/8)*1
	PG2	(0.02/8)*3	(100/8)*1
	PG3	(0.02/8)*5	(100/8)*1
	PG4	(0.02/8)*7	(100/8)*1

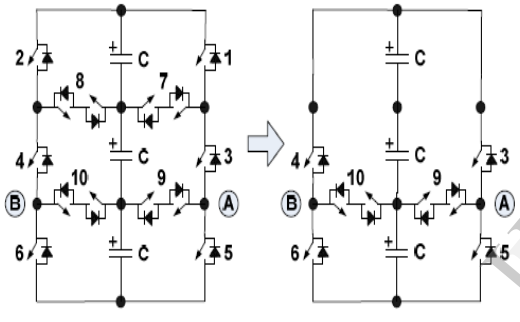
(*) PG-PULSE GENERATOR

3. EXPANSIONS TO NEW MULTI-LEVEL INVERTERS

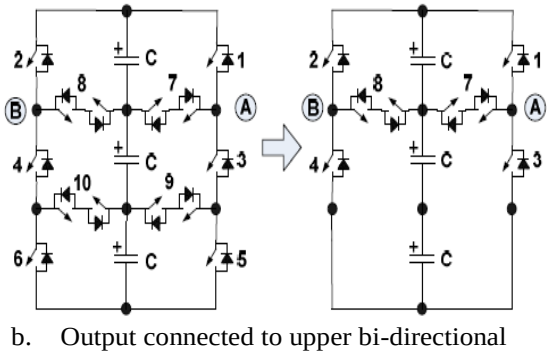
We can increase the output levels byadding new split-rail dc sources andnew bi-directional switching interconnections. Will introduce both full and reduced topologies for seven and nine-level inverters.

(i) Seven-Level Inverter Topology

The seven-level inverter has three dc sources and 14 semiconductor switches as shown in the Fig.7. The output can be connected across either the lower or upper bi-directional interconnection. For the instance, there are 4 ways to achieve 0V, 3 ways for ⅓ or -⅓V, 2 ways for 2 ⅔V or -⅔V, 1 way for V or –V voltage level. To reduce the voltage stress the circuit switches can be reduced still to 8. The switching table for seven-level inverter is given in the Table.5.



a. Output connected to lower bi-directional interconnection



b. Output connected to upper bi-directional interconnection

Fig.7. Seven-level single-phase inverter topologies

TABLE 5

SEVEN-LEVEL SWITCHING OPTIONS

Voltage	Turn-on switches				
	Full				Reduced
+V	1,4,6				1,4
-V	2,3,5				2,3
+⅔V	1,4,10	7,4,6			7,4
-⅔V	2,3,9	8,3,5			8,3
+⅓V	1,8	7,4,10	9,3,4,6		1,8
-⅓V	2,7	8,3,9	10,4,3,5		2,7
0	1,2	7,8	9,3,4,10	5,3,4,6	1,2/7,8/3,4

*(ii)Higher-Level Inverter Topologies*Anine-level inverter with full version and one of the reduced version is given in the Fig.8.

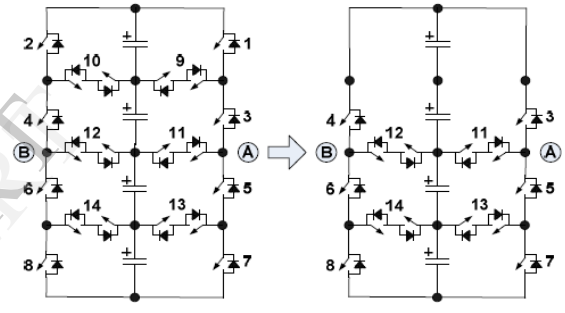


Fig.8. Nine-Level Single Phase inverter topologies.

(iii)Comparisons with the conventional topologies

Table. 6 and 7 gives the comparison between the proposed multilevel topologies and the conventional multilevel topologies.

TABLE 6

COMPARISON OF MAIN SWITCHING DEVICES PER PHASE

L	Equal DC Bus Caps	Proposed Topology		Existing Topologies
		Full	Reduced	
3	1	4	4	4
5	2	8	6	8
7	3	14	8	12
9	4	20	14	16
11	5	26	14	20
13	6	32	20	24
15	7	38	20	28
…	…	…	…	…
m	$\frac{m-1}{2}$	*for* $m \geq 5$, $2(m-1)+(m-5)$	*for m=7, 11, 15, …* $2(m-1)-\frac{m-5}{2}-3$ *for m=9, 13, 17, …* $2(m-1)-\frac{m-5}{2}$	$2(m-1)$

TABLE 7

COMPARISON OF OTHER POWER COMPONENTS PER PHASE

	Proposed Topology	Diode Clamped	Flying Capacitors	Cascade
DC-Bus Capacitors	$\frac{m-1}{2}$	$\frac{m-1}{2}$ or $m-1$ (*)	$\frac{m-1}{2}$ or $m-1$ (*)	$\frac{m-1}{2}$
Clamping Diodes	0	*(m-1)(m-2)*	0	0
Balancing Capacitors	0	0	$\frac{(m-1)(m-2)}{2}$	0

(*) – Number of dc-bus capacitors for half-bridge topologies.

From the above tables, it shows reduced version has a less power component number compared to the conventional multilevel topologies. Also with the less split-rail dc sources, the voltage stress of switches is higher compared to the same-level conventional topology.

4. OUTPUT RESULTS

The expected five-level output of the proposed topology and the pulses given to the switches are shown in the Fig.9 and 10.

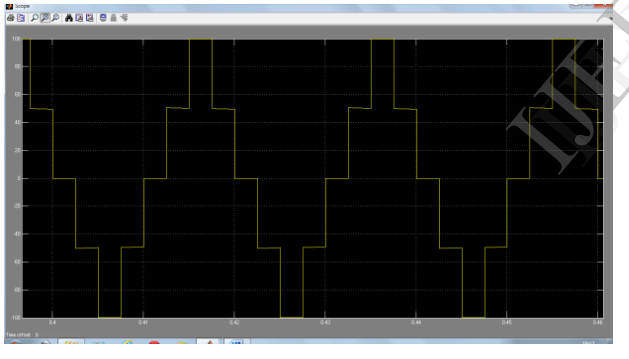


Fig.9. Expected output of the proposed topology

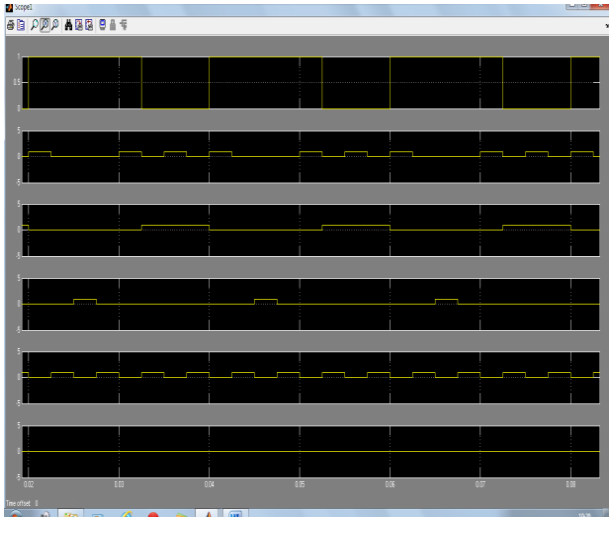


Fig.10. Switching pulses for each switch

5. CONCLUSIONS

A multilevel inverter can eliminate the need for the step-up transformer and reduce the harmonics produced by the inverter. A multilevel structure with more than three levels can significantly reduce the harmonic content [6]. The benefits of multilevel converter include lower-order harmonics cancellation, lower transient power loss due to low frequency switching, and reduced ac filters.

This paper proposed a multilevel inverter using a full-bridge approach with bidirectional interconnections. Comparing to well-known diode-clamped or flying capacitor multilevel topologies, the required power switch number can be largely reduced by removing redundant switching states. With asymmetrical dc inputs, the output levels can be significantly increased in the proposed generalised multilevel structure. This topology can be applied to solar photo-voltaic and energy storage applications.

6. REFERENCES

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