A Novel Approach in Fault Detection & Mitigation in Cascaded Converter STATCOMs

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Abstract: *At present, many transmission facilities confront one or more limiting network parameters plus the inability to direct power flow at will. In AC power systems given the insignificant electrical storage, the electrical generation and load must balance all times. To some extent, the electrical system is self regulating. If voltage is propped up with reactive power support, then the load will go up and consequently frequency will keep dropping and the system will collapse. Alternatively, if there is inadequate reactive power, the system can have voltage collapse. This problem can be overcome by using the FACTS controllers to control the interrelated parameters that govern the operation of transmission systems.STATCOMS is one of the FACTS controllers which have been well accepted as a power system controller for improving voltage regulation and reactive power compensation. This approach will be illustrated on an 11-level cascaded converter STATCOM. This paper introduces a novel approach to detect the existence of the faulted switch, identify which switch is faulty and reconfigure by mitigating the fault in cascaded STATCOMs (Static compensator) using proposed method and the effect on the dynamic performance and THD (Total Harmonic Distortion) analyzed using PSPWM (Phase shift pulse width modulation technique) technique .The approach has been validated on 115kv system with a STATCOM compensating the non linear load electric arc furnace.*

Keywords *- cascaded converter STATCOMs, Fault detection, mitigate*

I. INTRODUCTION

The static synchronous compensator (STATCOM) has been well accepted as a power system controller for improving voltage regulation and reactive compensation [1]. There are several compelling reasons to consider a multilevel converter topology for the STATCOM [2]. These well known reasons include the following: (1) lower harmonic injection into the power system; (2) decreased stress on the electronic components due to decreased voltages; and (3) lower switching losses. Various multilevel converters also readily lend themselves to a variety of PWM strategies to improve efficiency and control. An eleven-level cascaded multilevel STATCOM is shown in Figure 1. This converter uses several full bridges in series to synthesize staircase waveforms. Because every full bridge can have three output voltages with different switching combinations, the number of output voltage levels is $2n + 1$ where n is the number of full bridges in every phase. The converter cells are identical and therefore modular. As higher level converters are used for high output rating power applications, a large number of power switching devices will be used. Each of these devices is a potential failure point. Therefore, it is important to design a sophisticated control to produce a fault-tolerant STATCOM. A faulty power cell in a cascaded H-Bridge STATCOM can potentially cause switch modules to explode leading to the fault conditions such as a short circuit or an overvoltage on the power system resulting in an expensive down time[3]. Subsequently, it is crucial to identify the existence and location of the fault for it to be removed. A fault-tolerant neutral point-clamped converter was proposed in, a reconfiguration system based on bidirectional switches has been designed for three-phase asymmetric cascaded H-bridge inverters. In this paper, the methods propose requires only that the output dc link voltage of each phase be measured. This measurement is typically accomplished anyway for control purposes. If a fault is detected, the module in which the fault occurred is then isolated and removed from service. This approach is consistent with the modular design of cascaded converters in which the cells are designed to be interchangeable and rapidly removed and replaced. Until the module is replaced, the multilevel STATCOM continues to operate with slightly decreased, but still acceptable, performance.

In summary, this approach offers the following advantages:

• No additional sensing requirements;

• Additional hardware is limited to two by-pass switches per module;

•Is consistent with the modular approach of cascaded multilevel converters; and

• The dynamic performance and THD of the STATCOM is not significantly impacted.

A cascaded multilevel STATCOM contains several H-bridges in series to synthesize a staircase waveform. The inverter legs are identical and are therefore modular. In the eleven-level STATCOM, each leg has five H-bridges. Since each full bridge generates three different level voltages (*V*, 0, −*V)* under different switching states, the number of output voltage levels will be eleven. A multilevel configuration offers several advantages over other converter types.
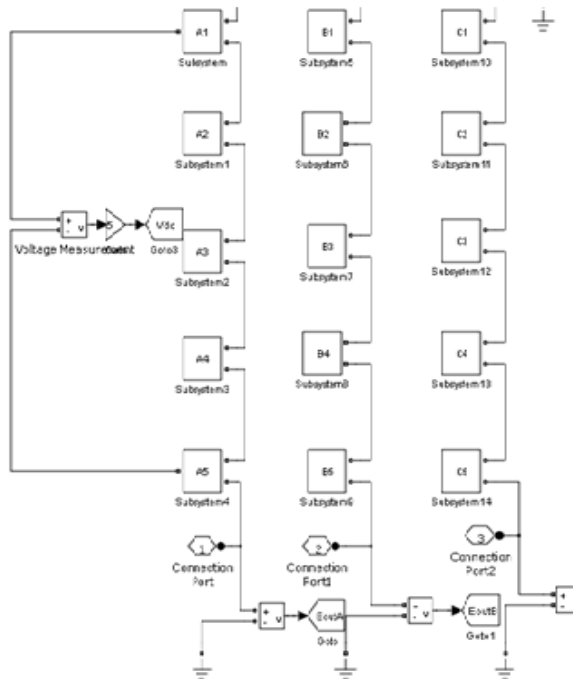

Figure 1. Eleven level cascaded multi level STATCOM

II.   MULTILEVEL STATCOM

(1) It is better suited for high-voltage, high-power applications than the conventional converters since the currents and voltages across the individual switching devices are smaller.

(2) It generates a multistep staircase voltage waveform approaching a more sinusoidal output voltage by increasing the number of levels.

(3) It has better dc voltage balancing, since each bridge has its own dc source.

To achieve a high-quality output voltage waveform, the voltages across all of the dc capacitors should maintain a constant value. Since there are multiple possible switching states that can be used to synthesize a given voltage level, the particular

switching topology is chosen such that the capacitors with the lowest voltages are charged or conversely, the capacitors with the highest voltages are discharged. This redundant state selection approach is used to maintain the total dc link voltage to a near constant value and each individual cell capacitor within a tight bound. Different pulse width modulation (PWM) techniques have been used to obtain the multilevel converter output voltage.
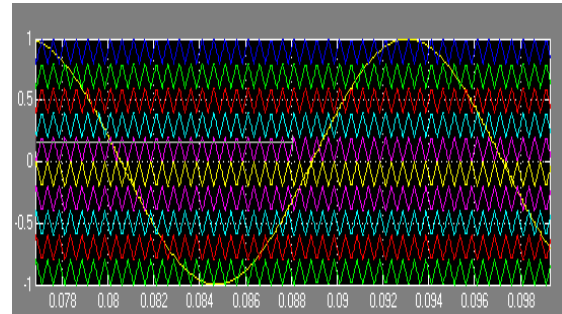

Figure 2. Carrier and reference waveform for PSPWM.

One common pulse width modulation (PWM) approach is the phase shift PWM (PSPWM) switching concept. The PSPWM strategy causes cancellation of all carrier and associated sideband harmonics up to the (N − 1) th carrier group for an N-level converter. Where N is the number of cells in each phase. Fig 2 illustrates the carrier and reference waveforms for a phase leg of the eleven-level STATCOM. In this figure, the carrier frequency has been decreased for better clarity. Normally, the carrier frequency for PWM is in the range of 1–10 kHz.

III.   FAULT ANALYSIS FOR THE MULTILEVEL STATCOM

A converter cell block, as shown in Fig. 3, can experience several types of faults. Each switch in the cell can fail in an open or closed state. The closed state is the most severe failure since it may lead to shoot through and short circuit the entire cell. An open circuit can be avoided by using a proper gate circuit to control the gate current of the switch during the failure. If a short circuit failure occurs, the capacitors will rapidly discharge through the conducting switch pair if no protective action is taken. Hence, the counterpart switch to the failed switch must be quickly turned off to avoid system collapse due to a sharp current surge. Nomenclature for the proposed method is given in table 1.

Table 1. Nomenclature

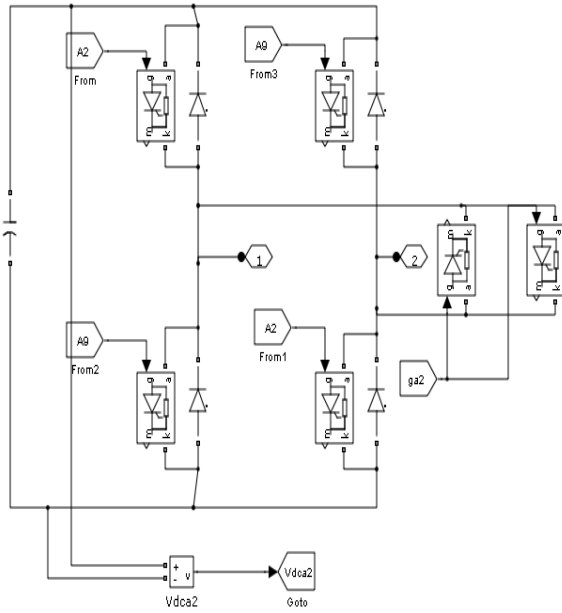|	
E_{out}	STATCOM output voltage (V)
$\hat{E}_{out}$	Filtered STATCOM output voltage (RMS) (V)
E'	STATCOM threshold voltage (constant) (V)
S_{j1}, S_{j2}	Switching signal of the j-th cell (0, 1)
f_i	possible STATCOM output voltage (V)
x_i	difference between possible and actual STATCOM output (V)
g_j	bypass signal for j-th cell (0, 1)

Figure 3. Cell with fault switch.

The staircase voltage waveform shown in Fig.2 synthesized by combining the voltages of the various cells into the desired level of output voltage. However, the peak voltages require that all cells contribute to the voltage; therefore, the short circuit failure of any one cell will lead to the loss of the first and $(2n + 1)$ output levels and cause degradation in the ability of the STATCOM to produce the full output voltage level.

Consider the simplified eleven-level converter shown in Fig.1. The process for identifying and removing the faulty Cell block is summarized in Fig. 4. The input to the detection algorithm is $\hat{E}_{out}$ for each phase, where $\hat{E}_{out}$ is the STATCOM filtered RMS output voltage. If the STATCOM RMS output voltage drops below a preset threshold value (E'), then, a fault is known to have occurred. Once a fault has been detected to have occurred, then the next step is to identify the faulty cell. By utilizing the switching signals in each converter cell, (i.e., S_1 and

S_2), it is possible to calculate all of the possible voltages that can be produced as show in table 2.

Table 2. Switching state and output voltage of a H-bridge

S_1	S_2	V_{ax}^+	V_{ax}^-	V_{ax}
0	0	0	0	0
0	1	0	V_{dc}	- V_{dc}
1	0	V_{dc}	0	V_{dc}
1	1	V_{dc}	V_{dc}	0

Thus, the output voltage of a cell is

$$v_{ax} = v_{ax} + -v_{ax}^- \qquad (1)$$

at any given instant as illustrated in Table 2.
And since the cells of the STATCOM are serially connected, the total output voltage per phase is

$$V_{yo} = \sum_{X=1}^{n} v_{yx} \qquad y \in [a,b,c] \qquad (2)$$

Where n is the number of blocks.

By utilizing the switching signals in each converter cell, (i.e., $Sj1$ and $Sj2$, j is the cell number), it is possible to calculate all of the possible voltages that can be produced at any given instant. When there is a fault in the multilevel converter, the capacitor at the faulty block will rapidly discharge. This discharge results in a phase shift in the output ac voltage as well as a change in amplitude of voltage. The set of all possible phase fault voltages for an eleven-level converter is given by

$$f_1 = V_{dco} (S_{21} - S_{22} + S_{31} - S_{32} + S_{41} - S_{42} + S_{51} - S_{52})$$
(Cell 1 faulted)

$$f_2 = V_{dco} (S_{11} - S_{12} + S_{31} - S_{32} + S_{41} - S_{42} + S_{51} - S_{52})$$
(Cell 2 faulted)

$$\cdot$$
$$\cdot$$
$$\cdot$$

$$F_5 = V_{dco} (S_{11} - S_{12} + S_{21} - S_{22} + S_{31} - S_{32} + S_{41} - S_{42})$$
(Cell 5 faulted)

Or more succinctly as

$$F_i = V_{dco} \sum_{\substack{j=1 \\ j \neq i}}^{n} (S_{j1} - S_{j2}), \qquad I = 1,.....,n$$
(3)

Where V_{dc0} is the ideal voltage across a single cell block. If there is a faulted cell, only one f_i will be near the actual STATCOM output phase voltage E_{out}; all of the others will be too high. Therefore, to determine the location of the fault cell, each f_i is compared against E_{out} to yield

$$X_i = E_{out} - f_i , \qquad i = 1, ..., n \qquad (4)$$

The smallest xi indicates the location of the faulted block because this indicates the f_i which most closely predicts the actual E_{out}.
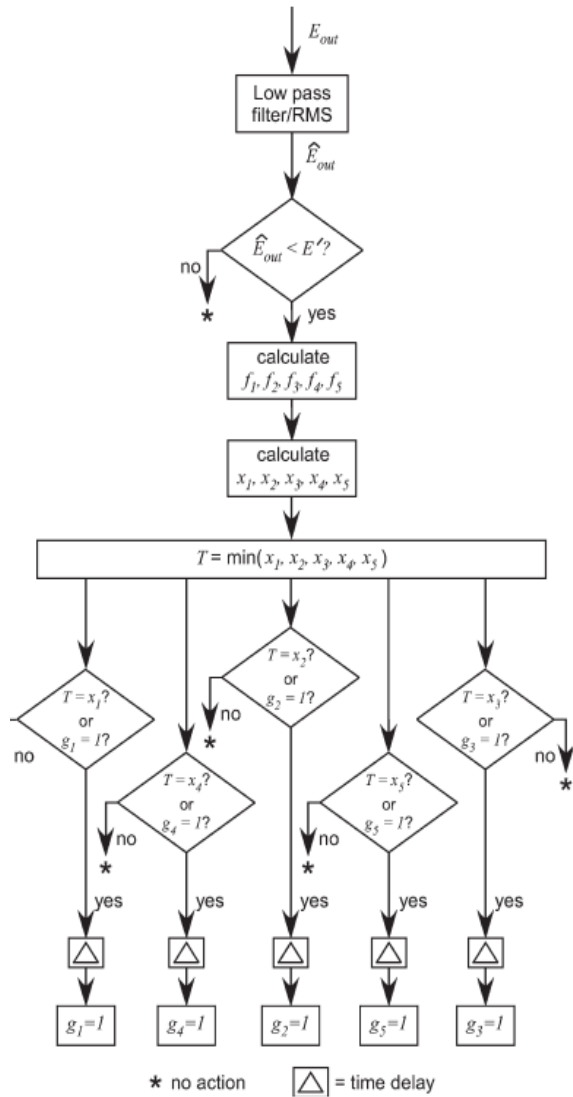

Figure 4. Flow chart for eleven level converter.

The choice of threshold voltage E' depends on the number of cells in the converter. The ideal output voltage is

$$\hat{E}_{out,\,0} = \frac{n\,V_{dco}}{\sqrt{2}} \tag{5}$$

During a fault, E_{out} will decrease by V_{dc0} yielding

$$\hat{E}_{out,fault} = \frac{(n-1)\,V_{dc0}}{\sqrt{2}} = \frac{n-1}{n}\,\hat{E}_{out},0. \tag{6}$$

Therefore, the threshold voltage E' should be chosen such that $(n - 1/n)\,E_{out,\,0} \leq E' \leq E_{out,\,0}$. In an eleven-level converter, $n = 5$ and the faulted RMS voltage

will decrease by roughly 20%. Therefore, a good choice for E' is 85% of the rated output STATCOM voltage.

The last step is to actuate the module bypass switch g_i shown in Fig. 3. A slight time delay is added to the logic to neglect for momentary spikes that may occur. It is desirable to neglect momentary sags in the dc link voltage, but respond to sags of increased duration that indicate a faulted module. Fig. 5 shows the realization logic for the proposed fault detection and module removal method. The use of a fault handling switch in multilevel converters is not uncommon. In, a fault handling switch is used in a flying capacitor multilevel inverter. While the additional circuitry does increase the cost of the circuit, it also increases the reliability be enabling the circuit to keep working (albeit at a slightly reduced operating range) until the module can be replaced.

IV. EXAMPLE AND RESULTS

The single line diagram of the electrical distribution system feeding an arc furnace is shown in Fig. 6. The STATCOM has been shown to be an efficient controller to mitigate arc furnace flicker [4]. The electrical network consists of a 115-kV generator and impedance that is equivalent to that of a large network at the point of common coupling (PCC). The STATCOM is connected to the system through a Y-Delta transformer. The system was
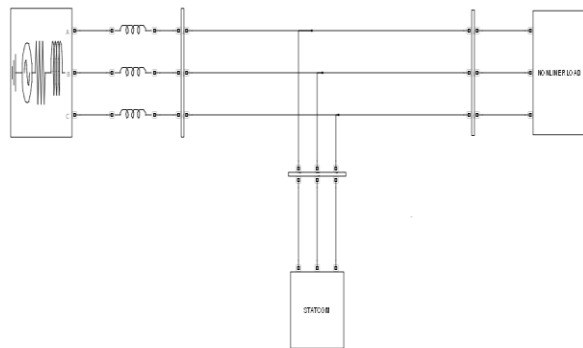

Figure 6. Single line diagram of arc furnace load.

Simulated using PSCAD/EMDTC. The electrical arc furnace load is nonsinusoidal, unbalanced, and randomly fluctuating. Electric arc furnaces are typically used to melt steel and will produce current harmonics that are random. In addition to the integer harmonics, arc furnace currents are rich in inter harmonics [5]. The flicker waveform has sub synchronous variations in the 5–35-Hz range [6]. Fig. 7 shows the active power drawn by the arc furnace. Note that the STATCOM is able to improve the line active power such that active power variations caused by the arc furnace do not propagate throughout the system as shown in Fig. 8.

The simulation model and control scheme is described in detail in [7]. The dc capacitor voltages normally vary and are kept in relative balance through redundant state selection .
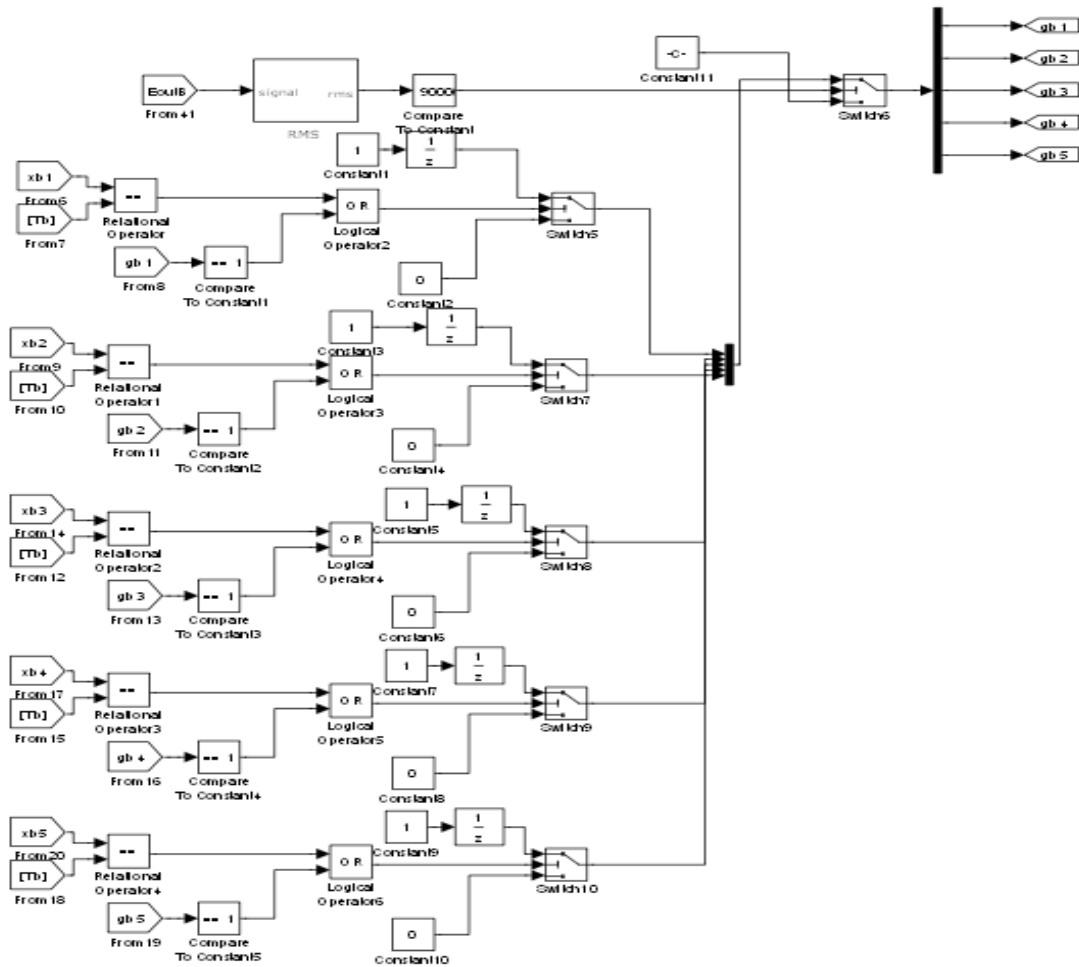

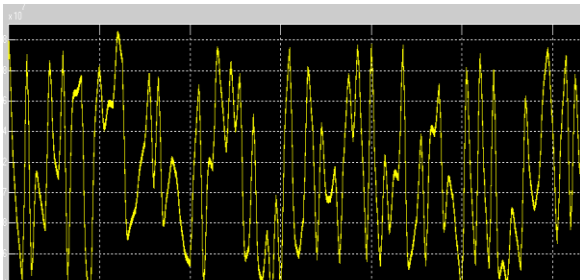Figure 5. Proposed fault detection and module removal

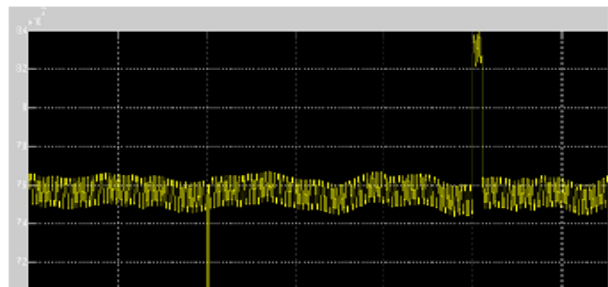Figure 6. Active power drawn by the arc furnace load

Figure 7.Line active power drawn by the arc furnace load

A. Dynamic Performance

To test the proposed fault detection and mitigation approach, a faulty switch was initiated at 2.5 s. Within 300 ms, the fault has been detected, the module removed, and the STATCOM restored to steady-state operation. This fault duration is longer than is necessary; the fault was intentionally left on to better illustrate its effect on the system and removal. The

STATCOM bus voltage and line and STATCOM active powers are shown before the fault, during, and after the faulty module is removed (Figs. 7 and 8). Note that both the bus voltage and line active power are adversely affected during the fault. In both cases, the high frequency oscillations are increased. Once the faulty module is removed, the system returns to its prefault behavior. There is a small induced low-frequency oscillation that can be observed in the line active power, but this is rapidly damped by the STATCOM's control. The average dc link voltage before, during, and after the fault is shown in Fig. 9. During the fault, the dc voltage drops rapidly as the faulted module capacitor discharges. When the faulty module is removed, the average dc voltage drops to roughly 80% of the initial voltage, as expected. The continued variation in the dc link voltage is due to the continual variation of the arc furnace load that the STATCOM is compensating and is normal.
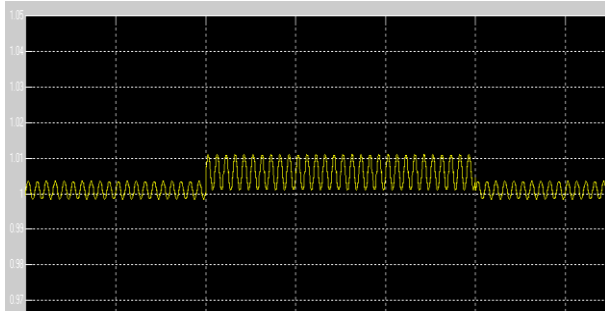

Figure 8. STATCOM voltage before, during, and after fault.
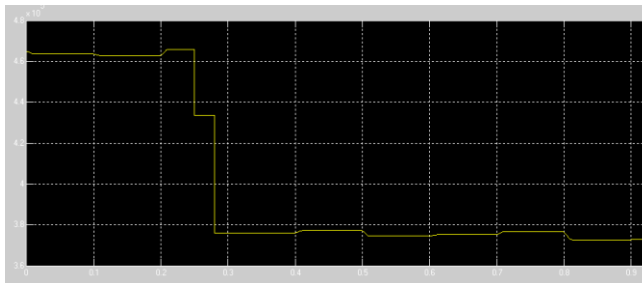

Figure 9. DC voltage before, during, and after fault.

Fig. 10 shows two cycles of the STATCOM multilevel voltage output. There are several important aspects of this output waveform that have been highlighted. First, note the voltage collapse of the first level due to the faulted cell. This collapse in voltage will occur at the level that corresponds to the faulty cell. It is not possible to directly correlate the level number with the cell number (i.e., a collapse in level four does not necessarily indicate a fault in cell 4
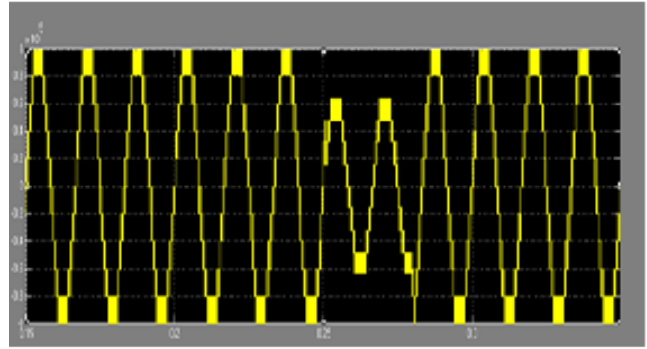

Figure 10. Converter output with faulted cell.

because of the redundant state selection scheme that is used to balance the capacitor voltages further aspect of note is the increase in length of the top level duration. This is due to the increase in the modulation gain k due to the decrease in dc link voltage. Since the STATCOM output voltage is directly proportional to

$$V\text{stat} = kV\text{dc} \cos \alpha$$

where k is the modulation gain and α is the phase angle. If $V\text{dc}$ decreases by 20%, then, k must increase by 20% to compensate. An increase of this magnitude in modulation gain takes the PWM into over modulation where the magnitude of the reference waveform exceeds the magnitude of the carrier. This results in an increased length of time at higher voltage levels. Over modulation may also result in the increase of lower frequency harmonics. The modulation gain k is shown in Fig. 11.
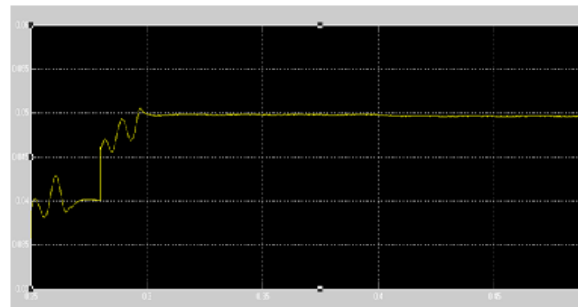

Figure 11. Modulation gain before, during and after fault.

The individual module capacitor voltages in each phase for a faulty a phase switch are shown in Fig. 12. Note that the faulted module voltage decays rapidly at 2.5 s (when the fault was applied). The remaining capacitor voltages in phase a show significant "chopping" as the redundant state selection approach rapidly alternates between modules to maintain the average dc link voltage. A crowbar circuit is used with each module to limit the maximum dc voltage, leading to the chopping behavior. Phase b shows a continual decline in all of

the capacitor voltages until the corresponding faulty module is removed at 2.8 s. The capacitor voltages increase until they are in the nominal range and then exhibit similar "chopping" until they are regulated. Phase *c* does not exhibit chopping because all of the individual cell voltages are of similar magnitude and do not exceed the crowbar maximum.
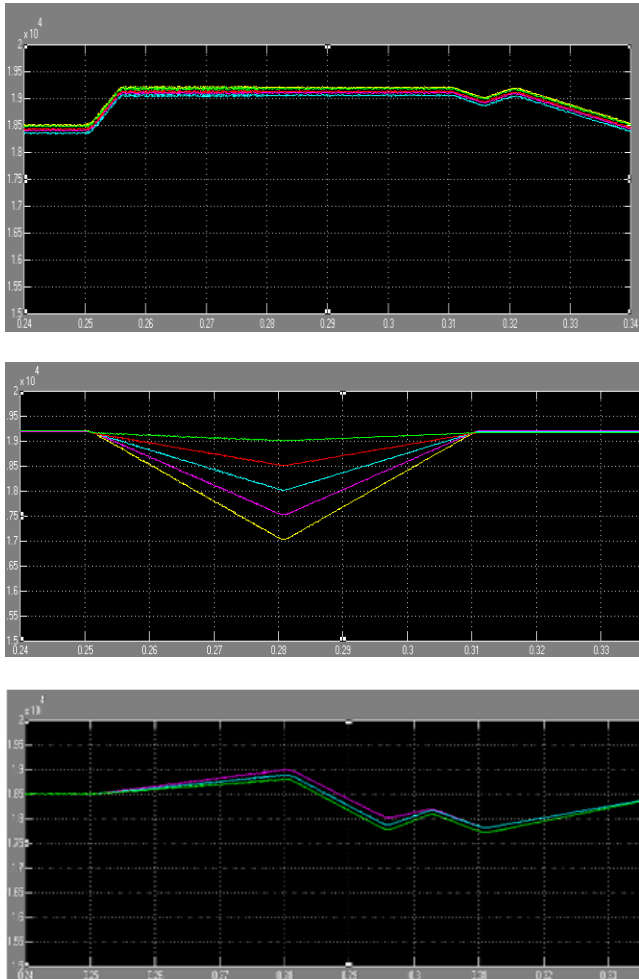

Figure 12.Indivisual module capacitor voltages before,during and after fault in phase-a,phase-b and phase-c.

B. THD Performance

Harmonic injection is a concern with STATCOMs [8]. A harmonic analysis has been performed on the output voltage at the point of common coupling. One of the primary reasons for using a multilevel converter is the reduction in harmonic content in the output waveform. Fig. 13 shows the harmonic distortion levels at the STATCOM PCC before, during, and after the fault. Since this is measured at the PCC, the output waveform has already been filtered to remove high-frequency components.

Before the fault, the THD level is less than 1%, which is quite good. During the fault, the THD increases to over 5%. When the fault is removed, the THD decreases and settles at approximately 2.5%, which is in the acceptable range for a 115-kV system . Therefore, the loss of one of the cells does not necessitate the immediate removal of the STATCOM from service. The increase in THD after removing the faulty cell is due to several reasons. First, the STATCOM filters were tuned to the resonant frequencies associated with the eleven level converter and are not as effective when the converter topology changes to a 9-level. Second, the over modulation required for the 9-level converter increases the content of the lower frequency harmonics. While the third harmonic is quite high during the fault, it returns to prefault levels after the fault is cleared, whereas the fifth and seventh remain fairly high due to the overmodulation. Even though they are increased over the prefault value, they still remain under the 1.5%-limit required of 115-kV systems.
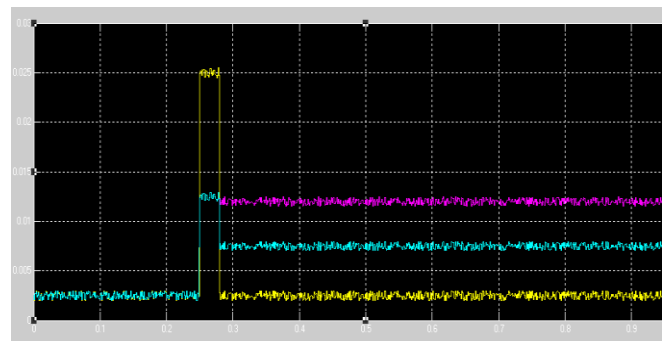

Figure 13. Percent harmonic content of the faulty phase before, during and after fault.

V. CONCLUSION

In this paper, a fault detection and mitigation strategy for a multilevel cascaded converter has been proposed. This approach requires no extra sensors and only one additional bypass switch per module per phase. The approach has been validated on a 115-kV system with a STATCOM compensating an electric arc furnace load. This application was chosen since the arc furnace provides a severe application with its non sinusoidal, unbalanced, and randomly fluctuating load. The proposed approach was able to accurately identify and remove the faulted module. In addition, the STATCOM was able to remain in service and continue to provide compensation without exceeding the total harmonic distortion allowances.

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