A novel approach of Inductive effects and reduce IR drop in high speed vlsi

MLN.Acharyulu [1], Murthi Sarma [2],K.Lalkishore [3]
Prof,GPCET,krnl[1],Prof&HOD,BVC odalarevu[2],VC of JNTUA[3]

Abstract
This paper deals with one of the main challenges facing the chip designers is signal Integrity and IR drop .With increasing operating frequencies and elevating power consumptions in VLSI circuits, the design and analysis of on chip power distribution networks has become a critical design task . The decap inserting and inductive (L di/dt) effects can cause ringing, overshoot and reflections of signals due to impedance mismatch between the source and destination. Such phenomena can occur on clock lines and long buses. In addition, the switching noise due to inductive voltage drops is an issue for power distribution network. Therefore, it is important to model inductive effects accurately for high speed VLSI designs. The inductance effects can no longer be ignored as technology scaling progresses into sub-nm processes, since interconnect lengths become longer as the functionalities of the IC chip grow, the resistance of Copper (Cu) interconnect becomes less compared to previous generations of Aluminum (Al) interconnects, the chip operating frequencies increases into multi-gigahertz range, and signal rise and fall times become faster. In this paper study of noise induced by parasitic inductance and capacitance are observed, this work is based on simulation interconnect with parameters obtained from flop array method, swapping cell and clock buffers moments to reduce the IR drop. These voltage drops on power supply lines of switching devices in a clock distribution network can introduce significant amount of skew which in turn degrades the signal integrity. The IR Drop analysis part is done using the RedHawk .

Keywords: Dynamic power, Ldi/dt, electromigration, IR drop, switching noise, FAO(fixing and optimizations)s.

1.1 Introduction

As power continues to drop with the VLSI technology scaling associated with significance increasing device numbers in a die, power network design becomes a very challenging task for a chip with millions of transistors .Power Distribution Networks in High Speed Integrated Circuits[1]. The common task in VLSI power network design is to provide enough power lines across the chip to reduce the voltage drops from the power pads to the center of the chip. Decoupling Capacitor Effects on Switching Noise[7] electromagnetic models on high speed digital circuits[16] decoupling circuit for suppressing radiated emissions in vlsi[18] The voltage drops are mainly caused by the resistance or inductance of the power network metal lines. Inductance effects in on-chip interconnect structures have become increasingly significant [22] due to longer metal interconnects, reductions in wire resistance (as a result of copper interconnects and wider upper-layer metal lines) and higher frequency operation. These effects are particularly significant for global interconnect lines such as those in clock distribution networks, signal buses, and power grids for high-performance microprocessors. On-chip inductance impacts these in terms of delay variations, degradation of signal integrity due to vershoots/oscillations, aggravation of signal crosstalk, and increased power grid noise. The main difficulty in the extraction and simulation of on-chip inductance is the fact that inductance is a unction of a closed current loop. Therefore, it is required that both the current through a signal net and the return currents through the power grid be considered simultaneously instead of being analyzed in isolation. The current distribution in the entire circuit, including the grid, must be known in order to obtain a correct estimate of loop inductance. However, actual chip topologies consist of complex power grid and signal line structures, and current distribution depends on many elements, including device and interconnect decoupling capacitance, power grid resistance and inductance, pad locations, and operating frequency. Thus, the determination of current paths and, hence, the inductance is quite difficult, since it requires the accurate modeling and simulation of the complete signal net and power grid topology. Traditional approaches to inductance analysis are based on simple loop inductance models[23], [24], [25]. The loop inductance and resistance are extracted by defining ports at the driving gate, and then solving the current distribution

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for an RL model of the circuit using tools such as FastHenry[26]. The extracted inductance and resistance are then combined with lumped capacitance to construct a netlist. Crosstalk noise is the coupling of electromagnetic energy between traces .This induced energy degrades the signal integrity of the victim trace and causes errors or instability in the circuits connected to the victim trace [27]. This coupled noise also changes into emitted energy that radiates from the cable linked to the victim trace [28]. The amount of crosstalk noise depends on not only the space between adjacent traces, but also on the reflection due to the impedance mismatches at the driver and the terminations of the traces. To avoid such kinds of crosstalk noise, the layout of the substrate should be determined taking into consideration the sensitivities of the victim traces. In addition, crosstalk between adjacent power planes is also an important onsideration .Most of the latest LSI chips include several power supply banks for core and I/O circuits in order to decrease total power consumption. Consequently, the substrate or interposer should be provided with different power areas and planes in them. The power distribution system is essentially a route for supplying dc voltage to a chip. However, at frequencies above a few hundred megahertz, this power distribution system involves many harmonics of switching noise and it involuntarily works as a resonator [29]. The return easily couple with nearby signal traces and cause crosstalk problems [32].When signals transit through via holes among the power or ground planes with different voltage, the return current path of the signal is discontinuous at the via holes . Beginning at IC , the current follows the conducting trace to the via, and then is carried by conduction current on the via onto the trace on the lower level through the second via and to IC .The return current uses the upper surface of the adjacent ground plane as the return from IC , following beneath the signal trace. When the return current encounters the via, it transitions through the anti-pad hole to the lower surface of the ground plane, and then through displacement current is continued to the upper surface of the voltage plane. The displacement current is a distributed property of the parallel power planes, and excites the distributed modes of the planes. The current is continued to the lower surface of the voltage plane through the antipad in the voltage plane, and follows beneath the signal trace on the lower layer to the via adjacent to IC , where the process is repeated. If the signal line happens to be an I/O line that goes off the substrate,there is a conductive path for radiated EMI [33], [34].This type of discontinuity induces the dc voltage fluctuation and consequently causes PI problems [35]. It also causes strong radiation due to resonance of the power distribution plane [36]. In particular, the routing of high-speed digital signals should be designed taking the return path into consideration. From the viewpoint of PI, the lower the ac impedance of the power distribution network the better for the chip, package,and substrate [37]. From the viewpoint of EMI, however, transmission of switching noise from a chip to a package or substrate through the common impedance path is undesirable. Also,the dc power bus resonates at frequencies above a few hundred megahertz, because the power and ground planes pair up and work as a parallel plate transmission line resonator [38]. The power network can be modeled as a low-pass filter with RL segments in series, attached with capacitors at each end. The current sources of the switching gates and the intentional decoupling capacitors are also inserted in the model. The IR drop is proportional to the average current consumed by the circuit in the chip. The L. di/dt drop is proportional to the time- domain change of the current, due to the switching of the logic gates in the chip operation. Accurate Crosstalk Effects of Coupling Noise between the Interconnects on Signal Integrity LossesinDeepSubmicron[15] Because of the large voltage drop due to various factors we need to analyze the IR drop of the power network.The potential sources of power-grid network design problems related to IR drop, ground bounce, and electro migration, and discusses the methodologies available to detect them. Apache Design Solution[2] Reliability Issues - Electro-Migration / IR Drop [3] p/g pad placement optimization for best ir drop[4] Power integrity and energy aware floor planning[20] Integrated-circuit design usually assumes the availability of an ideal power supply that can instantly deliver any amount of current to maintain the specified voltage throughout the chip. Aggressive interconnect scaling has increased the average current density and the resistance per unit length of wires and on-chip Inductance. Since the supply voltage level is also reduced with the technology scaling, the power

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supply noise becomes even more pronounced because the ratio of the peak noise voltage to the ideal supply voltage level increases with each scaled technology node. The power supply noise mainly manifests itself as a voltage drop in the power distribution networks ,after Red Hawk static (IR) or dynamic voltage drop (DvD) analyses have identified areas in the design that have unacceptable voltage drops, RedHawk Fixing and Optimization (FAO) functions allow you to modify the power grid and/or allocate new decoupling capacitance to meet specific static and dynamic voltage drop targets, and also power related circuit timing problems. Fixing voltage drop problems also can reduce noise from ground bounce. Operations on instances with multiple Vdd power sources are handled transparently. Once a trial power grid and initial placement information is available, FAO can be used to globally modify power grid parameters to meet specific voltage drop targets. After detailed placement, and prior to detailed routing, tool can be used to identify high dynamic voltage drop areas, or areas with significant timing impacts from DvD, and fix them through a combination of power grid wire changes and targeted decap placement.

1.2 Basic concepts in IR drop and Ground Bounce

the closed formula for plane resistance between two via contacts is given in Figure1 various kinds of metal structures including planes, vias and traces constitute the power distribution system between the supply source and one or more IC components. The supply source is typically implemented as a DC-DC converter and referred to as a voltage regulator module (VRM). Assuming the current requirements are met, the IR drop is determined by the effective path resistance between the VRM and the IC components. In a microelectronic system, the system's IR drop may be budgeted into three portions. On chip IR drop, package and board. On-chip IR drop has been extensively studied because the resistive loss is severe due to the fine feature-size (a few microns and below) of the on-die power grid. On the other hand, package and board-level IR drop have not been given much attention due to their much smaller contribution to the overall path resistance and hence voltage drop. However, due to increased current requirements and reduced supply voltage noise margins, package and board IR drop (in the range of tens to hundreds of mill volts) now can have

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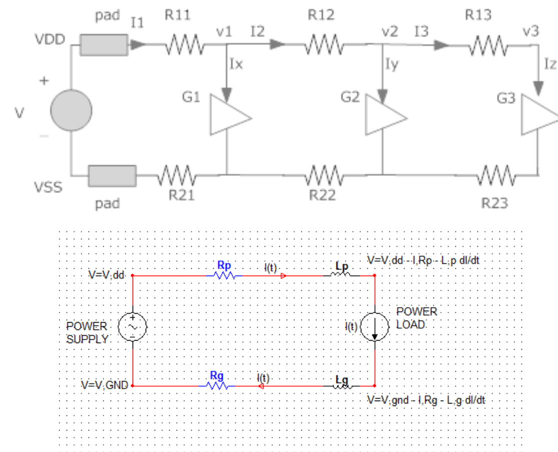

Figure1(a)&1(b)Electrical network representation of the power grid.

a significant impact on the operation of high-speed devices. The Fig 1 shows the entire chip power grid is represented in a electrical network with R and C .It shows a chip power supply connected to the chip pads. The power-grid network is illustrated by the R11-R13 resistors for VDD and R21-R23 resistors for VSS. These resistors represent the resistance of interconnect from the pads to the cells or transistors. G1- G3 cells are connected to VDD and VSS.

1.3 Local and Global IR drop

IR drop and ground bounce can be both local and global phenomena. They can be local phenomena when a number of cells in close proximity switch simultaneously, causing IR drop or ground bounce in that localized area. A higher power grid resistance to a specific portion of the chip can also cause localized IR drop or ground bounce. They can be global phenomena when activity in one region of a chip causes effects in other regions. For example, block B2 (A) in Figure 2 suffers from IR drop, because of

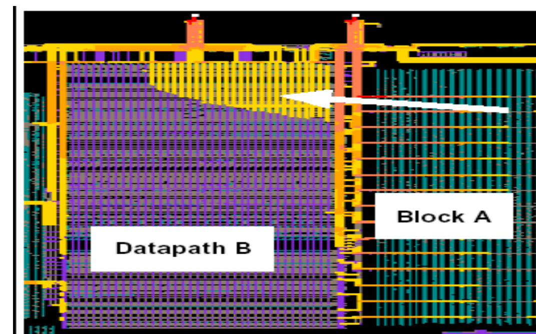

Figure 2 shows the Drop Due to over consumption

the current drawn by block B1 (B). In an ideal power grid with equally distributed current and peripheral power pads, the power grid has a set of equipotent surfaces that form concentric circles centered in the middle of the chip as shown in Figure 3 The center of these concentric circles has the largest IR drop or ground bounce, and the amount of the effect decreases toward the pads; its continuities in these circles typically identify regions containing discontinuities in the power grid or unequally distributed current flow. Large amounts of IR drop or ground bounce can be caused by simultaneous switching of cells and transistors. If all cells and transistors of a design switched at once, the local or global IR drop or ground bounce on a chip would be extremely large.Potential causes of simultaneous switching are the following:a) Synchronized clock networks b) Bus drivers c) Memory word line drivers d) Signal I/O circuitry e) Any groups of large drivers designed to switch together

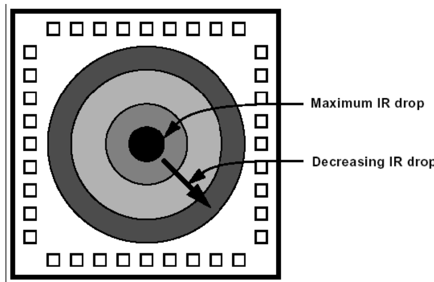

Figure 3 Equally Distributed Current Resulting in Concentric Rings of IR drop or Ground Bounce

Section II

IR Drop Analysis Generated Flow

The following flow has been generated for the purpose of Static and Dynamic power analysis in fig 4.Each block will be explained in detail for the purpose of easy understanding of what we are doing in the flow. There are a few utilities provided by the vendor for extracting the required outputs from the available inputs. Each utility is explained in detail along with its purpose, method of usage, inputs required and the outputs generated to help out to run the final flow The first most important is the directory structure. Initially create the directory structure as per the convenience. Later we need to copy the available inputs into their respective directories.

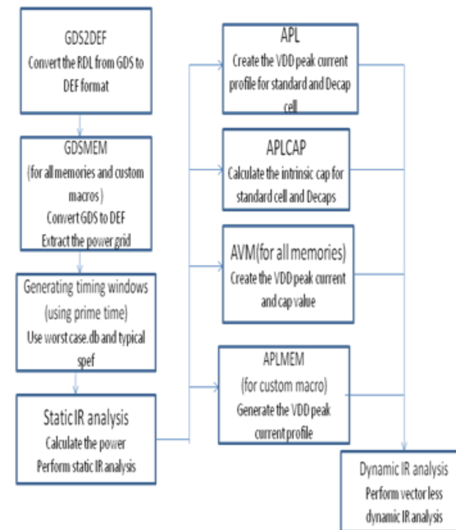

Figure 4 Generated Flow Diagram

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STEP 1In this step we extract the net list files for the available/used cells in the library extraction file and also the macros. For cell characterization, the tool needs to know the size of the each transistor and their locations. So you need to run Calibre to get the extracted netlist which is based on the GDSII format, resulting in a spice netlist with $X $Y location of each transistors. The gdsmem doesn't take ".GLOBAL" into account. It needs to explicitly state the VDD and GND pin names. Having the list of memories and custom macros that we are using, you can put them into a file and run a script which will create the required netlist which contains the $X and $Y locations. Based on the macros found in the gds Dir and net list Dir, or based on the cells list, the script generates a Calibre run file to extract the locations even for the macros

GDS2DEF :This step is only useful when performing Analysis for a flip-chip design. This step is not required when performing analysis for a wire bond design. This is because; there is an extra layer present in the flip-chip kind of designs, namely the RDL Layer.This layer should be separately run for having its own def, lib and lef files. This is because; this contains no cells and also there is no need to add any current sinks to the RDL.

The use of this RDL is that it contains all the bumps on it. We need to specify the voltage input points, so that it can consider those points as the sources for supply and feed it to the core. The drop along the

package wires is also taken into account .The IO ring / RD layer can be assigned to any part or to the whole chip. In our project as there were a few issues we have included it in the partition1. The rest were analyzed without the ring.

STEP2:

GDSMEM :The primary use of gdsmem is to convert GDSII of memory cells, but it can also be used on blocks such as analog cells, I/O cells and other IP for which DEF is not available. The program creates corresponding DEF, LEF and LIB files named after the cell, such as <cell-name>.def, <cell-name>.lef, and <cell-name>.lib. A current distribution that is more characteristic to the cell can be obtained from this process. If used with alternatives such as a SPICE netlist with the X, Y locations of the transistors, the current sinks can be appropriately scaled. The gdsmem utility can handle 45-degree geometries in the GDSII. Other non-Manhattan shapes are not modeled.After this utility has been run, we have design extraction files, libraries for each and every cell and also the macros and IP's present in the design.

STEP3:

Generating Timing Windows (Switching windows) Generation of the timing window file is one of the important steps in the analysis flow. RedHawk's PrimeTime TCL interface pt2timing is used to obtain timing information such as slew (transition times) and timing windows. This information is used by Red Hawk to improve the accuracy of both static IR and Vector less Dynamic voltage drop analysis. For static IR drop analysis, the slew information is used to calculate the average power. In addition, for dynamic voltage drop analysis, the timing window information is used to calculate the peak power and voltage drop.The following steps are performed in the PrimeTime environment:

1. Invoke PrimeTime, pt_shell
2. Read in the design.

If a fully annotated PrimeTime database is available, use the read_db command.

pt_shell> read_db <path>/<design_db_name>

If a fully-annotated database is not available, then the Verilog netlist and library must be read using the read_verilog command:

pt_shell> read_verilog <path>/<verilog_netlist>

3. Link the design:Ensure that all link paths are set correctly before linking the design. pt_shell> link_design
4. Read in the parasitic information.

The parasitic information yields accurate timing information in the design:

pt_shell> read_parasitics <path>/<paraistic_netlist>

5. Set up case analysis and constraints.

The appropriate case analysis and constraints must be set up prior to calculating timing information. Case analysis is required to get the correct operating conditions for clock gating or muxing. Source the appropriate PrimeTime constraint files for your design.Note that STA tools such as PrimeTime use BC/WC analysis as default, where the worst-case corner conditions are used for the Setup time check and the best case corner conditions are used for the Hold time check on a clock path. If the worst pin timing is used for min_arrival and the best pin timing is used for max_arrival, then the min_arrival can be greater than max_arrival. To avoid this situation, make sure that the following conditions are met prior to running PrimeTime timing analysis:

The SPEF file is generated for worst-case corner conditions

The .lib and .db files contain worst-case corner conditions

For PrimeTime script, use set_analysis_type single and Set_operating_condition or set_min_library to be 'worst'. Use a propagated clock

6. Source the PrimeTime TCL script.

The pt2timing.tcl script extracts the slew (transition times) and timing window information. The default units for these values are nanoseconds (e-9).

Note that if ILMs are used for the full-chip timing, then the ILM must be disabled prior to running the pt2timing.tcl script: pt_shell> source <path>/pt2timing.tcl

7. Run the PrimeTime script: pt_shell> getSTA *

The STA output file is <design_name>.timing. The STA output file must be specified in the .gsr file using the STA_FILE or BLOCK_STA_FILE option.

STEP4:

Using all the above inputs, run the command file, which contains the entire required inputs list.

A model file is provided in the Appendix.

STEP5:

Now as the static power analysis is done, we get an estimate whether there will be an extra drop or not if

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dynamic is performed. The Static results are used in generating the flow for Dynamic Analysis. The APL-based dynamic analysis uses SPICE-level current waveforms in the Apache Power Libraries (APL). This method provides transistor-level accuracy needed for detailed dynamic voltage drop, decap analysis, and verification. Apache Power Library (APL) function characterizes every cell in the design library to extract the current profiles, which are used by RedHawk for time-point based transient simulation. APL also extracts intrinsic, output-state dependent decoupling capacitance (intrinsic decap), equivalent power circuit resistance (called "Effective Series Resistance") and leakage power for every cell used in the design. The general APL flow is shown in Figure 5 below.

STEP6:

The APLCAP utility enables us to calculate the intrinsic capacitance of the standard cells. The intrinsic capacitance is nothing but the capacitance which is because of the cell in inactive state. The standard cells also include the Decap cells. Now we have known the current profile, ESR and capacitance values of all the cells which are being used in the design.

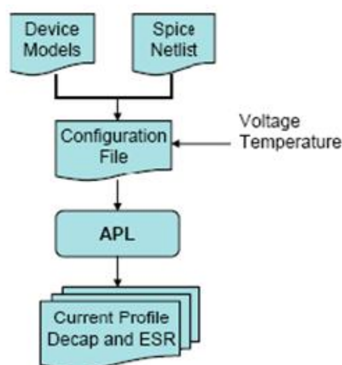

Figure 5 APL flow for extracting the current profile, decaps, and power circuit Effective Series Resistance for each cell

STEP7:

Embedded memories are taking an increasing share of real estate in SoC designs. Given their increasing complexity and power consumption, it is necessary to model embedded memory blocks accurately to consider their impact in a full-chip dynamic voltage drop (DvD) analysis. Voltage drop inside memory blocks poses a problem for deep sub-micron designs. Also, high power demand from memory instances can cause DvD in the surrounding logic, thus impacting their timing and functionality. At a full-chip level, the concern lies in ensuring that the memory blocks get adequate power based on their specifications.

Section III

3.1.Power grid fixing and optimization

As the design moves through final placement and routing, you can use Fixing and Optimization functions to automatically modify the grid parameters and decap placement to meet specified goals for both voltage drop and also power related circuit timing. When all of your voltage drop constraints are met, you can export an ECO file with the needed design changes and then perform a final Spice-accurate power analysis signoff of the design.

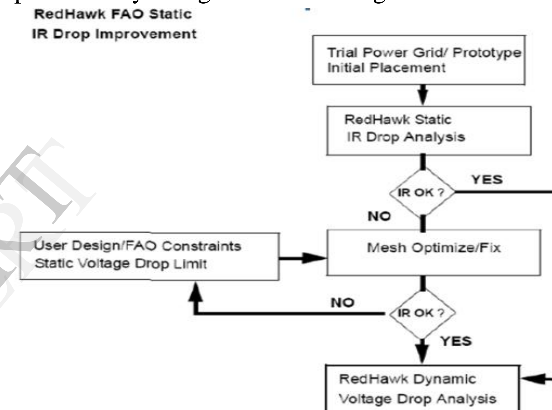

Figure 6. Flow of IR drop improvement

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3.1.2. Automated Power Grid Optimization and fixing procedures

The key commands for using FAO to adjust grid widths are and have the following functionality: mesh optimize - investigates a grid width solution within a defined area (fao_region). All wire segments on the specified metal layers will be adjusted to the same width to solve the voltage drop problem, either for the full chip or within the width of the specified region (but the full height of the chip). With the –taper option, grid wire segments are only resized within fao _region and not outside of it (not the full height of the chip).mesh fix - investigates a grid width solution within a rectangular region that includes all "hot spots" (high voltage drop nodes) and their associated fix window areas. For all hot spots within fao_region, wire segments in vertical and horizontal bands (full width and height of chip)

defined by the dimensions of the fix window, will be adjusted to an appropriate width to solve the voltage drop problem. With the -taper option, grid wire segments are only resized within the specified region (fao_region), and not outside of it.

mesh snscalc - for a selected region and set of layers and nets, mesh snscalc calculates and reports a number representing the relative average sensitivity for modifying the width of wires associated each layer and net selected--the higher the sensitivity number reported (in mv of voltage drop reduction per micron of additional wire width), the more effective a wire width change would be in reducing the worstcase voltage drop within the selected region. Using this command is recommended before performing any grid resizing.

mesh sub grid - adds a new subgrid mesh, with an area defined by the GSR keyword 'fao_region', including power nets defined by 'fao_sub_grid_nets' and with physical characteristics defined by 'fao_sub_grid_spec'. The new subgrid is targeted to achieve a voltage drop specified by the GSR keyword 'noise_reduction' . The min/max width of the new grids to be sized is specified by 'fao_range'. The minimum width is also used to create the initial sub grid before sizing analysis.mesh set width - allows the mesh wire width to be modified for the specified layer(s). By default the wire width is modified equally on both sides of the mesh center line, but the width change can be made on only one side of the wire by specifying the ‘expand_dir’ (or it could be the contracting direction if you are making the width smaller).Several additional commands are available for modifying the power grid, but are not needed frequently, and are summarized below.Mesh add - allows you to add a specified mesh section to the grid, including specific layers and regions of the design. Useful for easily modifying the grid and evaluating the effect on voltage drop Mesh delete - allows you to delete a specified mesh section of the grid, including specific layers and regions of the design. Useful for easily modifying the grid and evaluating the effect on voltage drop mesh vias - allow you to add a group of vias in a region of the design using specified via models mesh generate - generates a prototype grid based on the user constraints that are provided in the design constraints file (.dcf) Ring add/delete - adds or deletes a specified power/ground ring

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Example 1- Full Chip Grid Fixing - Reducing Static IR Drop Conditions: Early in design development. Your design requires a lower voltage drop. You want to use full chip uniform grid optimize methodology, so mesh optimize is used.Goal: Perform full power grid optimization for static voltage, reducing the static IR drop target from the existing high drop,

1. Decide on what GSR keyword settings are necessary. This time we will tighten the voltage drop, evaluating the grid width on metal6 for whole design. Keep in mind if a tighter voltage drop limit is specified (using ‘noise reduction’), then the fao_range should be increased to allow FAO to increase grid widths.

For example, if you want to reduce the voltage limit by 10%, then the following
GSR keyword settings should be used:
gsr set fao_turbo_mode 0
gsr set fao_nets VDD
gsr set fao_layers {{metal6 hor <= 29.4}}
gsr set fao_range {{metal6 10 35}}
gsr set noise_reduction 10

The allowable range of horizontal metal6 widths for this analysis is now 10-35 microns, instead of (8-29.4u) less width, and the ‘noise_reduction’ value is now a positive number, 10 percent.

2. Run mesh optimize as follows:
Mesh optimize -eco <filename>.eco

3. Look at your results report file reported by the redhawk.gion: <0 0 4817.32 8316.08>
FAO Mode: accurate,Simulation Mode: static,Net: VDD
Noise Reduction: -15%, Initial Worst Static Noise: 17.578mv
Voltage Noise Constraints: 20.2147mv,
* Searching Target Grids * Net <VDD>: Layer <metal6>: identified 44 wires
* Sizing Target Grids *

Following the run, FAO reports 44 wire change recommendations, as shown in the log file below. In this case, there will be less metal usage in the metal6 VDD net as a result of the relaxation in the static voltage drop limit. Note that new via models also are specified to match the wire changes Optimization succeed: no error Optimized width of layer metal6: 30.0um

Metal Usage Change Report
Net <VDD>:

Layer <metal6>:5.05281e+06um^2 => 4.09119e+06um^2 (-19.03%)
Total: 5.05281e+06um^2 => 4.09119e+06^2 (-19.03%)

3.2 Decoupling Capacitance Optimization

Static IR drop is traditionally controlled by a relatively simple process of wire sizing, adding more power straps or vias, introducing additional metal layers, or by switching to a flip-chip package with power-ground planes. Traditional static IR drop fixes can penalize the area, routability, performance, and chip cost when used to excessively guard band the design. However, guard banding will not protect a design from dynamic current spikes, as it is a transient phenomenon, which is data-dependent. Dynamic hot spots can only be resolved by inserting decoupling capacitance at precise locations close to a victim to filter out current spikes.

Decoupling capacitance has a number of components that must be considered together during analysis and optimization. Some decoupling capacitance components are intrinsic to the design, and some are intentionally inserted into the design to reduce dynamic voltage noise, as depicted in the circuit model. The various types of decap components are listed below:

With 20x20um^2 : (Red:CKBD Green:DCAP)

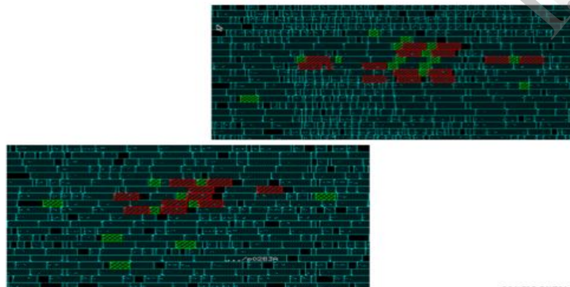

Figure 7 Decap cell placement

Intrinsicdecap
- Well capacitance Cwell,- Device capacitance, Cdev
- Power ground capacitance, Cpg, - Cell loading, Cload,- Macro capacitance, Cmacro, • Intentional decap, Cdecap

Without a robust dynamic voltage drop and decap analysis methodology designers are forced to use up all their filler cells and insert intentional capacitance in an adhoc fashion after post-layout verification. Unfortunately, this method does not repair the actual dynamic noise problem and can in fact cause unexpected timing failures and increased leakage currents. Decap insertion is best accomplished early stage in the design stage; to ensure that the location and correct amount of intentional decap is allocated during the placement.In this design we added the decap cells where we seen the more IR drop .in that region we added the 8 to 10 Decap cells in the 20x20 square micron region to reduce the voltage drop. The bellow fig 7 shows the regions where we added the in the blocks In above fig the decap cell are in the green color and CKBD cells are in red.we added the decap cells nearer to the clock cells which have a more voltage drop. We done the analysis without decap cell addition and with decap cell addition. The worst IR drop in the design as below Worst voltage drop at minTW without Dcap addition: 149.4mv (16.6%), Worst voltage drop at minTW with Dcap addition: 143.8mv (15.9%) ,In this minTW is the minimum value during the timing window (switching window), in design we analyze the IR drop is over the simulation cycle in this cycle we analyze IR over the 2 to3 switching windows, during this the design is stable, This whole cycle is purpose of accurate results.In switching window we considered three cases maximum, average and minimum , In this three the worst IR drop results are at the minimum value during the switching.

The below are the number instance above the 13% voltage drop

In the block zzz_t:
Without Dcap addition: 4198
With Dcap addition: 1922

The contour maps shows the IR drop regions in the design with and without decap cell as shown in fig 8 and fig 9

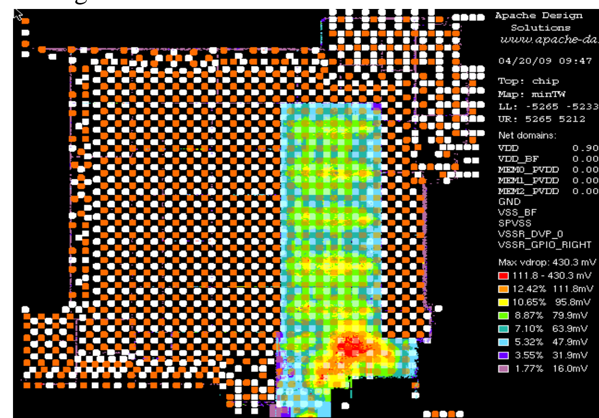

Figure 8 Without decap addition ,

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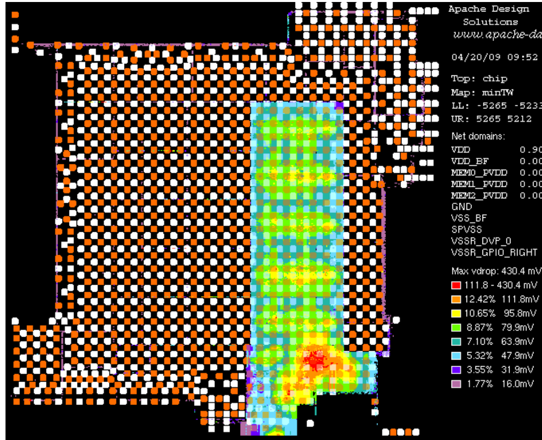

Figure 9 with decap addition

In this the voltage drop is more in the without decap cells which is 149.4mv, by adding the decap cells the drop is reduced to 143.8mv we gained 3mv, and the number cells also less greater than 13%.So by adding the decap cells we can reduce the IR drop effect, but the amount of decap cells addition also take care because the decap cells have more leakage compare to other cells. The addition of decap cells is with in the limit.

3.3 CLOCK CELLS (CKBD) MOVEMENTS

We observed in our design having a more voltage drop where the clock cells are placed clustering means in that region the CKBD cells are more in side by side, we done the experiment the IR drop analysis with clock cells movement that 10 to 15 microns between the one clock cells to another clock cells. By moving the clock cells, timing is bad 5ps to 10ps, we done this experiment only the timing is recovered in the data path.The IR drop values with and without CKBD movements are shown below on two blocks.

In the block (tile): yyy_t

IR drop is at minTW value without ckbd spreading is 139.3mv (15.47%)

IR drop is at minTW value with ckbd spreading is 134.6mv (14.9%)

Number of instances above 13% IR drop.

Without ckbd spreading: 36176

With ckbd spreading: 13650

Number of instances above 12% IR drop.

Without ckbd spreading: 88764

With ckbd spreading: 78224

The block yyy_t have voltage drop before moving the clock cells is 139.3mv and after spreading the cells that come down to 134.6mv.This amount of drop we saved by moving cells because the clocks cells are switching two time over the one cycle.So we need to take care in CTS to place the clock cells with some distance. By moving the cells the number instances have less voltage drop. Similarly in the block: zzz_t shown in below. IR drop is at minTW value without ckbd spreading: 135.2mv 15.02%) IR drop is at minTW value with ckbd spreading: 131.6mv (14.6%)Number of instances above 13% IR drop.

Without ckbd spreading: 288, With ckbd spreading: 131, Number of instances above 12% IR drop. Without ckbd spreading: 88764,With ckbd spreading: 78224 ,

From the above cases the clustering clock placement is having more voltage drop we need to consider the IR drop effect during CTS to reduce the voltage drop due to the clock cells.

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3.4 SVT to HVT cell swapping

In this method after routing the design, in non critical paths we swapping the svt cells to hvt cells upto the paths are not violating the timing. The hvt cells have less leakage compare to the svt cells.

The below details shows the in block HVT percentage before and after swapping and corresponding leakage

The block xxx_01 with out HVT swapping

Total Leakage = 59351.389uW, Total Leakage saving = 1758.145uW (= 2.17%)

Total Stdvt cells = 608442 (95.38%) 1153827.81um^2 59049.803uW (74.42%)

Normal svt = 17523 (02.75%) 47514.05um^2 6 234.927uW (07.86%)

Wimpy svt = 590919 (92.64%) 1106313.77um^2 52814.876uW (66.56%)

Total Hivt cells = 29457 (04.62%) 33452.32um^2 582.181uW (00.73%)

Normal hvt = 50 (00.01%) 84.67um^2 2.574uW (00.00%)

Wimpy hvt = 29407 (04.61%) 33367.65um^2 579.607uW (00.73%)

The block xxx_01 after HVT swapping

Total Leakage = 46389.693uW, Total Leakage saving = 21912.877uW (= 24.82%)

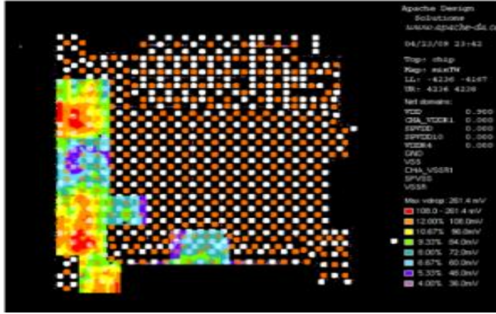

Figure 10 IR drop map without HVT swap

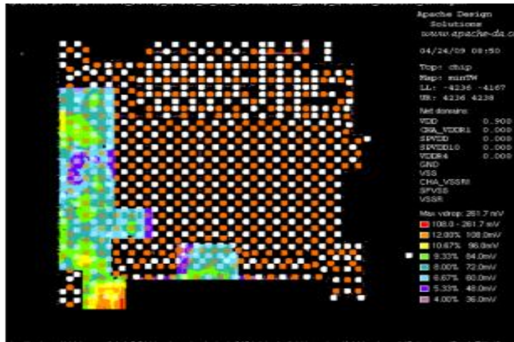

Figure 11 IR drop map after HVT swap

Total Stdvt cells = 379651 (59.37%) 671390.75um^2 38960.389uW (58.68%)
Normal svt = 59554 (09.31%) 106252.25um^2 11751.426uW (17.70%)
Wimpy svt = 320097 (50.06%) 565138.50um^2 27208.964uW (40.98%)
Total Hivt cells = 259765 (40.63%) 519374.87um^2 7735.979uW (11.65%)
Normal hvt = 48 (00.01%) 55.21um^2 1.371uW (00.00%)
Wimpy hvt = 259717 (40.62%) 519319.66um^2 7734.608uW (11.65%)

In the above first column is percentage of cells, second column is area occupied by corresponding cell and the third column is leakage. In the above tile the hvt percentage before swapping in table 1 and 2 and after swapping the hvt percentage is 40.6%.total leakage is come down from 59351.389uW to 46389.693uW. The IR drop details are shown below tables before and after hvt cell swapping.

There are several GSR keywords that specify how the cell swap command operates:In fao_region:
specifies the target analysis area containing high power instances to be fixed From the above tables the IR drop is decreased in the tile xxx_01 from 130mv to 109mv. The no of cells swapping is depends on the timing criticality of the design. In the above two tiles the voltage drop is gained by almost 20mv.This is the one of the technique to reduce the IR drop effect in the chip.The below fig shows the IR drop contour map before and after HVT swapping fao_nets: when there are multiple V_{DD} nets in the design, specifies the name of the V_{DD} net with which the hot instances are associated noise_ limit : for the list of worst case hot instances, the noise _limit specifies the voltage drop threshold below which the hot instance will not be considered for swapping. For example, if noise_limit is set at 5%, hot instances with less than a 5% voltage drop would not be considered for swapping. num_hot inst: specifies the number of worst case hot instances to be swapped in the region fix_window: specifies the size of the area centered on each identified hotinst within which the cell would be moved or swapped (default: 40 x 40 u) fao_verbose: (0/1) controls the volume of output messages. (Default: 0, small amount)

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3.5 Flop Array Method

This flop array method we mention the flop array pattern in tune file , this pattern of flops are mentioned with exact toggle rate by conforming from the front end team. In this method by specifying the data toggle rate we can analyze the accurate voltage drop. This pattern is as follows line_(\d+)_data_reg_(\d+)_tag_(\d+)_addr_reg_(\d+)

Table 1 IR drop reports before swapping HVTcells

Tile Name	IR DROP (mv)	IR drop %	%inst >=14%	%inst >=12%	%inst >=10%	Nr inst >=14%	%inst >=12%	%inst >=10%
xxx_01	109.70	12.11	0.00	4.20	33.02	0	25692	201990
xxx_02	111.96	12.44	0.00	2.34	30.45	0	12386	161182

data_reg_(\d+)__(\d+)_methodfifo_(\w+)_reg_(\d+)_ _(\d+)_ cb(\w+)state_reg_(\d+)__(\d+)_ In this

Table 2 IR drop details after HVT swapping

Tile Name	IR DROP (mv)	IR drop %	%inst >14%	%inst >12%	%inst >10%	Nr inst >14%	%inst >12%	%inst >10%
xxx_01	130.20	14.47	0.01	9.01	60.16	62	55102	367917
xxx_02	128.40	14.27	0.01	5.59	47.69	52	29589	252439

Table 3 IR drop results without flop array

way the array of flop patterns are specified with data

TileName	IRDROP (mv)	IR drop %	%inst >14 %	%inst >12 %	%inst >10 %	Nr inst >14 %	Nr inst >12%	Nr inst >10%
xxx_01	123.50	13.72	0.00	3.08	40.87	0	16305	216362
xxx_02	127.90	13.21	0.00	21.45	69.86	0	131179	427236

toggle rate, instead of common toggle rate. The following table shows the IR drop results with and with out flop array method, we mentioned for the two blocks.In table 3 and 4 indicates the voltage drop without and with flop array, in the xx_01 design the

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Table 4 IR drop results with flop array method

Tile Name	IR DROP (mv)	IR drop %	%inst >14%	%inst >12%	%inst >10%	Nr inst >14%	%inst >12%	%inst >10%
xxx_01	124.10	13.79	0.00	4.72	48.17	0	24987	255007
xxx_02	142.38	15.82	2.05	34.19	78.98	12537	209092	483011

drop is decreased to 1mv and in xxx_02 design the drop is 15mv by mentioning the flop array pattern , this is depend on how many flops to mention the

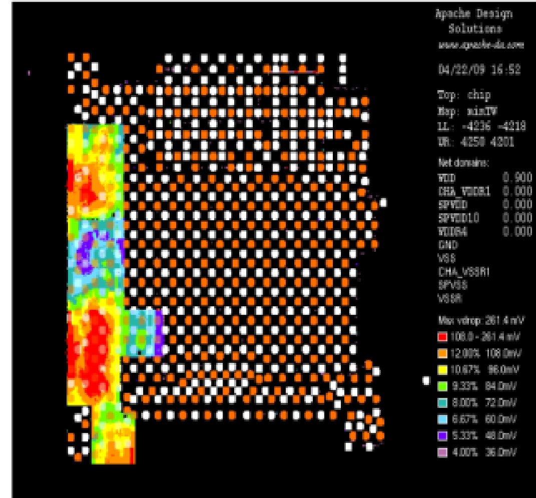

Figure 12 Voltage drop map without flop array method

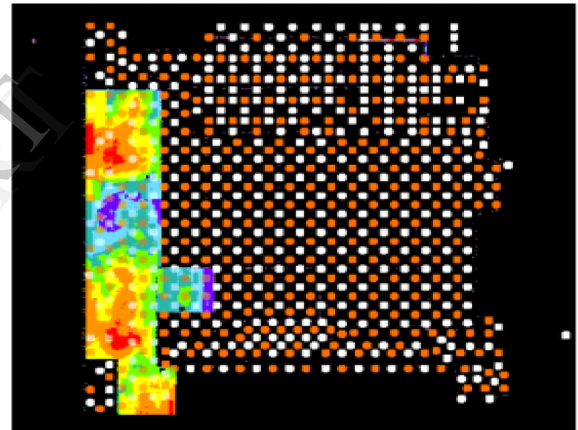

Figure 13 Voltage drop map with flop array method

exact data toggle rate .The below maps shows the voltage drop regions without and with flop array From the above figures the drop is more in without flop array compared to the with flop array. This array of pattern is taken from the front end team with data toggle rate of the flops. By specifying the flops with exact the voltage drop analysis is accurate but this is very difficult to mention.

Section IV

4.0 Conclusions:In this paper Redhawk physical power methodology, the inputs and outputs of the static and dynamic analysis. The IR drop flow analysis with the red hawk tools with different stages, the generic flow and in each stage we discussed about step and corresponding stage details. In this paper we analyze the different optimization methods like grid optimizing by increasing the width and make the proper via connections between the layers. The decoupling addition analysis, clock cell movement and swapping the svt cell to hvt cell. Implementing the above methods controlling the IR drop effects within the limits. The conclusion is the high frequency and more power consumption, we reduce this effects by adding decap cells, clock cell moment and swapping the svt to hvt cells in the not timing critical paths. The future work is taking care at the ckts stage do not place the clock buffer together, for each clock buffer need to maintain the 10 to 15um each other, and also the increases the number of parallel grid strips by decreasing the M8 and M9 metal widths, In block level decreasing the power grid pitch by considering area impact.

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