International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 7 Issue 02, February-2018

A Novel Low power and Swing Restoration SRAM Logic Circuit Technique

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***Abstract*- Design and Analysis of Static RandomAccess memories (SRAMs) which focus on optimizing Read and Write operation of 8T SRAM cell which is better than 6T SRAM cell Using Swing Restoration Dual Node Voltage. The read and Write time and improve Stability. PMOS Transistor with less width reduces the power consumption. In this paper Comparative Analysis of 6T and 8T SRAM Cells is done for 180nm Technology with Cadence Virtuoso schematics Tool.**

Keywords- Swing Restoration Logic, Dual Voltage, Delay, Stability, Read and Write access time, Low Power and Power dissipation.

I. INTRODUCTION

Low power SRAMs have become a critical component of many VLSI chips. This is especially true for microprocessors, where the on-chip cache sizes are growing with each generation to bridge the increasing divergence in the speeds of the processors and the main memory [P. Barnes 2010, S. Hesley, et.al, 2009]. This Paper is organized as follows: the characteristics of 6T SRAM cell are described are represented in section II. In section III, Proposed 8T SRAM cell is described. Section IV includes the simulation results which give comparison of different parameters of 6T and 8T SRAM cells and section V conclusion the work.

II. SIX TRANSISTOR (6T) SRAM CELL

In a conventional 6T SRAM cell, the data storage nodes are directly accessed through the bit-line access transistors during read operations, as shown in Fig.1. While reading, the storage node voltages are disturbed between cross-coupled inverter pair and bit lines. The BL and BLB are the bit lines and WL is the word line. The access transistors are controlled by WL (word line) to perform the operation of read and write operation. Bit lines act as input and output nodes. During a read operation, bit lines transfer the data from SRAM cells to a sense amplifier. Based on the technology the minimum length of the transistors is 180nm [1].

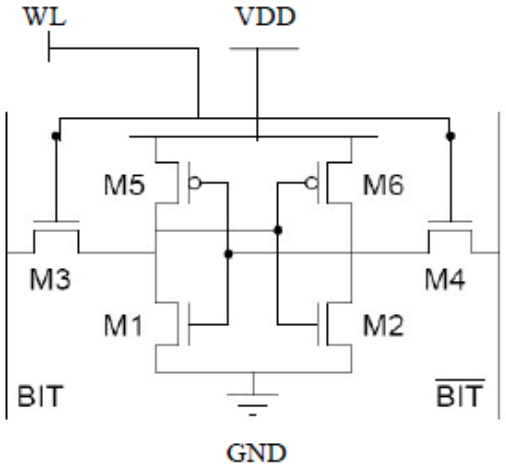

Fig.1. 6T SRAM Cell

III. PROPOSED EIGHT TRANSISTOR (8T) SRAM CELL

In this proposed SRAM, Dual Voltage with Swing Restoration Logic Perform node voltage in Hold, read and write operation and other parameters like Delay, Stability, are used. Comparison between Low power design 6T and proposed 8T SRAM Cell design is done. The comparison result revels that read, write and hold mode operation for 8T SRAM cell is better than 6T SRAM cell. This is because higher noise margin are obtained which ensure good write ability for the bit-cell.

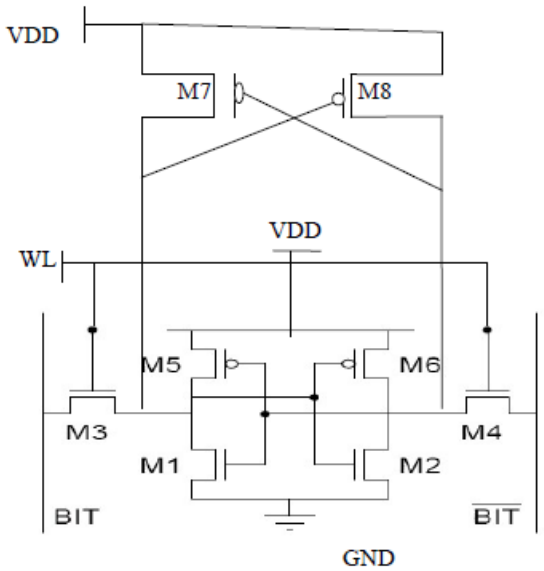

Fig.2. Proposed 8T SRAM Cell

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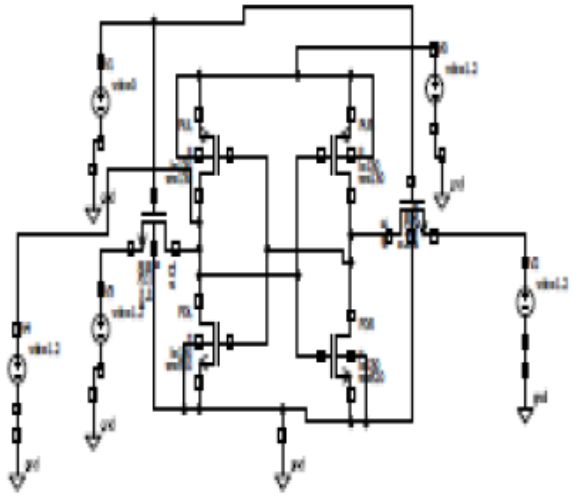
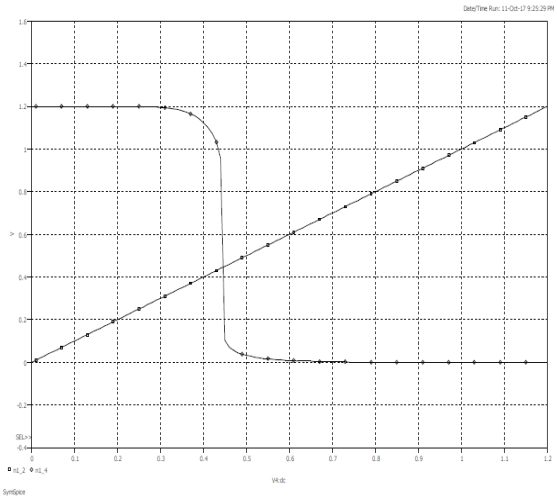
IV. SIMULATION RESULTS AND DC ANALYSIS

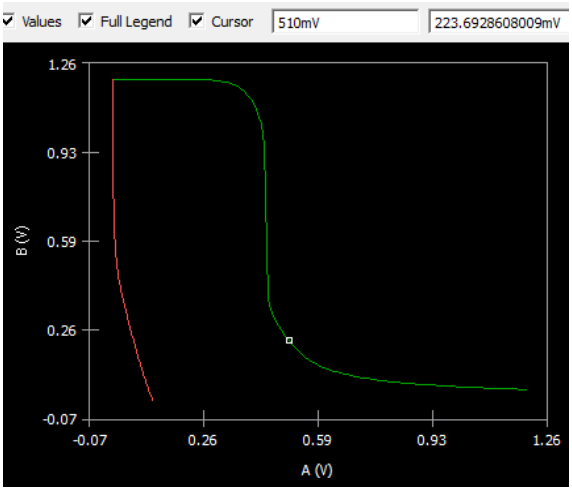
A. 6T SRAM cell output



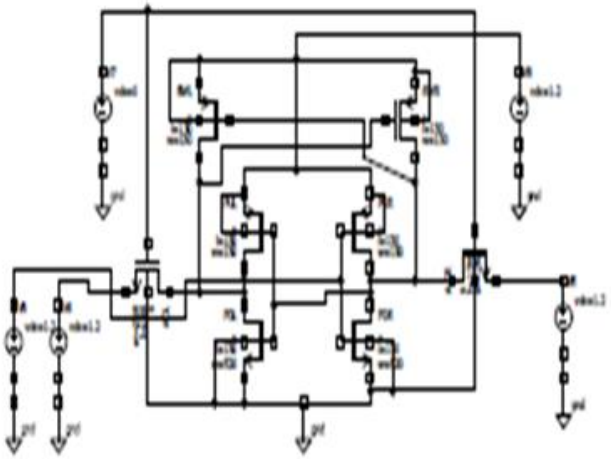
B. 6T SRAM cell DC analysis



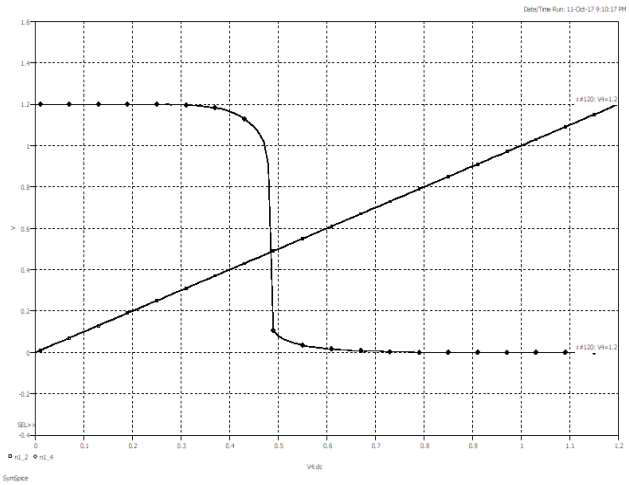
E. 6T SRAM CELL WRITE NOISE MARGIN



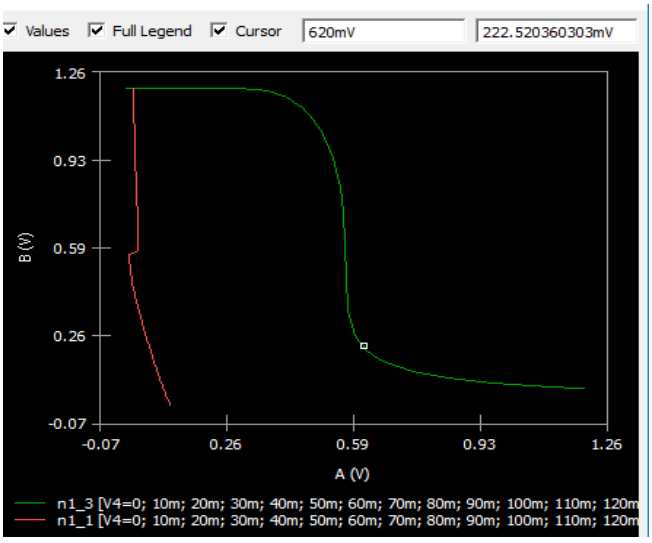
C. PROPOSED 8T SRAM CELL OUTPUT



D. PROPOSED 8T SRAM CELL DC ANALYSIS



F. PROPOSED 8T SRAM CELL WRITE NOISE MARGIN



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V. CONCLUSION

A low power and swing node restoration SRAM logic circuit technique is presented in the paper. In this paper comparative analysis of 6T and 8T SRAM cells in 180nm Technology is also presented.

In the proposed SRAM cell and Dual node voltage with Swing Restoration logic perform D.C. analysis Hold mode operation. D.C. analysis HOLD operation good noise margin 8T SRAM cell is better than 6T. This conclusion is good for power consumption is low. Then 8T SRAM Cell Write mode is power analysis is better Then 6T SRAM Cell. Then speed is higher for proposed 8T SRAM Cell.

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