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A Novel on Design and Analysis of on Chip Low Drop out Regulator for Improving Transient Response

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Abstract: **In Power management of System on Chips On chip (SOC) Linear Low Drop out (LDO) Regulators are dominating compared to other regulators. In LDOs Analog circuits playing an important role in the control of switching power supplies because of its simplicity and less expensive. To meet the increasing requirements of present and future processors with low voltage and higher load currents, a LDO with better transient performance is must. This lead to design a LDO with compensator which will make the loop stable for all load current variation. In this paper, a prototype of pole-zero(PZ) compensator for linear voltage regulator is designed for system level integration. Based on the frequency behavior analysis of the linear regulators, a PZ compensation scheme is presented for the PMOS linear regulator. This PZ scheme is able to control the large frequency variation of the PMOS linear regulator output pole. The effectiveness of PZ compensation is examined by mathematical modeling in Matlab and Simulink. Using this system level (high level) analysis of plant transfer function yields to design a controller for faster response of LDO.**

Keywords : LDO, PZ, Transient response, SOC.

I. INTRODUCTION

Scaling of transistors have boosted the growth of highly packed designs. System on a chip (SOC), integrates all components of an electronic system on a single chip. The high computing power of a large number of transistors, powers multi-core SOCs. But increased frequency of operation due to device scaling also results in larger power dissipation, with power numbers rising proportionately with faster computations. Multi core systems that run multiple processes, need power management techniques for efficient operation. These units control the regulated voltage for the system. The power supply module needs to be integrated into the design itself with voltage references, regulators and controllers. A faster computation consumes more power and also increases the frequency of load transitions. Hence a voltage regulator with higher efficiency and faster transient response, with minimum power dissipation is needed to be used in multi-core SOCs. The regulated voltage for a SOC is generated from an external supply voltage with a Band Gap reference as shown in Figure 1.

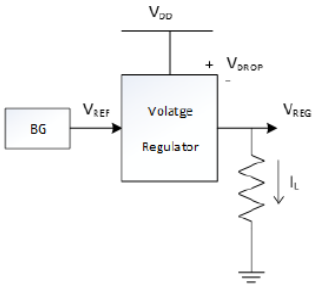

Fig 1. Simple LDO topology

Low Drop out Regulators

The output voltage of a regulator should have minimal changes in its output level with respect to variations in the process, input voltage, noise, temperature and other factors. Supply level gets reduced by an amount of V_{DROP} due to the saturation drop across the regulator. This loss needs to be small especially in current system designs with supply voltages being close to 1V. The quiescent current I_Q drawn by the regulator for its internal operation, accounts for the difference between input and output currents of the regulator. Dropout voltage refers to the input-to-output differential voltage at which the module fails to regulate the input supply. This point occurs when input level approaches the output voltage.

The rest of this paper is structured as follows: Section II presents the system model of LDO, in Section III, shows procedure to design compensator. Section IV shows the simulation results with droop and overshoot analysis. Finally, Section V concludes the paper.

II. CONVENTIONAL LINEAR LDO

This section of the paper presents about analog LDO and some of the theoretical aspects used through the paper.

In general, large voltage drops reduces the efficiency of regulators [1]. If we ignore the dissipation loss due to the non-ideal elements, its efficiency can be derived through the following set of equations:

$$P_{out} = V_{out} * I_L \quad (1)$$

$$P_{in} = V_{DD} * (I_L + I_L) \quad (2)$$

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out}}{V_{DD}} = \frac{I_L}{I_L + I_Q} = \frac{V_{out}}{V_{out} + V_{drop}} * \frac{I_L}{I_L + I_Q} \quad (3)$$

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Equation (3) highlights the need to reduce the drop across the regulator and the bias current IQ. Hence the design of LDO is important to increase its efficiency. A voltage regulator is similar to a voltage controlled voltage source (VCCS) with requirements of low output resistance R_{OUT}. This can be achieved by employing a negative feedback system as discussed in subsequent section.

Conventional PMOS LDO

Voltage regulators operate in saturation region where the transistor acts as a voltage controlled current source. Under varying load conditions, V_{gs} controls the low drop out regulator to supply the load current. This allows the voltage drop from the unregulated voltage to regulated voltage to be as low as saturation voltage across the transistor. The sampling resistors convert the current to voltage according to the following equation (4).

$$V_{out} = \left(1 + \frac{R1}{R2}\right) * V_{Ref} \qquad (4)$$

The negative feedback loop controls the regulator action and provides the necessary reduction in R_{out} as given by equation (5).

$$R_{out} = \left(\frac{r_{ds}}{1 + A_0}\right) \qquad (5)$$

where loop gain $A_0 = A_1 * A_2 * \frac{R_2}{R_1+R_2}$, Error amplifier gain $A_1 = g_m * r_o$, Pass Transistor gain $A_2 = g_{m0} * r_{mo}$.

Low dropout regulators comprise of a voltage reference, a pass transistor element, an error amplifier and sampling resistors as shown below in Figure 2.

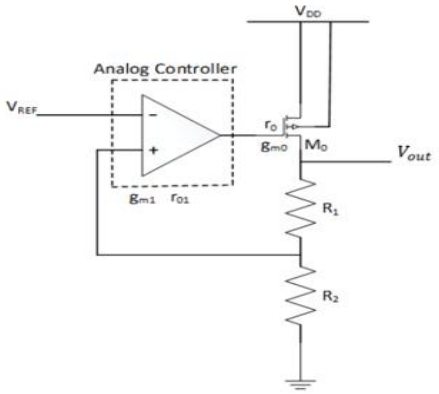

Fig 2. Conventional LDO regulator with analog Controller

LDO Performance Metrics:

The validation flow for the design for LDO includes different parameters. These are enlisted according to the analysis as follows:

A. DC Analysis

DC analysis includes supply voltage has to provide average input supply and also average LDO output. Load current (I_L), efficiency of the regulator decreases with increase in V_{drop} and I_Q. The I_L depends on activity of the load. Important DC analysis is Transient Analysis; it refers to switching loads conditions. Major factors to characterize LDO performance are settling time, Overshoot, and Voltage droop.

B. AC Analysis

Negative feedback systems are inevitable for its advantages of better control. But it brings along stability issues. AC analysis provides information about the circuit bandwidth, cutoff frequency, the gain, the role-off, or any peaking in the frequency response.

DC gain of the system refers to the flat gain at low frequency before the first 20 dB/decade roll off. 3-dB bandwidth also main factor AC analysis. The main components of AC part to decide system response are Phase margin (PM) and Gain margin (GM). The final key factor is Power Supply Rejection Ratio (PSRR), it gives a performance metric for ripple in the input supply and its effect on the output across different ripple frequencies.

The conventional PMOS LDO is shown in figure 3 with load connected. The load capacitor C_o with ESR R_c provides pole and zero these two components are main key elements in LDO stability.

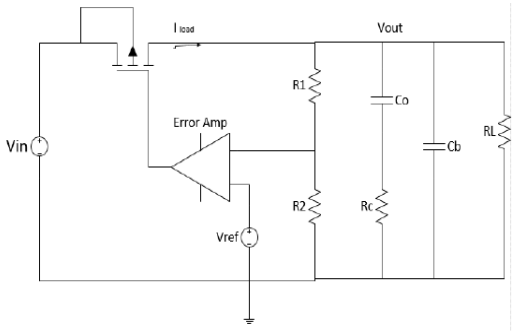

Fig 3. Conventional LDO with Load connected

$$G(s) = \frac{(1+S/W_Z)}{(1+\frac{S}{W_L})(1+\frac{S}{W_b})}$$
$$G_{dc} = \frac{R_L}{r_{ds} + R_L} \qquad (6)$$

The overall, Open loop transfer function of the plant is given by

$$TF = K_{dc} * \frac{(1 + S/W_Z)}{(1 + \frac{S}{W_L})(1 + \frac{S}{W_b})(1 + \frac{S}{W_{opamp}})} \qquad (7)$$

where K_{dc} is low frequency gain of the system. It includes PMOS gain $G_{dc,}$ feedback gain, and error amplifier gain.

$$W_L = \frac{1}{C_L[R_c + (r_{ds}||R_L)]}$$
$$W_Z = \frac{1}{R_c C_L}$$
$$W_{opamp} = \frac{1}{R_{op} C_{gs}} \qquad (8)$$
$$W_b = \frac{1}{C_b R_c (r_{ds}||R_L)/[R_c + (r_{ds}||R_L)]}$$

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where W_L is the pole due to load resistance and load capacitor, W_Z is the zero produced by ESR, W_{opamp} is the pole due to operational amplifier and PMOS interaction, W_b is the pole produced by combination of load and bypass capacitor. In coming section detailed analysis is provided about these poles and zeros.

III. COMPENSATOR DESIGN AND ANALYSIS

The calculated open loop transfer function is having three poles and one zero. W_{opamp} is insignificant to consider in stability analysis, because frequency of the pole is very high so it becomes insignificant pole. So Gain of opamp will be considered in the analysis. Load pole is the dominant pole which will impact stability. Below figure is the simplified load equivalent circuit.

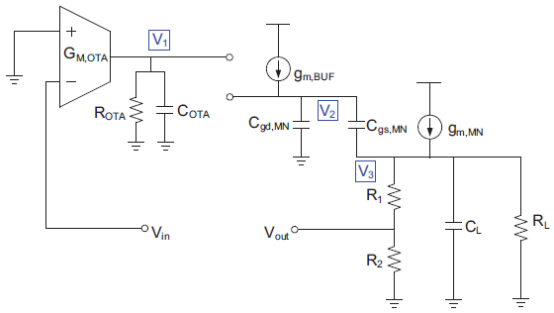

Fig 4. Small signal equivalent circuit of Conventional LDO

Equivalent impedance seen at output terminal is calculated as equation 7.

The Open loop transfer function (Eq 7) of the feedback loop has three poles, one (P_{int}) pole due to bypass capacitor, second pole (P_{load}) pole due to load, P_{opamp} pole due to opamp-PMOS interaction and one Zero (W_z) due to ESR of load capacitor. Pint is fixed at certain frequency, Z_{esr} depends on ESR value, so it is also static zero for certain conditions. P_{load} is variant to load current due to r_{ds} of PMOS and R_L are in their expressions. Since Z_{esr} is a high frequency LHP zero because ESR value is very low in the order of milli ohms, so it increases both gain and phase of system at a certain frequency range and possibly makes the feedback loop more stable. Choosing an output capacitor for LDO regulators with PMOS pass element can be difficult due to specific ESR requirements. The optimum ESR capacitors are necessary to get stable response of the system. If you choose ESR value according to your load capacitor range, then Z_{esr} will not impact the stability of the system.

The only problem creator to the stability of the loop is the output load pole P_{load}, why because it can change a lot with output load current range. Therefore, the compensation scheme must accommodate the P_{load} movement with load. In other words, the compensation should provide stability over the load variation or Line variation. The wide variation of load pole P_{load} creates difficulties for compensation. To overcome problem with this movement or variation of load pole, there are two possible solutions those might be effective are,

1. Making P_{load} always out of the expected bandwidth.
2. Accommodate P_{load} movement by adding a zero.

Solution 1 can be implemented by increasing the load current (in mA range) to move P_{load} to higher frequency why because from equation P_{load} is inversely proportional to i.e., increase in load current I_L cause to decrease R_L so that P_{load} frequency will increases. But this is not acceptable for the low quiescent current requirement in this design [6]. It can also be realized by some pole-splitting methods, which push the output pole out of the bandwidth. However, two reasons make this solution not suitable for this design. One is the gain of MOS power transistor in source follower configuration is near 1 which makes pole spitting very difficult. The other is the large load capacitor (*nF*) resulting the output pole at relatively low frequency. To push this pole to the higher frequency may require a very large spitting capacitor and high current consumption.

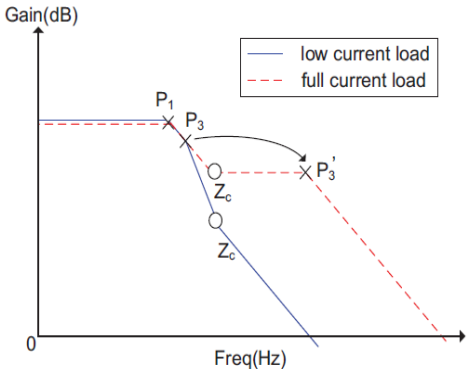

Fig 5. PZ compensator Solution II

Solution 2 can be conceptually shown in Figure 5, where Z_c is the zero added in the loop. It can be seen that as the load current increases, the output pole P_{load} moves to the higher frequency. However, due to the existence of Z_c, the loop is stable because the phase shift of Pint is compensated by Z_c. It is interesting to notice that as P_{load} goes to higher frequency, the bandwidth also gets extended. This may add advantages on transient performance as the bandwidth of the linear regulator is playing a role in line/load response. It seems that Solution II is a good candidate for the frequency compensation. To compensate this loop, the zero Z_c should meet two requirements: One is it must near the minimum frequency of P_{load} to ensure the low current load stability; the other requirement is the associated pole generated by adding zero Z_c should be outside the maximum close-loop bandwidth. The drawback of Solution 2 is the generation of low frequency Z_c needs large passive components (big resistor and big capacitor), which requires large silicon area. Also, adding Z_c through passive components will bring an associate pole with it [5][6] .

PZ compensator:

From above analysis it is clear that the Open loop plant is not stable for varying load currents, because of load pole movement. Henceforth to accommodate problem with load pole P_{load}, we need to introduce a ZERO before the P_{load} so that P_{load} will move out of the bandwidth. Another important performance metric for LDO is settling time, to get faster response bandwidth of LDO as high as possible. To get better bandwidth Gain curve of the system should roll off with slope of -20 dB. So system requires a POLE. By using this analysis, to get improved transient response PZ (pole-zero)

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compensation is necessary. One more important factor for second order system Integrator will provide better transient analysis with low steady state error. Finally, PZ compensator equation as follows:

$$Gc = Kc * \frac{(1 + \frac{S}{W_{zc}})}{(1 + \frac{S}{W_{pc}})} \quad (10)$$

The above equation represents PZ compensator of PMOS LDO. Kc represents the additional dc gain which will compensate for PMOS and Error Amplifier dc gain. W_{zc} and W_{pc} are the zero and poles of compensator. To find the appropriate locations of the Pole and Zero, it is required to follow below procedure:

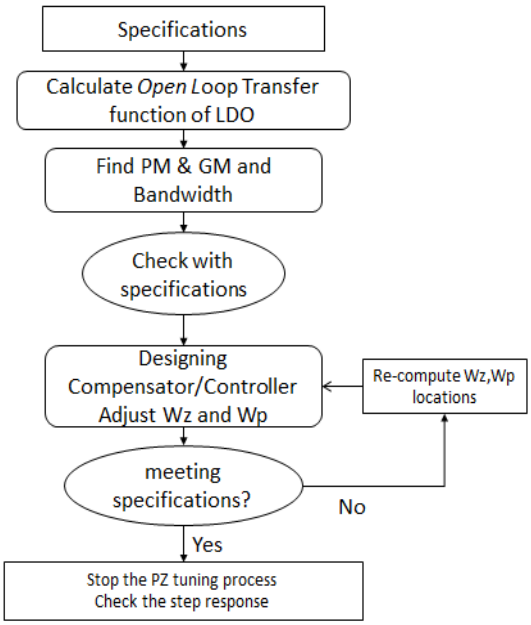

Fig 6. PZ-compensator Design flow

The above flow chart outlines the procedure to design the PZ compensator to satisfy steady-state error and phase margin requirements. First calculate the open loop transfer function (OLTF) then calculate Kc to satisfy the steady-state error. Then find out bode plot of the OLTF G(s) given in equation. Then determine the amount of phase shift in G(s) at the gain crossover frequency and calculate the uncompensated phase margin PM. Find the Phase angle of the system by using,

$$\theta = PM(required) + 10° - PM(uncompen) \quad (11)$$

Now tan angle of the above phase will give the location of the pole and zero. By using PID tuner in MATLAB, can calculate quickly. After finding PZ locations i.e., calculated compensator, multiply it with OLTF G(s), will get Plant OLTF (POLTF):

$$POLTF = G(s) * G_c(s) \quad (12)$$

Now again find PM and GM check with specifications, if the specs are reached then stop the PID tuning then find the step response of the closed loop system. Else recompute the PZ locations by changing gain of the system.

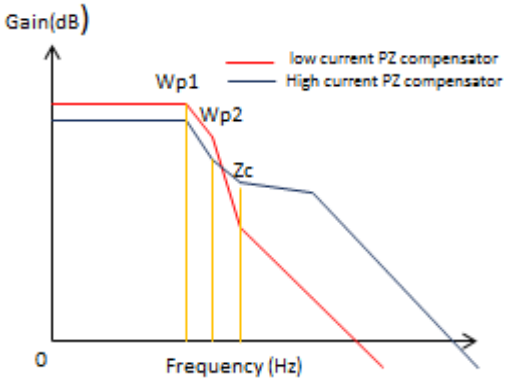

Fig 7. PZ – compensator BW improvement

IV. SIMULATION RESULTS AND DISCUSSION

This chapter presents the simulated results that characterize the LDO. The results are presented to cover several circumstances that the circuit could be subjected to. The simulation variations are presented with respect to PM and GM.

AC analysis:

In this section the AC analysis is performed for the generic process corner, due to the complexity of the circuit. The circuit is simulated and then get the "R_{ds}" information across different loads and V_{ID}'s. Based on R_{on} information computed plant open loop transfer function. Then designed controller or compensator to get required system specifications.

Table 1. Specifications for Analysis

V_{in}	1.15
V_{out}	1.0
V_{drop}	150 mV
RI	V_{out}/I_{load}
R_c(ohms)	2
g_m	123 mA/V
r_{ds}	65
R_1(ohms)	64 K
R_2(ohms)	36 K
C_o(F)	15e-9
C_b(F)	0.5e-9
I_{load}	1-10 A

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The above Table describes typical specifications.

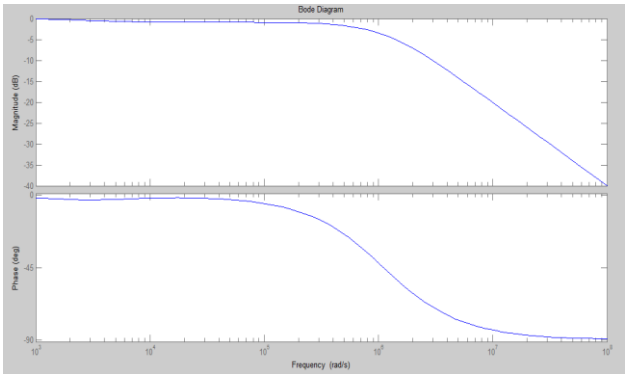

Fig. 8 Open loop Plant Uncompensated Bode plot

Figure 8 shows that Open loop plant bode plot, there we can observe that GM=infinite and PM = 180º that means this plant cannot improve the transient response at load current, so it is required to design a controller or compensator which brings open loop controller PM to required i.e., 45º. Figure 9 is Compensator bode plot, with PM = 134º at 4.92e9 rad/sec which boosts the Plant to required PM and Bandwidth.

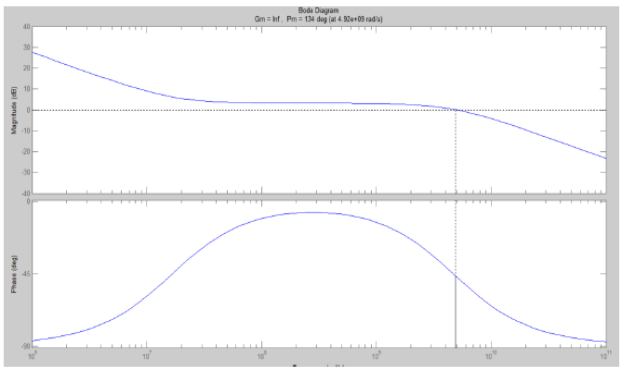

Fig. 9. PZ – Compensator Bode Plot.

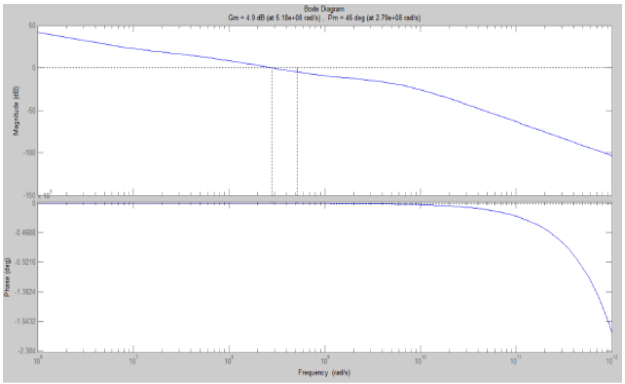

Fig. 10. Plot for compensated Bode plot

Figure 10 shows that plant is multiplied with compensator and gives the PM of 45º at 2.798e08 rad/sec and GM = 4.9 dB. Figure 12 is, which show step response of the system with time and frequency domain specifications, for this see Table 1.

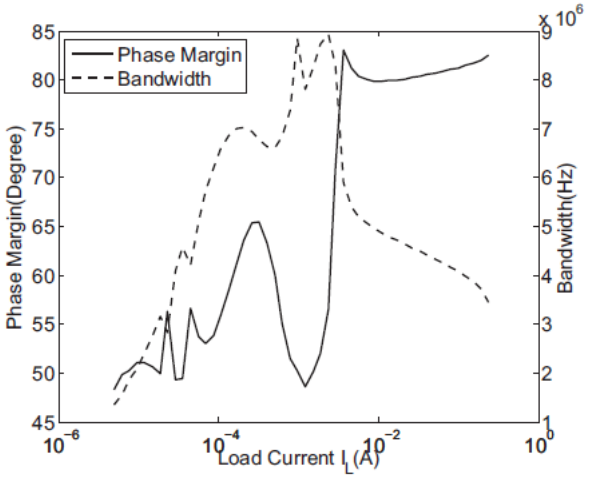

Fig 11: Phase and Gain Margin analysis with load current

Figure 11 shows the phase margin and bandwidth over all current load for regulation loop, it can be observed that the bandwidth of this loop is always higher than 1MHz. The minimum bandwidth is get at the current is at 250mA, which is around 3.5MHz. The bottleneck of the main voltage regulation loop bandwidth should be lower than this value.

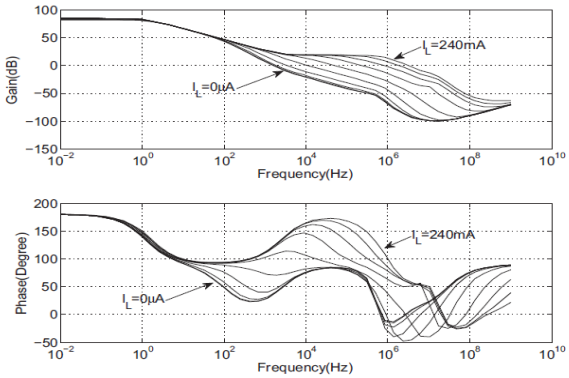

Fig. 12 Bode plot for different load currents

The above plot represents open-loop bode plot of LDO regulator with PID compensator over different load current is shown in Figure 12. As the load current increasing, the output pole is moving to higher frequency. Owing to the added zero and pole controller scheme, the system stability can be ensured.

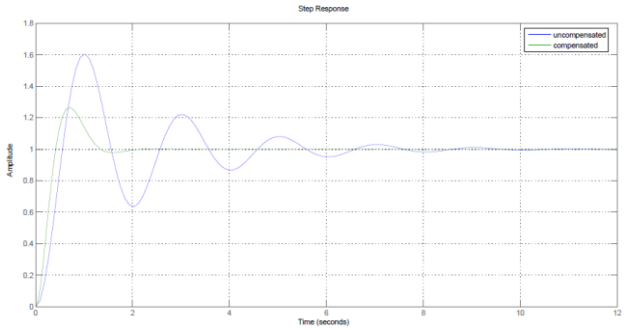

Fig 12: Step response of compensated and uncompensated closed loop system for I_L=3A and V_o=1V

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The Step response of overall closed loop is shown in Figure 12. The PM and Bandwidth of the closed loop step response is replicated in this plot. As I_L varies from minimum to maximum PM and Bandwidths are also increased, so that transient behaviour of the loop also improves.

Table 2. Time domain analysis

Open loop Plant Analysis	Rise Time (ns)	Peak Time (ns)	Settling Time (ns)	PM	GM	BW (MHz)
Without Compensation	80	100	200	35	1.2e4	200
With Compensation	50	75	95	45-60	4.9 dB	279

V. CONCLUSION

A PZ-Compensator is designed and analyzed in MATLAB. It is observed that this method is a simplest method to improve transient performance of LDO. It also showed that with this method response time decreased from 80ns to 50ns. In future, proposed method will be implemented with transistor level design and will verify droop and overshoot.

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