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A Novel SRAM Cell Design for Low Power Applications

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***Abstract*— In this paper, we initially discuss some of the SRAM designs available like 6T SRAM and 9T SRAM and go on to propose a new 9T SRAM based cell design which proves to be more efficient in terms of power consumption and average delay. We further extend the concept and propose a 10T SRAM cell and discuss the merits and demerits of such a design. The entire paper is written focusing mainly on low power implementation of SRAM.**

***Keywords*— SRAM, 9T SRAM, Low Power VLSI, Low Power SRAM, Memory, SRAM Cell, 45nm SRAM**

I. INTRODUCTION

With the advent of portable computers and mobile computational devices, there is an immense need for minimizing the power consumption of electronic circuits. This is the direct effect resulting from the reduction of device size which leads to smaller and low storage capacity batteries that power these devices.

Memories, owing to their high density and increased number of cells contribute a significant fraction towards power consumption of the device. In this paper, an attempt is made to propose a novel SRAM cell architecture that consumes less power than the conventional SRAM cell and which has improved delay characteristics than the conventional architecture.

This paper is divided into several sections as follows. Section 2 discusses the conventional 6T SRAM cell and the process of reading from and writing into that cell. Section 3 discusses the proposed 9T SRAM cell that offers a significant improvement in terms of delay and power consumption. We also discuss the optimum transistor size and supply voltage as supported by simulation results to achieve minimum power dissipation along with acceptable rise and fall times of the output. Section 4 mentions a variation of the proposed design and weighs in the merits and demerits of the same. Section 5 provides a comparative study of all the above mentioned SRAM cell designs. Finally, section 6 concludes this paper.

II. CONVENTIONAL 6T SRAM CELL

Figure 1 shows the schematic diagram of a conventional SRAM cell that is made up of 6 transistors (6T SRAM). It consists of a pair of cross coupled inverters and two pass transistors which allow read and write access to the cell. The main advantage of this cell is that it occupies little area and has lower values of rise and fall times. That is, the output reaches its final value at a much faster rate. The process of reading and writing into such a cell is explained below.

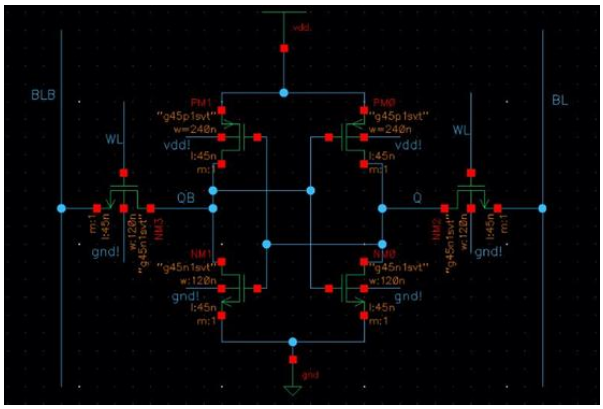

Figure 1: Conventional 6T SRAM

To write a value into the 6T SRAM cell shown in figure 1, the corresponding bit line is made high. That is, to write logical 1 into the cell, BL is made high while BLB is maintained low. To write logical 0 into the cell, BL is made low and BLB is made high. Word line WL is then made high which turns on the pass transistors NM2 and NM3. When BL=1 and BLB=0, NM1 and PM0 are turned ON so that Q is pulled high by PM0 and QB is pulled low by NM1. Thus, 1 is written into the cell. When BL=0 and BLB=1, NM0 and PM1 are turned ON so that Q is pulled low by NM0 and QB is pulled high by PM1. Thus, 0 is written into the cell.

To read a value from the cell, BL and BLB are pre-charged to HIGH and then word line WL is asserted. If 1 is stored in the cell, NM1 will be turned ON which pulls BLB to LOW. If 0 is stored in the cell, NM0 will be turned ON which pulls BL to LOW.[3]

III. PROPOSED 9T SRAM CELL

The 6T SRAM cell discussed above is a poor choice when it comes to low power applications. This is because, during the write operation, when the value stored in the cell is being flipped, momentarily there exists a direct path from VDD to GND which results in a large amount of short circuit power to be dissipated. This increases the overall power consumption of the circuit. A method to overcome this is suggested in [1] and is shown in figure 2. The method involves the use of an NMOS access transistor that is triggered by WLB that is placed between GND and NM0, NM1. By suitable turning the access transistor ON and OFF, short circuit current and thus

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the short circuit power can be reduced. Also, transmission gates are used instead of pass transistors NM3 and NM4.

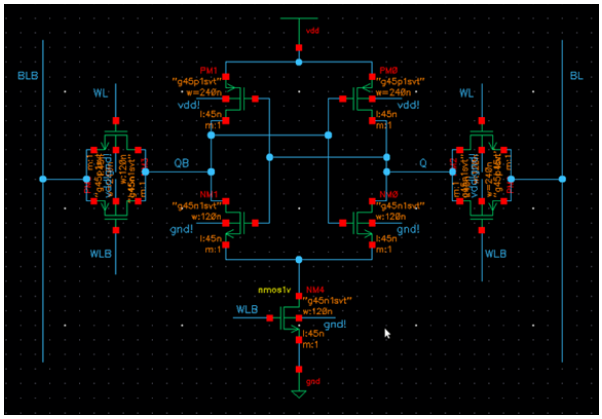

Figure 2: 9T SRAM as suggested in [1]

The two major problems associated with such a circuit are as follows. Firstly, during the read cycle, the access transistor remains OFF since WLB=0. Thus, there exists no path to GND that might pull one of the bit lines LOW. Thus, reading data from such a cell would be difficult. Secondly, during the write phase, one of the PMOS transistors will be ON which creates a direct path from VDD to the corresponding bit line. Thus, some current is drawn from the source to charge the intermediate parasitic capacitances and the bit line parasitic capacitance. This slightly increases the power consumed by the cell.

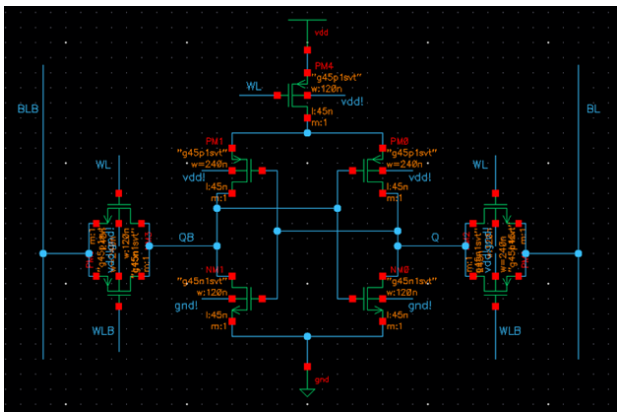

Figure 3: Proposed 9T SRAM

The above mentioned difficulties are overcome by the proposed design which is shown in figure 3. In this design a PMOS access transistor is used in between VDD and PM0, PM1 instead of the NMOS transistor. This cuts off any possible short circuit power dissipation that might occur when both NMOS and PMOS transistors are ON during switching operations. The simulation result clearly demonstrates the superiority of the proposed design when compared to other designs in terms of power dissipation.

The channel length of the MOSFETS has been optimized for low power requirements. It is kept to the technology library's minimum value (45nm in this study) as per [2]. The Wp/Wn ratio is also fixed at 2 as per [2]. The simulation result for power dissipation vs Wn is shown in figure 4.

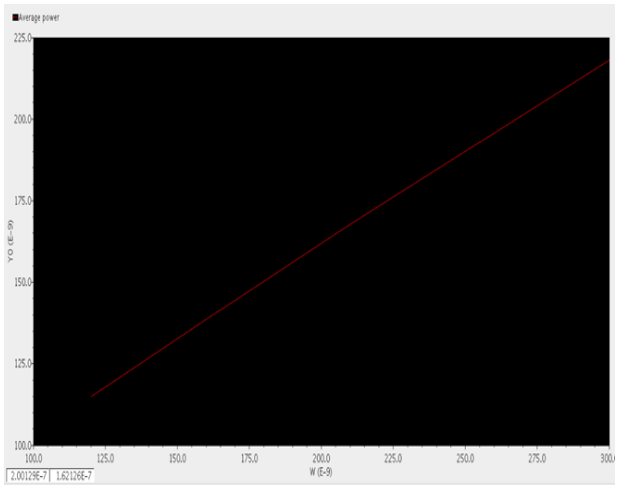

Figure 4: Power vs Wn

The graph clearly shows that power dissipation is minimum at minimum value of Wn. Thus, Wn is fixed at 120nm which is the lowest available at 45nm technology library. VDD should be kept as low as possible to achieve minimum power dissipation. But it should at least be 4Vt in order to avoid excessive delay introduced [2]. A plot of average rise and fall time vs VDD as shown in figure 5 indicates that at VDD=1 V, the rise and fall time are very close to its minimum value. Hence, VDD is fixed at 1 V.

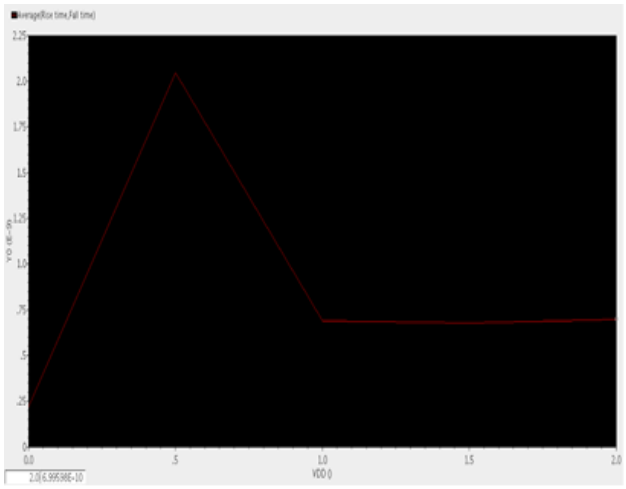

Figure 5: Average (Rise time, Fall time) vs VDD

IV. 10T SRAM CELL

A variation of the proposed 9T SRAM is shown in figure 6. This 10T SRAM design uses both NMOS and PMOS access transistors to limit the short circuit current. A considerable improvement in power dissipation is observed at the cost of rise and fall times. Also, the area occupied by the cell is increased as one extra transistor is introduced. The usage of such a cell can be restricted to designs which concentrate strictly on low power requirement and are not critical towards area or rise and fall delays. As explained in section 3, this cell also suffers from the problem associated with reading data. An alternate method of reading should be used to overcome this which adds an additional overhead on power, area and delay.

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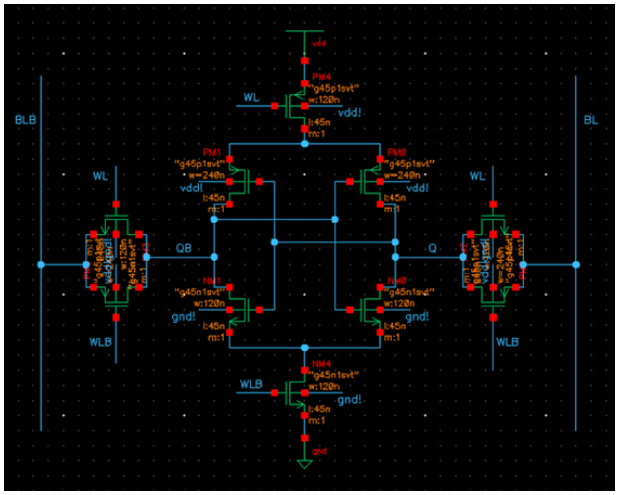

Figure 6: 10T SRAM

V. RESULTS

The proposed 9T SRAM cell was simulated using Cadence at 45nm technology. The resulting output waveforms are shown in figure 7.

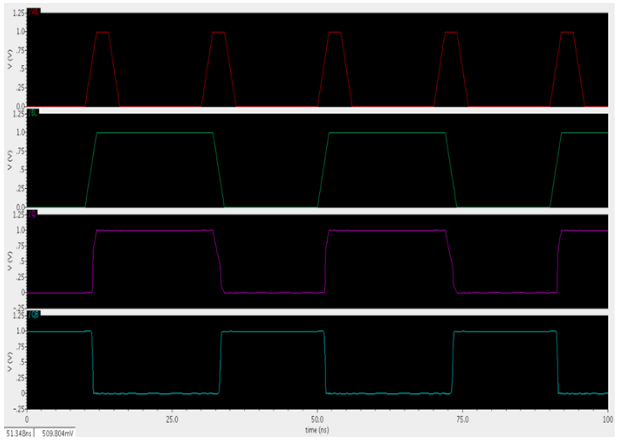

Figure 7: Output waveforms of proposed 9T SRAM

Figure 8 shows the power dissipation of the proposed SRAM cell. The power analysis is done using Cadence software and the graph in figure 8 depicts the total power dissipated.

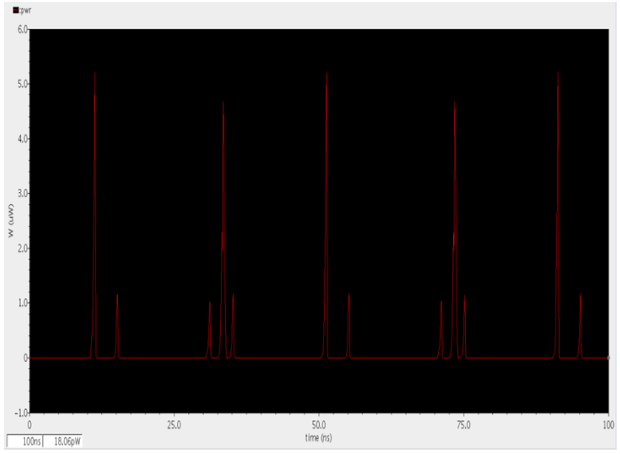

Figure 8: Total power dissipation in proposed 9T SRAM

Similar analysis has been performed on other SRAM cells that were mentioned above for the sake of comparison. Table 1 depicts the values of various parameters that were chosen for the study.

Table 1: SRAM cell parameters

	L	W_n	W_p/W_n	VDD
Conventional 6T SRAM	45nm	120nm	2	1 V
9T SRAM as mentioned in [1]	45nm	120nm	2	1 V
Proposed 9T SRAM	45nm	120nm	2	1 V
Proposed 10T SRAM	45nm	120nm	2	1 V

Details of power analysis and average delay of the above mentioned SRAM cells are shown in table 2. All simulations are performed using Cadence software at 45nm technology. From this table it is clear that 10T SRAM offers the best result at the cost of more area. For most of the applications, proposed 9T SRAM cell can be used that achieves less power dissipation as well as occupies lesser area.

Table 2: Simulation results of different SRAM cells

	Average Power(nW)	Peak Power(µW)	Average Delay(ps)
Conventional 6T SRAM	615.2	32.97	850.0
9T SRAM as mentioned in [1]	323.0	15.16	358.2
Proposed 9T SRAM	115.0	5.225	246.5
Proposed 10T SRAM	83.72	4.451	241.6

VI. CONCLUSION

From the above discussion, it can be concluded that the proposed 9T SRAM cell achieves excellent low power dissipation and low delay when compared to the other 9T SRAM cell. Also, it overcomes the problems of the 9T SRAM shown in figure 2 as explained in section 3. Thus the proposed 9T SRAM cell would be a better choice for low power applications.

We see a gradual improvement of power and delay as we move from 6T SRAM to 10T SRAM. This is achieved at the cost of area and rise/fall time. Ultimately, it is the application that dictates which SRAM cell should be included in the design of memories.

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