Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 5 Issue 02, February-2016

A Review Paper based on Built in Self Test

Ritu Singh Thakur
M. Tech Scholar ECE Department
Dr. C. V. Raman University
Bilaspur, India

Akanksha Awasthi
Asst. Prof. ECE Department
Dr. C. V. Raman University
Bilaspur, India

Ravish Gupta
Asst. Prof. ECE Department
Dr. C. V. Raman University
Bilaspur, India

***Abstract* - In the era of submicron technology memories may develop failure during the operation within their expected lifetime. The circuit needs to put on test mode and validates that whether it is free of fault or not, with the assumption that they would not damage within the expected life span, as the technology is shrinking assumption does not hold for the modern day. In the virtue of submicron technology to conquer such problem redundant circuitry kept on chips which replace the faulty part. It tests circuit every time before they start up. Module sensitizes the fault and propagates the effect to the output of CUT the main emphasis of the circuit design is to have low area and high speed, and low power. It generates many patterns for 0 to 2^n if there are n flip-flops. The BIST a redundant circuit kept on the chip which replaces the erroneous circuit with the error-free part. This paper concluded basic test problems and some reliable methods of solution are discussed. The basic concept of BIST is that it provides a path by which system could test it.**

Keywords- Built -in Self-Test, Boundary-Scan, Test Pattern Generation, Response Analysis, Scan Path.

I. INTRODUCTION

In very-large-scale integration (VLSI) a large number of transistors integrated into a single chip. VLSI started in the 1970s when the complexity of semiconductor and communication technologies was developed. It was very helpful when dealing with large no of transistors. A built-in self-test (BIST) is a mechanism that permits a machine to test itself. BIST have been designed to meet requirements such as High reliability, Low latency in the cycle and low Cost of testing during manufacture [1].

The Reduction in complexity and cost, therefore the dependency on the external source for testing is reduced. Cost can be reduced by two ways: Reduces the test cycle duration, Reduces the complexity of the test/probe setup, by reducing the number of I/O signals that must be driven/ examined under test control. Test pattern generator circuit and output analyzer are placed on the same chip to proceed in the testing process.

As the complexity of circuits continues to increase, a number of faults and the type of faults generated in the design so that it necessary to detect them on chip. Testing of integrated circuits using structurally based technique is being done. In this review paper, the testing using various testing methods has been studied. The basic part of this BIST is LFSR, CUT, and MISR etc. In the testing mode, a number of test pattern has been generated and applied to the circuit and compare with the error-free responses. [7] By this procedure the circuit under test is checked either it is working or not properly. To test the memory circuits' BIST is used and a large no of test patterns are generated to check it. For the industrial purposes, the modules are tested both after manufacturing and periodicals in the field. During testing, a number of tests are applied to check that the RAM operates normally. Testing verifies not only the correctness of the design function, but also the correctness of the fabrication process. It guarantees for the correctness of the function and fault free design. In addition, testing can also be used during the latter stages of the product lifecycle, in order to detect errors due to aging, environment or other factors. Testing a circuit every time before they start-up, is called Built-In-Self-Test (BIST). In this module, we studied the details of BIST. Once BIST finds a fault, the readjustment in connections to replace the faulty part with a fault free one is a design problem and would not be discussed here. The simulation has been done by using VHDL/Verilog HDL Modelsim and synthesize has been done by using the XILINX ISE Design Tool.

For the high density and high capacity, the embedded memory SoC's are implemented. Memories in modern SoC's occupy large areas and even a large number of active components. Memories are tightly constrained according to the technology, hence are more likely to fail. Due to this RAM is neither more accurate nor reliable. Hence, memories need to be designed in a balanced manner which brings the importance of BISR to the surface. Built-in self-repair (BISR) technique is widely used to rectify RAMs). To repair RAMSs with different sizes and a different number of redundancies a reconfigurable BISR scheme has been presented. An efficient BIRA algorithm for 2-D redundancy allocation has been presented. BIRA

(This work is licensed under a Creative Commons Attribution 4.0 International License.)

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 5 Issue 02, February-2016

hardware can support different type of RAMs on which the BIRA algorithm has been realized [16] [9]. Ellamar inferred that the transparent test approach is applicable to the idle state of systems. And the test time is reduced to avoid the lag. Transparent word oriented March tests are directly obtained by repeatedly executing the corresponding bit oriented March test on each bit of the word. In this system RAMs are of different size are used and each has different 4rwidth structure. This scheme tests a RAM utilizing an ALU module whose number of stages can be larger than the word width and that can be Used to test an array of RAM modules where the largest RAM word width does not exceed the number of stages of ALU [6]. Husin proposed single module of the Built-in-Self-Test (BIST) for Random access Memory (RAM) architecture. The main concern of the output response analysis in the BIST for RAM is TPG (test pattern generator) [7]. March TEST algorithm is provided to analyze the output of the counter. The ORA compares the output of the decoder and itself the RAM output which is formed according to the theory of numerical autonomy of error vectors from the circuit under test in the mean time. Pass or fail for the faulty detection of RAM will be shown at the output of ORA. A random access memory with built-in self-test has been successfully designed. The motive of studying the DFT method is obtained by reviewing various schemes such as built-in self-test and external test. The BIST techniques are also divided into online and offline testing [7].

II. BASIC ARCHITECTURE OF BIST

Offline testing using ATE is also counting as BIST both are equivalently same where the test pattern generator and the test response analyzer are on-chip circuitry (instead of equipment). As equipment are replaced by circuitry, so it is certainly defined that compressed implementation of test pattern generator and response analyzer are to be designed. The basic architecture of BIST is shown in Figure 1[1].

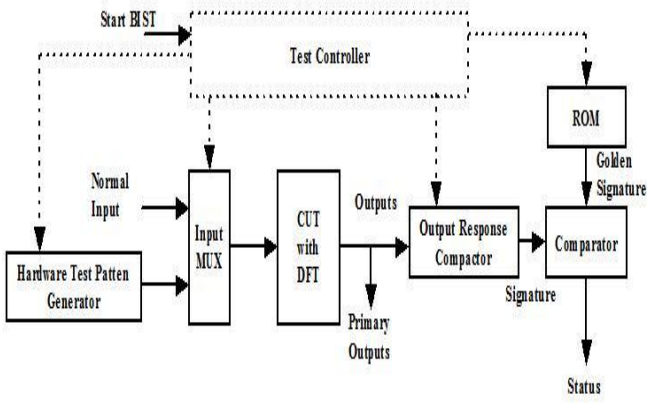

Figure1. Basic architecture of BIST

As shown in Figure 2, BIST circuitry comprises the following modules (and the following functionalities) [2]

There are two types of BIST architecture:
Centralized BIST, Disturbed BIST [7]

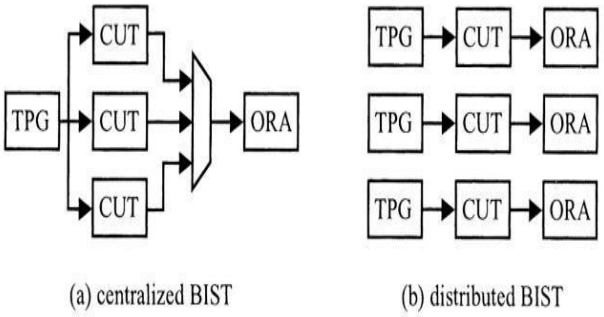

Figure2. Types of BIST

A. Hardware Test Pattern Generator

To sensitize the faults and propagate the effect to the outputs (of the CUT) this module generates the test patterns. The test pattern generator is a circuit. The area is limited hence, the store and then the generating of the test pattern is obtained by ATPG algorithms on the CUT (discussed in Module XI) using the hardware test pattern generator is not feasible. It can be said that the test pattern generator cannot be a memory where all test patterns obtained by running ATPG algorithms (or random pattern generation algorithms) on the CUT are stored and applied during execution of the BIST. Instead of the test pattern generator which is basically a type of register that synthesizes the random patterns which behave as test patterns. The main implication of the circuit design is to design for the low area yet generate as many different patterns (from 0 to 2n, if there are n flip-flops in the register) as possible.

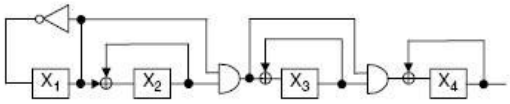

Figure3. Example of Binary Counter

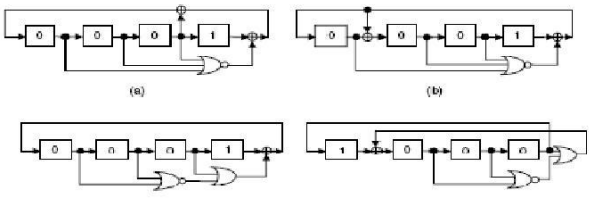

Figure3. Example of LFSR

B. Input Multiplexers

The multiplexer allows normal inputs into the circuit when it is functional and test inputs from the pattern generator when BIST is executed. A central test controller feeds the input of the multiplexer

(This work is licensed under a Creative Commons Attribution 4.0 International License.)

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 5 Issue 02, February-2016

C. Output Response Compactor

Lossy compression of the outputs of the CUT is done with the response of the compactor. In BIST the output of the CUT is to be compared with the expected response (called a golden signature) in the case of off-line testing, when the CUT output does not match the expected response, hence the fault is detected. Same as the situation for test pattern generator, expected output responses cannot be explicitly stored in a memory and is compared with the responses of the CUT.

The output responses of the CUT to the test patterns are "compacted" into a "signature" which is compared to the expected signature for the fault-free circuit in most ORA techniques. As the result, the Pass/Fail detection is often composed of a set of bits of data that have the signature of the BIST sequence, then a single Pass/ Fail bit. It must be noted that the term compaction is used as the compression since compression is meant by no loss of information; since most ORA techniques pertain to some loss of information; compaction is a more accurate term [3].

D. ROM

It stores the golden signature, which needs to be compared to the compacted CUT response

E. Comparator

Hardware is meant to compare compacted CUT response with a golden signature (from ROM).

F. Test Controller

Whenever an IC is powered up (signal start BIST is made active) the test starts the BIST procedure to control the BIST. When the test is finished and status line becomes high if the fault is found. Following that, the controller connects normal inputs to the CUT via the multiplexer, thus making it ready for operation. Among the modules discussed above, the most important ones are the hardware test pattern generator and the response compactor. This includes the standard digital blocks. In the next two sections we will discuss these two blocks in details. The other ones are standard digital blocks [4].

REFERENCES

[1] Nptel.ac.in/courses/106103016/30
[2] M. Abramovici, M. Breuer and A. Friedman, Digital Systems Testing and Testable Design, Piscataway, New Jersey: IEEE Press, 1994.
[3] E. McCluskey, “Built-In Self-Test Techniques,” IEEE Design & Test of Computers, Vol. 2, No. 2, pp. 21-28, March 1985.
[4] R. A. Frohwerk, “Signature Analysis: A New Digital Field Service Method,” Hewlett-Packard Journal, vol. 28, no. 9, pp. 2–8, May 1977
[5] ShaikKarimullah G1, Abdul Rahim b C. Ushasree2.” Design and verification of online BIST for Different word sizes of memories.”
[6] Mrs. S. Ellammal M.E1, T.Saranya2” Transparent Test Scheme in Online BIST for Word-Oriented Memories” ISSN 2278 – 0882
[7] M.H. Husin, S.Y. Leong, M.F.M. Sabri, R. Nordiana “Built in self test for RAM Using VHDL” 2012 IEEE Colloquium on Humanities, Science & Engineering Research (CHUSER 2012), December 3-4, 2012,
[8] Andreas Steininger” Testing and Built-in Self-Test” Institute für Technische Informatik, Vienna University of Technology A-1040 Vienna / Austria, Treitlstrasse 3
[9] V.SRIDHAR 1 M.RAJENDRA PRASAD” Built-in self-repair (BISR) technique widely Used to repair embedded random access memories (RAMs)” International Journal of Computer Science Engineering (IJCSE)
[10] Version 2 IEEE IIT, Kharagpur” Built-In-Self-Test (BIST) for Embedded Systems”
[11] U.Siva Nagaraju, Dr.A.sahaya Anselin Nisha Diagnosis and Fault Tolerance for Embedded Bist RAM International Journal of Scientific Research, Vol.III, and Issue. IV Apr 2014
[12] Amit Bhanwal, Mayank Kumar, Yogendera Kumar,” FPGA based Design of Low Power Reconfigurable Router for Network on Chip (NoC)”, ISBN: 978-1-4799-8890 ©2015 IEEE, International Conference on Computing, Communication Automation (ICCCA2015).
[13] Madhuraj, Prince Kumar Pandey, Mayank kumar,”FPGA Implementation of Convolution using Wallace Tree Multiplier,” International Journal of Engineering Research & Technology (IJERT) ISSN: 2278-0181 IJERTV3IS061634, Vol. 3 Issue 6, June – 2014.
[14] Mayank Kumar, Mharban singh, Rajiv Kapoor,”Area & Dynamic Power Optimization of CMOS 1-Bit Full Adder Using Genetic Algorithm,” International Journal of Engineering Research & Technology (IJERT) ISSN: 2278-0181 IJERTV3IS061634, Vol. 3 Issue 5, may 2014.
[15] Akash Kumar, Mayank Kumar, Varun Kumar, Sushant Shama4.” Design of a Single Precision Floating Point Unit in Verilog,” IJSRD - International Journal for Scientific Research & Development| Vol. 2, Issue 03, 2014 | ISSN (online): 2321-0613.
[16] Sony Rama, Kishore Kumar and P.Rajesh Kumar . Sony Comp. Sci. & Engg. Elixir ISSN: 2229 -712x 41 (2011) 5579
[17] Chih-Sheng Hou, Jin-Fu Li, Member, IEEE, and Tsu-Wei Tseng IEEE transactions on computer-aided design of integrated circuits and systems, vol. 30, no. 11, November 2011

(This work is licensed under a Creative Commons Attribution 4.0 International License.)