A Review Paper on Design of Efficient two Stage Power Amplifier using 65nm CMOS Technology

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***Abstract*— In the modern Era, VLSI design is one of the paradigms to have low noise, high power and small chip area. The design of CMOS power amplifier is an effort in this domain which is applicable for wireless communication system. The proposed design employ switching mode of two stage power amplifier to exploit its soft switching property to achieve high output power and high efficiency.**

The two stage power amplifier for various communication applications in 65nm CMOS technology is proposed to be designed. The functionality of proposed design of two stage power amplifier will be verified for parameters like high output power and high efficiency. The main emphasis is on achieving high gain with low return losses.

The layout of the proposed two stage power amplifier will be tried to have minimum design area with improved parameters as compared to previous literature reviewed designs.

I. INTRODUCTION

In the modern Era, VLSI design is one of the paradigms to have low noise, high power and small chip area. The design of CMOS power amplifier is an effort in this domain which is applicable for wireless communication system.

RF amplifiers are electronic devices that accept a varying input signal and produce an output signal that varies in the same way as the input, but that has larger amplitude. RF amplifiers generate a completely new output signal based on the input, which may be voltage, current, or another type of signal. Usually, the input and output signals are of the same type; however, separate circuits are used. The input circuit applies varying resistance to an output circuit generated by the power supply, which smoothes the current to generate an even,uninterrupted signal. Depending on load of the output circuit, one or more RF pre-amplifiers may boost the signal and send the stronger output to a RF power amplifier (PA).

CMOS power amplifiers are integral parts in various analog and mixed-signal circuits and systems. The two-stage power amplifier is widely used because of its structure and robustness. In designing power amplifier, numerous electrical characteristics, e.g. gain, operating voltage, operating frequency, maximum output power all have to be taken into consideration.

In the proposed design our main aim is on implementation of high efficient two stage power amplifier in VLSI for various communication applications. We are using 65 nm CMOS technology for design of two stage CMOS power amplifier.

1.1 Block Diagram:

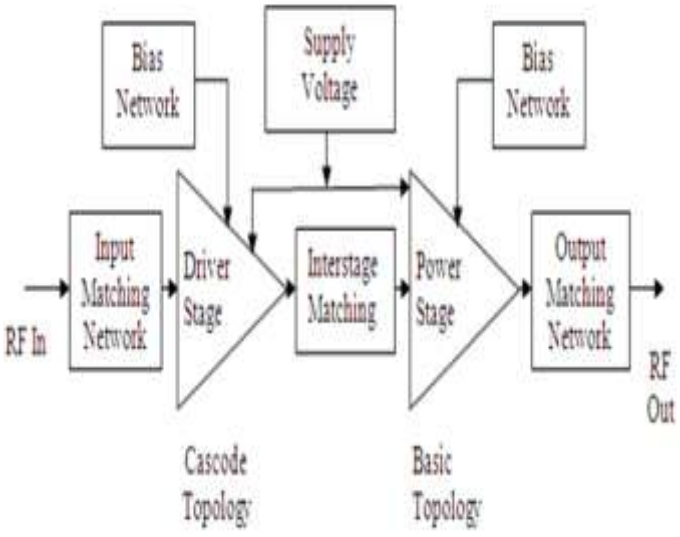

Figure 1.1. Block Diagram Of Complete Two Stage CMOS Power Amplifier

The above figure shows the functional block diagram of the designed two stage Power Amplifier. Input matching and Output matching networks are used at input and output stage respectively to minimize return losses which results in increased gain and output power. Input matching is done by calculation of input impedance using the ratio of the input voltage and input current. Passive elements having some impedance are connected at the input side forming a input matching network to match this impedance. The loss occurred in this part of the circuit due to improper matching is known as Input return loss and denoted as S(1,1). The same concept is utilized to find S(2,2) at the output side. An interstage matching network is also used as two stages are used for power amplification. Driver stage and Power stage with the supply and bias network are main blocks of the power amplifier. A cascade topology is used in the driver stage and a basic power amplifier topology is used in the power stage.

II. RELATED WORK

In the year of 2002, IEEE Journal of solid state circuits, Fully Integrated CMOS Power Amplifier Designed Using the Distributed Active-Transformer Architecture. A novel fully integrated single-stage circular geometry active-trans- former (DAT) power amplifier implemented in a low-voltage CMOS process achieves 1.9-W output power with 41% (31% single-ended) PAE at 2.4 GHz. It had used as a 450-mW 2.4-GHz amplifier with 27% PAE using a 1-V supply. The circuit includes input and output matching to 50 , requiring no external components & output matching had been fabricated using 0.35-µm CMOS transistors. It achieves a power added efficiency (PAE) of 41% at this power level. I.[1]

In the year of 2007 IEEE Custom Intergrated Circuits Conference (CICC), A fully integrated 90nm CMOS PA capable of delivering 6.7 dBm of linear power in the 60 GHz band has been demonstrated. The PA has a measured efficiency of 20% and is appropriate as a pre-driver or for short range mm-wave transmitter applications. This amplifier can be used as a pre-driver or as the main PA for short range wireless communication. The output power had been boosted with on-chip or spatial power combining.[2]

In 2010 IEEE International Conference, The paper presented a 2.4 GHz fully integrated CMOS power amplifier using capacitive cross coupling, fabricated in 0.18 µm CMOS with 3.3V supply voltage.PAE_{max} and PAE at 1db compression point are 34.3% and26.8%. P_{1db}, P_{sat} and PG are 25.2dBm, 27.7dBm and26.5dB.[3]

In October 2012, a fully integrated linear and efficient PA in 0.25- µm SiGe:C BiCMOS technology is presented and works at 2 GHz with a supply voltage of 2.5 V. The experimental results show a gain of 13 dB and a maximum output power of 23 dBm with a PAE of 38%.The efficiency enhancement is achieved using a switchable biasing and a reconfigurable output-matching network based on the available input power which is monitored by an on-chip envelope detector.[4]

In other October 2012 paper, the amplifier presented in this paper operates in saturation mode and regulates its bias current. The op-amp has 450mW power as well as 1.5V voltage. Its slew rate is 10volts/us than reported 450mW power & 1.5 V voltage amplifiers at 0.5 um technology. The amplifier presented in this paper operates in saturation mode and regulates its bias current. When a signal is applied the current in the amplifier increases so that these amplifiers have very high driving current. The op-amp has low power as well as low voltage. [5]

In August 2013 paper, Authors had used 0.13µm bandwidth to achieve Output power of 20.028 dBm with high efficiency of 44.669% is obtained at 1dB compression point using CMOS device for the power amplifier. Driver stage as the input stage and power stage as the output stage are the two stages. A cascode topology is used in the driver stage and basic topology is used in the power stage [6]

In the Solid State Circuits, IEEE journal presents a 1 W, Class-E power amplifier That implemented on 0.35 µm CMOS technology. At 2V supply and 1.98 GHz, The power amplifier achieves 48% power –added efficiency.[7]

As an improvement to the above literature reviews we will design a two stage power amplifier by using 65 nm CMOS technology for various communication applications.

III. DESIGN METHODOLOGY

Design Flow Graph:

Following steps are involved to obtain the proposed design.

- Schematic design for two stage power amplifier.
- Design for the driver stage of amplifier will be implemented first..
- Above design will be followed by design for the power stage of amplifier.
- Then it will be followed by impedance matching.
- Then biasing of circuit will be done.
- Finally simulation result will be achieved.

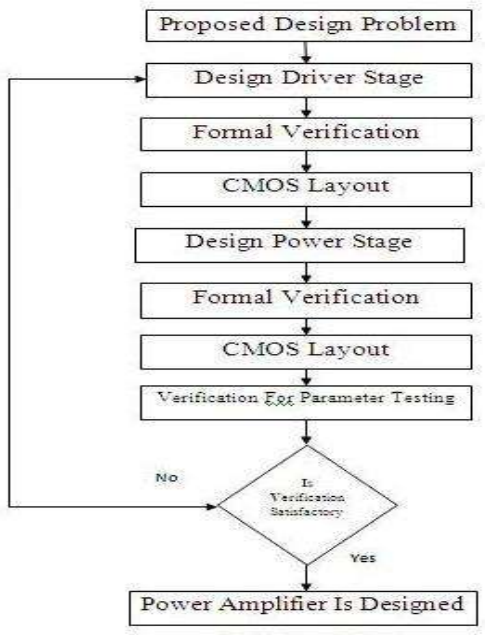

Figure 3.1: Flow Graph

CONCLUSION

Various papers concluded that power amplifier is designed using different CMOS technology. As an improvement to the above literature reviews we will design a two stage power amplifier by using 65 nm CMOS technology for various communication applications.

Here we will design two stage power amplifier with improved parameters such as operating voltage, gain, frequency, efficiency with low retuen loss. We will try to find better result as compare to various literature.

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