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A Self Timed Design with Enhanced Multi Threshold Approach

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***Abstract*—This paper enumerates the design of an ultra low-power self-timed architecture called Enhanced Multi-Threshold NULL Convention Logic (EMTNCL), which integrates Multi-Threshold CMOS (MTCMOS) with NULL Convention Logic (NCL), to capitulate significant leakage power diminution without any of the hindrances of applying MTCMOS to synchronous architectures. In contrast, the proposed EMTNCL architectures are smaller compared to conventional versions of CMOS, NCL and MTNCL and exploits high-V_t transistors to curb the stand-by leakage current during sleep mode whilst low-V_t transistors provide fast switching operations. The proposed EMTNCL exploits transistor sizing approach to achieve low power in deep sub micron technology.**

Keywords—Low-power; VLSI; Leakage Power; CMOS; MTCMOS; DI; NCL; MTNCL; EMTNCL.

I. INTRODUCTION

Designing low-power VLSI system has become a momentous goal because of the advance in computation and communication technology. The advances in electronic devices are not commensurate with the advances in battery operated technology. So in designing more constraints are faced; high speed, high gains and at the same time, low power consumption [1-3]. Historically, high speed is defined as performance metric by VLSI designers. High gains have been made for electronic circuits in terms of performance and area which are two conflicting constraints. The power consumption can be reduced by scaling the supply voltage. From half-sub-micron technology, scaling of supply voltage with feature size was embarked linearly. But scaling of supply voltages result in exponential increase of the sub-threshold leakage current caused by charge flow through a cell even if it is purportedly turned off [3, 4]. Hence, efficient leakage power reduction techniques are very decisive for the deep-submicron and nano-scale topologies.

Multi-threshold voltage CMOS (MTCMOS) technology is an appealing solution at circuit-level which provides a low-power and high-performance topology without any area overhead in deep submicron technology as compared to traditional CMOS logic style [5, 6, 9, 14]. Multi-threshold voltages are provided for each transistor in modern process technology. Delay-insensitive (DI) self-timed NULL Convention Logic (NCL) circuits, designed using CMOS design style, exhibits innate switching behavior since they only clasp when useful work is being done; however during idle/wake-up mode, there is still substantial leakage power. In this paper we incorporate the MTCMOS technique with NCL design methodology to sleep the NCL circuit during stand-by mode to capitulate a fast ultra-low power self-timed design topology at nano-scale, called Multi-Threshold NULL Convention Logic (MTNCL) [14-16, 18-22]. This paper outlines as follows: section 2 presents the overview of NULL convention logic and explains briefly about the MTNCL design methodology. Section 3 explain briefly about the proposed enhanced MTNCL (EMTNCL) to achieve better performance of the circuit and also the static implementation of EMTNCL full adder and a shift register is shown. While in section 4, the simulated results of all the 27 EMTNCL threshold gates, full adder and shift register are compared with respect to traditional CMOS logic, NCL and MTNCL in terms of power consumption and propagation delay and finally conclude in section 5.

II. LITERATURE SURVEY

A. NULL Convention Logic (NCL)

NULL Convention Logic is an appealing self-timed asynchronous design template [5]. To achieve self timed behavior, it states every logic gate by the logic itself. NCL uses multi-rail schemes based on delay-insensitive model, like dual-rail deigns with three valid states and an illegal state as shown in table 1. The control signal is the NULL instead of clock, unlike Boolean logic gates [5-12].

Table I: Dual Rail Encoding Scheme

STATE	RAIL-0	RAIL-1
NULL	0	0
DATA-0	0	1
DATA-1	1	0
ILLEGAL	1	1

NCL employs 27 basic fundamental threshold gates to construct a set of operations with four or fewer variables [12, 13]. To follow/achieve DI, all the threshold gates are implemented with hysteresis state- holding behavior. Fig.1 shows the symbol of basic THmn threshold gate with n inputs and threshold m, where m represents the number of DATA inputs required to assert the gate [7, 8].

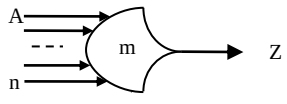

Fig. 1. THmn Threshold Gate

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Several CMOS implementations have been proposed such as dynamic, semi-static and static [7]. Among these the static implementation of NCL has more potential benefits than the other two as they can be operated at low threshold and holds the state-information [11]. Whilst the dynamic designs are not a DI since it does not hold state information and the semi-static approaches uses a week inverter which is responsible for huge amount of power dissipation. Thus the static implementations of threshold gates are impending in the NCL design flow [13].

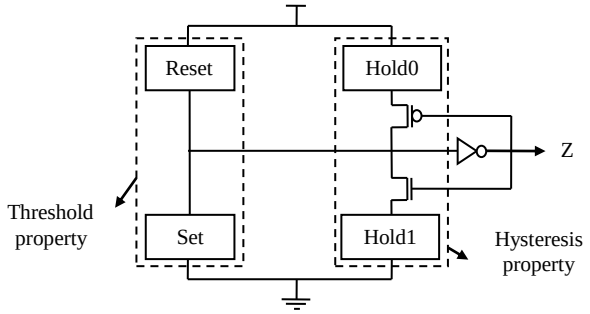

Fig.2. General architecture of Static-CMOS NCL threshold gate

The static-CMOS architecture of NCL threshold gate is shown in fig.2, where it composes of four blocks: SET, RESET, HOLD-0, and HOLD-1. SET block asserts the output to a DATA value when the number of valid DATA inputs equals/exceeds the value 'm', RESET is used to de-assert the output, HOLD-0, used to hold the asserted DATA and HOLD-1 is used to remain gate output in de-asserted state. To achieve DI self-timed behavior, NCL make use of NULL as its control element, where it is construe as a stand-by/no-active state means that when the output of a combinational circuit is NULL, the next DATA wave-front is propagated [10-13].

B. Multi-threshold NCL (MTNCL)

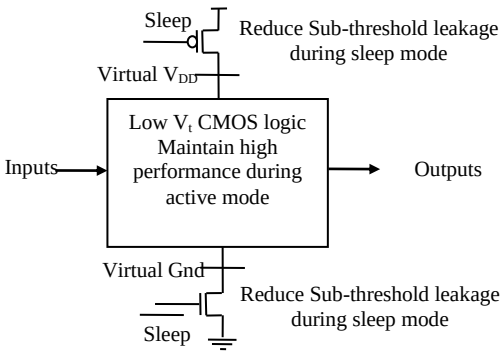

Fig.3. MTCMOS architecture

MTCMOS is a gate level abstraction commenced as an effectual way to reduce leakage current during stand-by mode without impacting latency of the system [14, 17]. MTCMOS circuits exploit diverse electrical properties of transistors with different threshold voltages (V_t), where V_t is the minimum operating voltage (V_{DD}) required to construct a conductive channel between drain and source diffusion regions. High-V_t (HVT) transistors have high off-resistance and less leakage but endure from slow switching speed while the Low-V_t transistors offers low off- resistance and high leakage current but are faster while switching [13-16]. MTCMOS design exploits HVT cells as power gating sources during stand-by state to trim down leakage power and to achieve high performance; it utilizes LVT cells as switching sources during active mode [16]. The general structure of MTCMOS architecture is shown in fig.3.

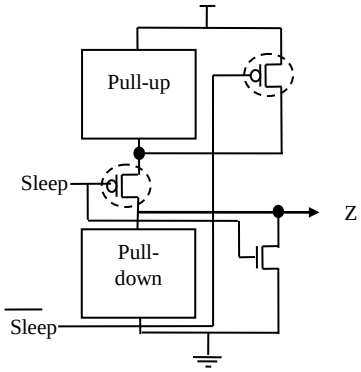

Fig.4. Fine Grained MTCMOS implementation

The SLEEP signal shown in fig.4 is designed to control the circuit operation. During stand-by mode, the SLEEP signal is emphasized causing HVT cells to turn off and permits low leakage current [14, 17]. When in active mode, the SLEEP signal is de-asserted for fast switching operation. In spite of its ease in design concept, implementing this technique involves many design contemplations that may impede its prevalent use. Moreover this design requires a complex logic circuitry to envisage the wake-up and stand-by events [18].

During the wake-up mode, the MTCMOS circuits generates more glitches which causes more power to dissipate and noise due to charging and discharging of virtual power line capacitance that require careful scaling for SLEEP transistors, a difficult chore in large scale designs (LSD) [15, 19]. This hindrance can be shunned if MTCMOS is implemented in fine-grained self-times asynchronous architecture. However, NCL gates consume more area overhead when realizing complex Boolean functions. To shun this effect, MTCMOS is exploited in every threshold NCL gate, called Multi-Threshold NULL Convention Logic (MTNCL) [15-19]. Incorporating asynchronous NCL with MTCMOS technique would yield area efficient, glitch free design, unlike conventional clocked synchronous architectures [18-22]. Sleep transistors can be exploited globally from the previous resisters output in fine-grained approach. By exploiting fine-grained methods the fundamental blocks are reduce to two due to the presence of control SLEEP signal [19].

III. PROPOSED ENHANCED MULTI THRESHOLD NCL (EMTNCL)

The scaling of individual transistor is a significant factor for power consumption and performance. Therefore in designing MTNCL, transistor sizing with energy-efficient characteristics is of primary concern. In this paper, we present a direct approach to transistor sizing for low power consumption. In contrast to the existing paradigms, the proposed architecture is scaled on critical and non-critical paths for ultra low power consumption.

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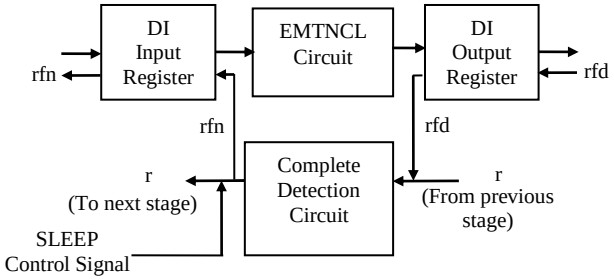

Fig.5. EMTNCL system frame work

The generalized frame work for the proposed architecture is shown in fig.5, where in stand-by (SLEEP) mode the system remains in no-DATA state or in-active state. To process a new valid rail from its DATA wave-front, firstly all the outputs of the EMTNCL architecture should be NULL. To achieve this constraint, the proposed EMTNCL must possess a set of registers at both input and output of the combinational EMTNCL circuit to control DATA flow and a complete detection circuitry, (CDC) for detecting circuit mode [17, 18]. The output from the CDC can be scrutinized as a request signal 'r', either requests for NULL (rfn) or requests for DATA (rfd). During wake-up mode, the CDC which is present in every stage, examines all the incoming input signals and request signal from next stage. If the incoming signals to the input register are NULL and the stage is requesting for DATA, then CDC of that stage propels a request-for-DATA to its previous stage. Thus based on the request signals DI registers interact with each other to achieve synchronization and self-timed operation. The performance of this system depends on the latency of every stage of CDC achieving glitch free and faster operation [19, 20].

A. Transistor level implementation of EMTNCL

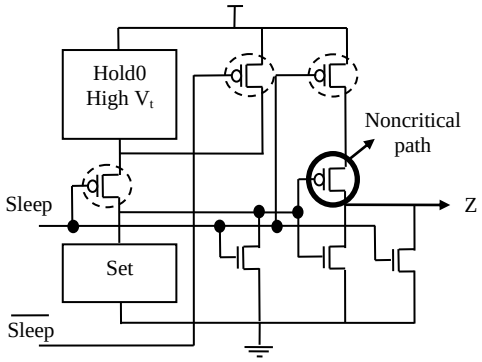

Fig.6. EMTNCL Architecture

The static implementation of EMTNCL is shown in fig.6 where the critical path and noncritical paths are sensitized. During SLEEP mode the EMTNCL gates produces NULL outputs through RESET block where the SLEEP control signal forces the output of EMTNCL gates to NULL. In addition, the handshaking (Return-to-One) protocol in NCL circuits entails that every two valid DATA be estranged by NULL value. Therefore, both HOLD-1 and RESET blocks are no longer desired. However this proposed technique produces unwanted transitions during wake-up events due to internal capacitance when the DATA wave-front arrives [20, 22].

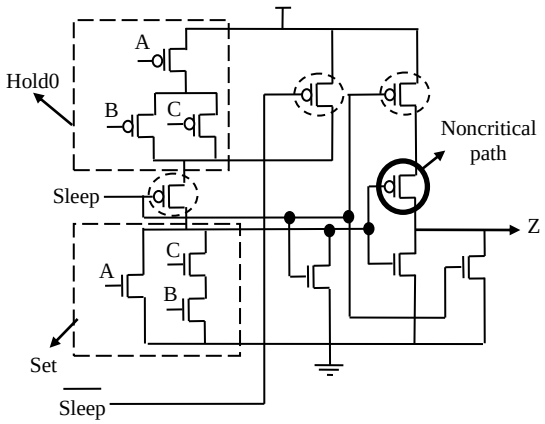

Fig.7. Transistor level implementation of TH23W2 EMTNCL Gate

The static TH23W2 EMTNCL gate is shown in fig.7, where n=3 and m=2. Assume the inputs of the gate are being NULL. Now if a valid DATA is sent through A, the gate meets its threshold, m=2 and produces valid DATA at the output. Similarly if a valid DATA is passed through rail B, the gate remains in NULL state since threshold is not met. Thus a complete DATA wave-front is propagated. Consecutively a NULL wave-front is generated when all the inputs of the gate are being NULL. Thus a complete NULL-DATA-NULL cycle is transmitted supporting Return-to-Zero (RTZ) protocol.

B. Implementtaion of static-EMTNCL Full Adder

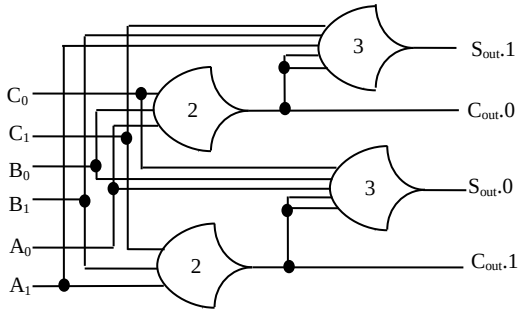

Fig.8. Gate level implementation of a Full Adder

In this paper, we present a gate level implementation of full adder using static EMTNCL approach. The sum of the inputs 'A' and 'B' is written to output Sum, S and generates a carry, C. The EMTNCL full adder exploits four static threshold gates to add the valid DATA where the inputs are given from input registers from alternating NULL/DATA wave-fronts. To produce a valid sum, all the inputs must me be propagated from the DATA wave-front or the corresponding register is requesting for the DATA to pass. After the valid DATA (sum, carry) is sent, the output register requests NULL from the NULL wave-front. Due to its hysteresis property, it does not produce NULL until all the inputs are being NULL. Now the complete detection circuitry detects for DATA and sends a request for DATA to the DI register. Thus complete DATA/NULL wave-fronts are propagated there by reducing unwanted switching results in low-power consumption.

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International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 5 Issue 01, January-2016

C. *Implementation of static EMTNCL Shift Register*

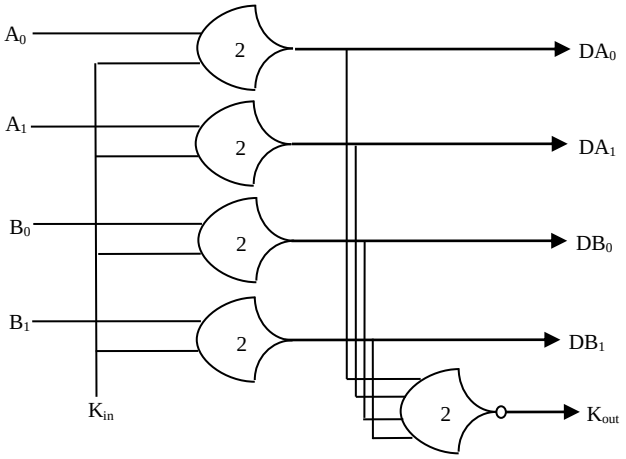

Fig.9. Gate level implementation of a Shift Register

NCL systems consist of at least two DI registers, one at the input and other at the output. The register interacts with each other as per the request and acknowledges signals. NCL registration is realized through cascade arrangement as shown in fig.9. This consists of TH22 gates to pass the DATA when K_{in} requests for valid DATA or NULL. This also consists of a NOR gate to generate the valid DATA/NULL. For example if the gate is reset to NULL then it produces logic zero. A 2-bit register stage, comprised of 2 single-bit dual-rail NCL registers, requires 2 completion signals, one for each bit. The NCL completion component uses these 2 K_{out} lines to detect complete DATA and NULL wave-fronts at the output of every register stage and request the next NULL and DATA set, respectively. In full-word completion, the single-bit output of the completion component is connected to all K_{in} lines of the previous register stage.

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

In this work, EMTNCL gates are designed and simulated to evaluate the average power and propagation delay. The proposed EMTNCL threshold gates are evaluated with traditional CMOS, NCL and MTNCL designs. To scrutinize the performance of proposed EMTNCL paradigms to other conventional designs, we have carried out simulation on Tanner EDA with 250nm technology. Each threshold logic gate has been designed and analyzed in terms of average power, propagation delay. The evaluated results are tabulate and the waveforms are collected.

A. *Simulation results for proposed EMTNCL Full Adder*

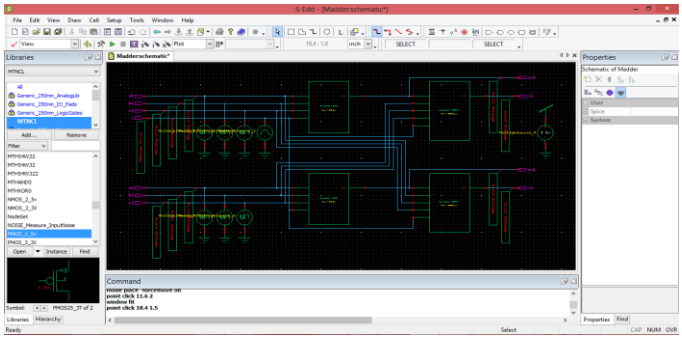

Fig. 10. Gate level implementation of Full Adder

The simulation for proposed enhanced MTNCL full adder has been performed using Tanner tool. Fig. 10 shows the Full Adder compilation with zero errors and zero warnings while fig. 11 shows output waveform of Full adder which verifies the truth table.

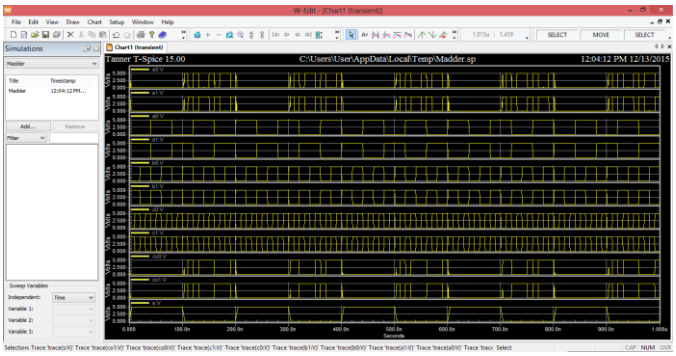

Figure 11: Output Waveforms for Full Adder

B. *Simulation results for proposed EMTNCL Shift Register*

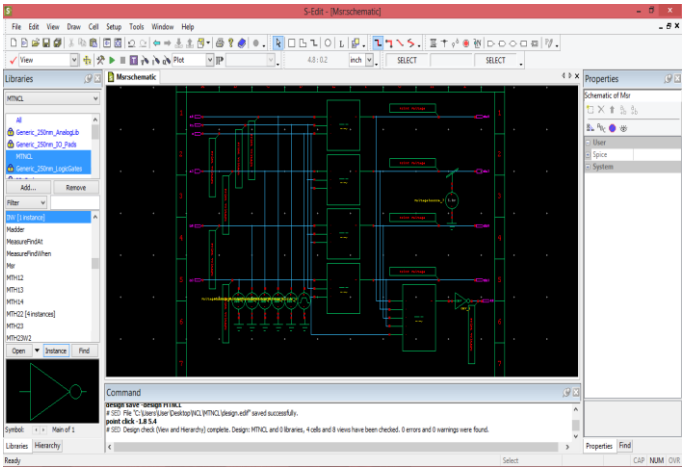

Figure 12: Gate level implementation of Shift Register

This paper proposes the design and analysis of shift registers using EMTNCL paradigm, shown in fig 12 and the simulation result of 2-bit shift registers is shown in fig. 13.

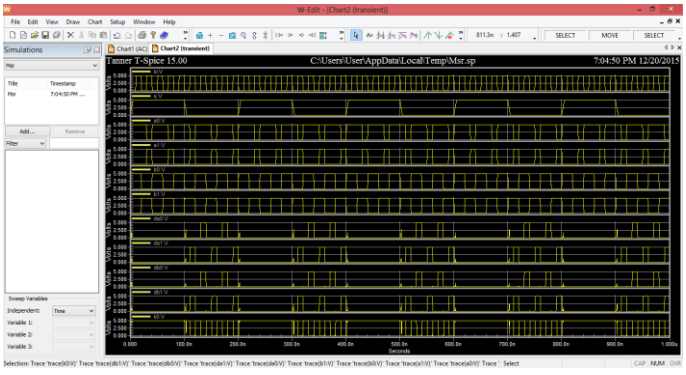

Figure 13: Output Waveforms for Shift Register

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ISSN: 2278-0181
Vol. 5 Issue 01, January-2016

C. *Average Power*

Power is the key characteristic of any experimental design output. Table 17 shows the average power for CMOS, NCL, MTNCL and EMTNCL paradigms. The tabulate results show that the paradigms based on transistor sized EMTNCL principle in terms of power confers higher performance when compared to conventional approaches. So, the proposed Enhanced Multi-Threshold NULL convention logic is an attractive solution for low power and ultra low power requirements.

Table II: Average Power (µW)

THRESHOLD GATE	CMOS	NCL	MTNCL	PROPOSED EMTNCL
TH12	50.00	70.50	82.90	29.50
TH13	19.90	28.70	860.0	20.40
TH14	9.20	14.40	47.90	17.40
TH22	57.10	68.20	82.70	33.60
TH23	35.80	31.40	69.50	36.30
TH23W2	34.20	30.60	64.80	23.30
TH24	36.70	20.10	58.40	21.10
TH24COMP	33.40	15.70	55.40	20.40
TH24W2	25.50	16.70	52.50	19.10
TH24W22	20.90	16.10	46.60	17.10
TH33	28.00	30.30	61.90	23.00
TH33W2	31.70	35.80	64.30	24.30
TH34	42.50	17.00	60.00	22.40
TH34W2	26.10	20.00	52.90	19.50
TH34W3	17.30	16.60	47.40	17.20
TH34W22	28.20	20.50	53.10	19.60
TH34W32	17.40	16.30	46.80	17.10
TH44	16.10	19.30	34.00	12.90
TH44W2	12.70	22.10	82.90	28.80
TH44W3	15.30	17.70	45.20	17.60
TH44W22	269.0	15.90	117.0	40.00
TH44W322	23.80	16.80	51.00	21.90
TH54W22	19.40	22.80	50.10	10.60
TH54W32	18.20	19.20	48.30	18.80
TH54W322	26.50	18.60	52.30	168.0
THAND0	28.70	13.70	45.10	16.80
THXOR0	35.70	15.60	59.10	14.40
FULL ADDER	10.90	58.10	175.0	79.90
SHIFT REGISTER	17.30	11.10	264.0	10.90

D. *Propagation Delay*

The delays of the proposed EMTNCL paradigms are tabulated in table 18 and compared with conventional designs. Compared to MTNCL the proposed design offers improved delay and achieves higher speed of operation but the downside is the it offers more delay overhead than traditional CMOS, NCL, and MTNCL designs.

Table III: Propagation Delay (ns)

THRESHOLD GATE	CMOS	NCL	MTNCL	PROPOSED EMTNCL
TH12	20.60	30.45	100.65	100.68
TH13	40.64	40.79	0.61	120.74
TH14	80.80	80.91	80.79	80.82
TH22	19.95	30.70	100.32	99.95
TH23	19.95	40.82	79.95	80.50
TH23W2	40.44	40.80	120.52	120.56
TH24	0.45	80.93	80.74	80.72
TH24COMP	0.45	80.92	40.66	40.68
TH24W2	0.45	80.93	80.73	80.75
TH24W22	80.68	80.93	80.76	80.73
TH33	40.15	40.45	119.95	119.95
TH33W2	39.95	40.83	120.40	119.96
TH34	0.47	80.91	40.58	40.66
TH34W2	0.45	80.92	80.59	80.48
TH34W3	80.61	80.92	80.50	80.53
TH34W22	0.76	80.90	80.65	80.56
TH34W32	80.49	80.93	80.58	80.65
TH44	80.13	80.88	80.22	79.95
TH44W2	40.52	80.91	40.66	40.76
TH44W3	80.41	80.89	80.46	80.48
TH44W22	0.66	80.91	80.53	80.58
TH44W322	0.76	80.92	80.61	26.06
TH54W22	80.23	80.88	80.30	79.95
TH54W32	79.95	80.90	80.40	79.95
TH54W322	0.43	80.91	80.44	0.61
THAND0	0.64	80.92	80.53	80.59
THXOR0	0.23	80.92	80.43	80.43
FULL ADDER	9.95	40.86	70.74	70.81
SHIFT REGISTER	20.21	20.75	62.75	62.67

V. CONCLUSION AND FUTURE SCOPE

To combat the downsides in conventional MTCMOS self-timed architectures, we incorporate MTCMOS into DI topologies such as NCL for ultra-low power operations known as Multi-Threshold NULL Convention Logic (MTNCL). Transistor sizing is done to the sensitised paths for significant power savings. Potential benefits of the proposed EMTNCL technique includes generation of sleep signal to reduce leakage power, reduces additional logic circuitry with no DATA is lost, more robust and less susceptible to process parameter variations. Upon comparison, it was found that the proposed EMTNCL technique vastly outperforms traditional MTNCL, NCL in all aspects and significantly outperforms MTCMOS architecture in terms of area, power and speed, although they can operate faster. Due to its delay insensitive nature, EMTNCL results in more supple switching requirements, which allows for deep V_{DD} (supply voltage) scaling for further power reduction.

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Vol. 5 Issue 01, January-2016

Whilst this work presents root to existing tribulations and has opened the door for novel research ventures. For future work, we will further scrutinize the circuit performance to achieve high performance, ultra low-power design and to reduce delay-overheads compared to conventional designs.

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