A Study and Comparison of Cascaded Multilevel Inverters using GATES for Switching

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Abstract— With the advent of high power drives in industries, high voltage motors are to be driven with the help of inverter. For this multilevel inverters are used instead of conventional inverters. This paper presents a study and comparison of seven level and seventeen level cascaded H-bridge multilevel inverter. For analysis and verification, MATLAB/SIMULINK models are modeled. Simulink models are simulated and analyzed to derive conclusions. The total harmonic distortion (THD) is used to compare the results.

Index Terms— *Multilevel inverters, Cascaded, H-bridge, Simulink model, and Total Harmonic Distortion.*

I. INTRODUCTION

Wide ranges of high power drives are used in industries, which require continuous power supply. At the time of power failure they are operated with D.C supply. For this purpose we need DC to AC converters. Conventional inverters have a lot of drawbacks like high switching losses, increased stress on switches, high harmonic content etc. For solving this problem H-bridge inverters are used. They are connected in series to get stepped and better output [1]. Hence the study and betterment of multilevel inverters is necessary.

In this work, the cascaded multilevel inverters are studied and compared based on harmonic contents. For this, five level, seven level and seventeen level inverters are modeled in Simulink to get the clear picture of improvement in output voltage waveform with increase in number of levels. Fourier analysis is done to get the percentage of total harmonic distortion present in the output.

II. STUDY OF CASCADED MULTILEVEL INVERTER

The multilevel cascaded inverter is the best alternative over conventional inverters. It is very suitable for medium voltage motor drives and utility applications [3]. Fig 1 shows a generalized model of single-phase cascaded H-bridge multilevel inverter.
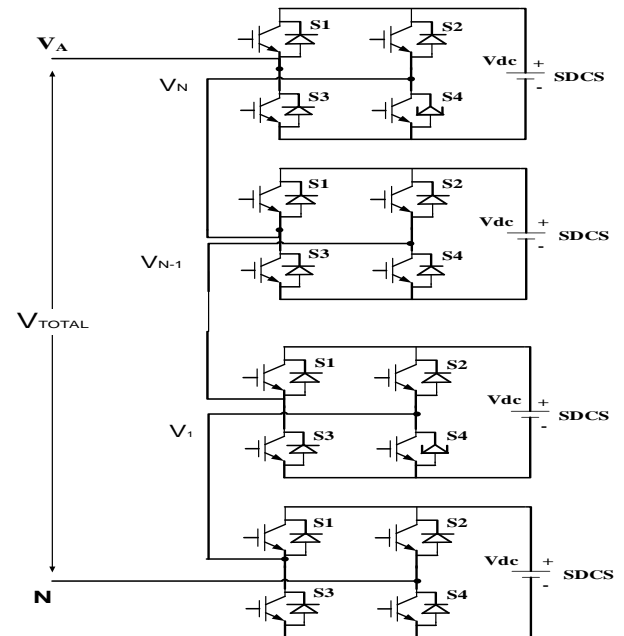

Fig.1. Single phase cascaded H-bridge multilevel inverter.

There are n bridges in fig1. Each bridge has four switches and an individual D.C source. The bridges are cascaded to get different voltage levels. In this paper we will study five, seven and seventeen level cascaded H-bridge inverter. The switches in each leg of each bridge are complimentary in nature such that short circuit doesn't take place.

The models proposed in this paper are single-phase multilevel inverters. They give stepped output as per the switching frequency and switching design of the gates [4]. The switches are strategically switched to get an output that resembles a sine wave. More the number of steps more close the output is to sine wave, lower the harmonic content, better is it for the machines.

III. MATLAB SIMULATION

A. The Network and Working Model of 5/7 Level Inverter

Working of cascaded H-bridge inverter along with its figure and explanation is already being discussed. In this paper, now we will see a model in which two H-bridges are used and a five level and seven level output is obtained. Fig 2 below shows the desired model.
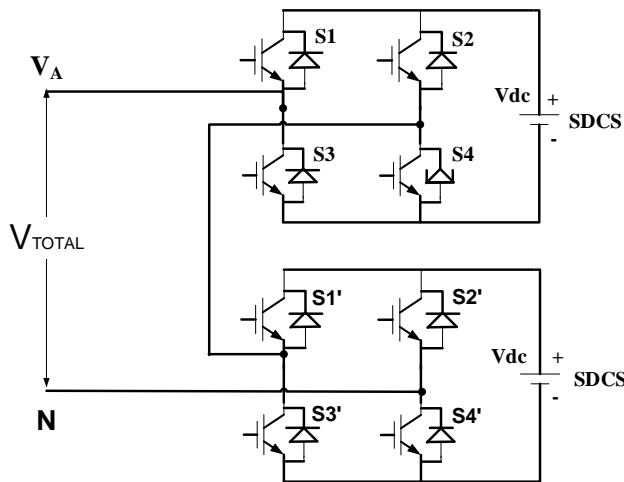
Fig2: Five level inverter and seven level inverter model with two H-bridges cascaded.

For the five level output from the model we keep both voltage sources equal. In this case both the D.C. Sources are kept at 24V. And for getting seven level output one of the D.C. sources is kept as double of the other to get one extra level of output. In this case the output so achieved has seven levels.

The MATLAB model for the above network is shown in the next fig 3. The switching pulses are obtained by giving signal to the discrete monostable flip-flop, which gives a pulse of a desired duration. These pulses are then passed through XOR gates where they are processed to get the final gate signals. These gate signals are given to sub-system 2. Now for the subsystem 1 pulse generator signals are sent to AND gate which processes the signal and gives the desired outputs. These outputs are used as gate signals for subsystem 1.
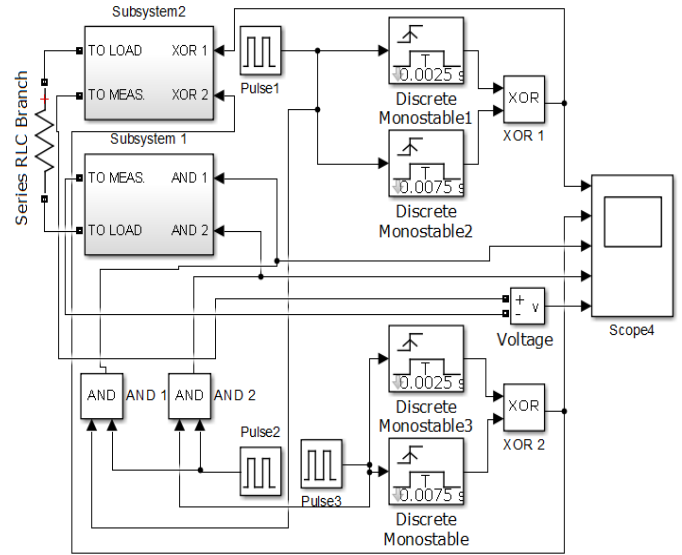
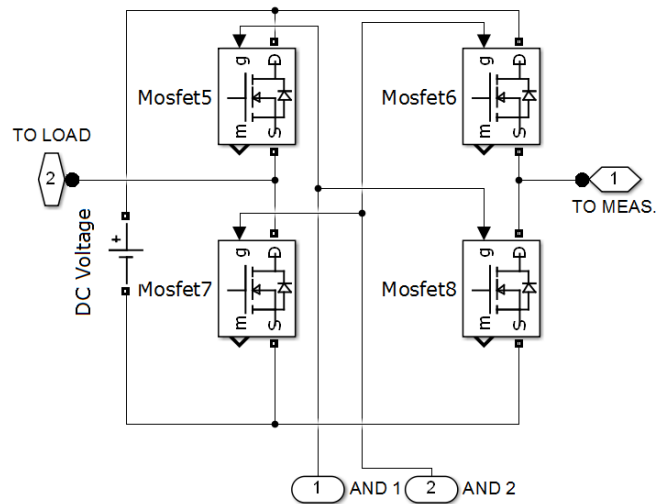Fig 3: Matlab model simulated for the above system using gates for switching

Fig 4: Sub-system 1 for the above SIMULINK model

The above fig 4 shows sub system 1. It can be seen that two gating signals are received from the AND gates. Two connections leave the subsystem, one is connected to the load and other is connected to voltage measurement unit; which is further connected to the scope for final output view.
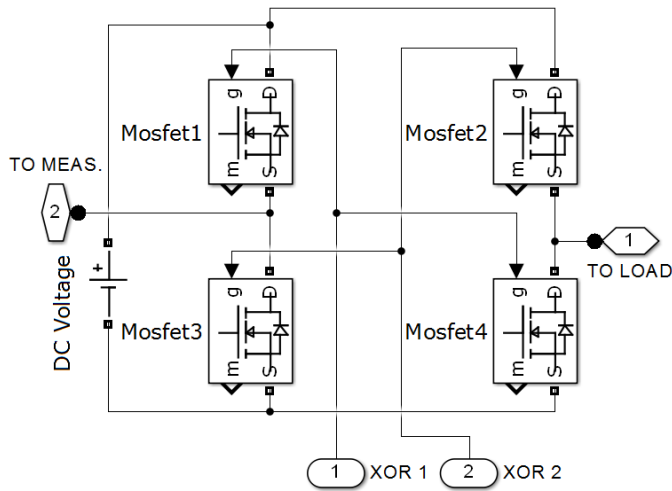
Fig 5: Sub-system 2 for the above SIMULINK model

The above figure 5 shows us subsystem 2 model. The gating signals are obtained from the XOR logical operators. Two connections are leaving the subsystem one is connected to load and other is connected to the voltage measurement unit to give final waveform in the scope.

B. Waveform for Switching and Final Waveform

FOR FIVE LEVEL OUTPUT:

The same network can be used to get both five and seven level output. The switching is done strategically to get the output as desired. The switching sequence and the co-related switches are tabulated and the output voltage than obtained is also shown in the table 1. This is followed by the graph showing the exact switching and final waveform
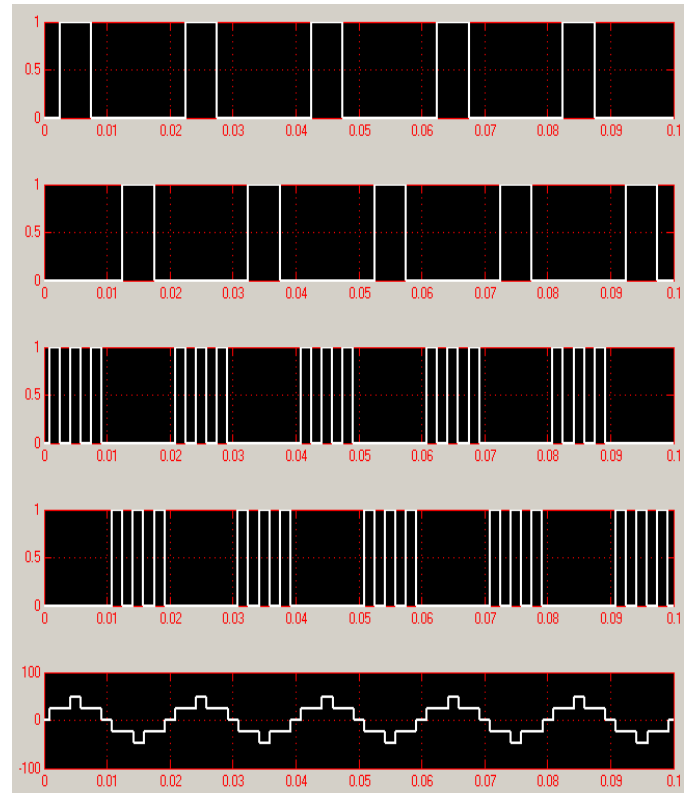

Fig 6: Switching and final waveform for five level inverter

FOR SEVEN LEVEL OUTPUT

The same network is now used to get seven level output. The switching sequence for the seven level output along with tabulated data for the switching and output waveform is given below. This followed by the output of the cascaded multilevel inverter.

Sr. No.	Operating switches	Operating GATES	Output Voltage
1	None	None	0 V
2	(S_5,S_8)	AND_1	24 V
3	(S_1,S_4)	XOR_1	24 V
4	$(S_1,S_4), (S_5,S_8)$	XOR_1 ,AND_1	48 V
5	(S_6,S_7)	AND_2	-24 V
6	(S_2,S_3)	XOR_2	-24 V
7	(S_6,S_7) ,(S_2,S_3)	XOR_2 ,AND_2	-48 V

Table 1. Switching sequence for the five level output

Sr. No.	Operating switches	Operating GATES	Output Voltage
1	None	None	0 V
2	(S_5,S_8)	AND_1	24 V
3	(S_1,S_4)	XOR_1	48 V
4	$(S_1,S_4), (S_5,S_8)$	XOR_1 ,AND_1	72 V
5	(S_6,S_7)	AND_2	-24 V
6	(S_2,S_3)	XOR_2	-48 V
7	(S_6,S_7) ,(S_2,S_3)	XOR_2 ,AND_2	-72 V

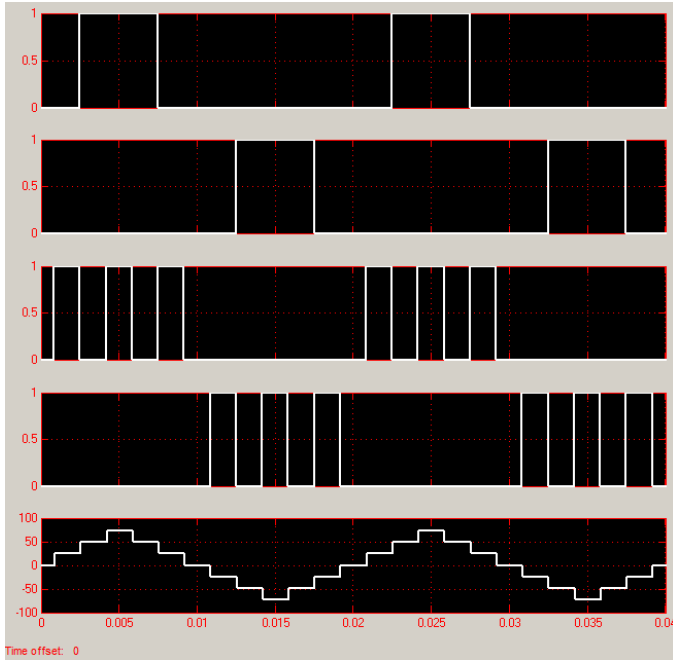Table 2. Switching sequence for the seven level output

Fig 7: Switching and final waveform for seven level inverter

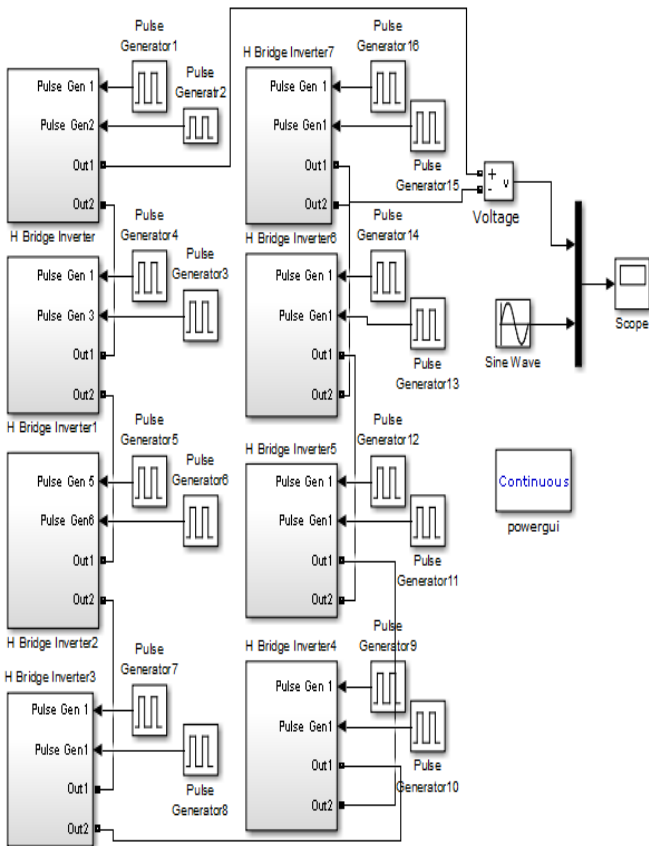## C. Seventeen Level Inverter Model

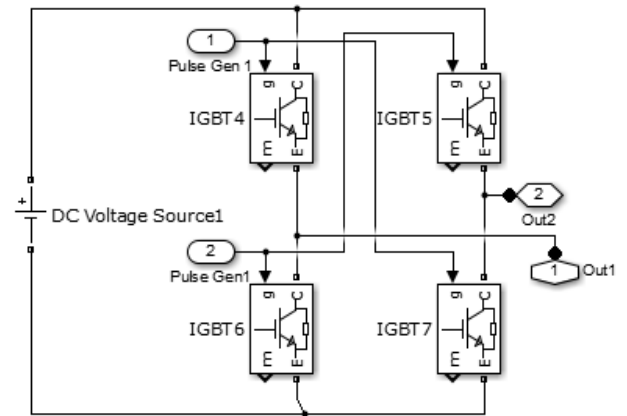Fig 8: Seventeen level cascaded multilevel inverter

Fig 9: Subsystem for the seventeen level cascaded multilevel inverter

The seventeen level inverter model has been prepared for analysis. It has total 8 H-bridge cascaded back to back, as shown in the MATLAB model. Each subsystem has 4 switches; here we have used IGBT for switching. The D.C Source voltage for each bridge is taken to be 1V, for testing purpose. IGBTs in each leg are complimentary to each other to avoid short circuit.

When the above model is simulated in SIMULINK and compared to a sinusoidal wave of magnitude of 8V (peak) we get the final output in the form as shown below.
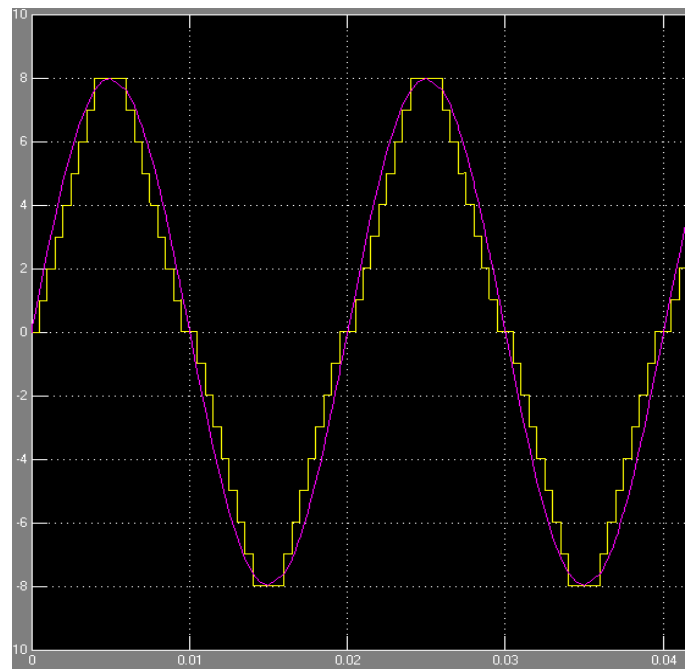
D. Final Output Waveform

Fig 10: Output waveform

IV. FOURIER ANALYSIS FOR THE OUTPUT WAVEFORM

The line to line RMS voltage can be found by the equation.

$$V_L = \left[\frac{2}{2\pi} \int_0^{\frac{2\pi}{3}} V_S^2 \, d(wt) \right]^{\frac{1}{2}}$$

$$= \sqrt{\frac{2}{3}} V_S = 0.8165 V_S$$

The RMS of nth component line voltage is

$$V_{Ln} = \frac{4V_S}{\sqrt{2}n\pi} sin \frac{n\pi}{3}$$

For n=1, represents the fundamental rms line voltage

$$V_{L1} = \frac{4V_S}{\sqrt{2}\pi} sin \frac{180}{3}$$

$$= 0.7797 \, V_S$$

The rms value of the line to neutral voltage i.e. phase voltage can be found from the line voltage component

$$V_P = \sqrt{\frac{1}{3}} V_L$$

$$= \sqrt{2}V_S/3$$
$$= 0.4714 \, V_S$$

The output THD component can be found from the equation

$$THD = \frac{\sqrt{(V_L^2 - V_{L1}^2)}}{V_{L1}}$$

$$\%THD = \frac{\sqrt{(V_L^2 - V_{L1}^2)}}{V_{L1}} \times 100$$

Using the FFT analysis function in MATLAB/SIMULINK can directly do this analysis. This gives us the evaluation of the total harmonic distortion in graphical form.

V. SIMULATION RESULTS

The simulation is performed on the multilevel inverter models. And FFT analysis is done on five level, seven level and seventeen level inverter models. The results indicating the percentage of total harmonic distortion along with the number of harmonics present in the output are shown below. Each harmonic is indicated in the graph below. This is shown as a percentage of the total output voltage. As we increase the level of inverter the percentage of the fundamental frequency component increases and the harmonic content decreases which is eminent in the graph.
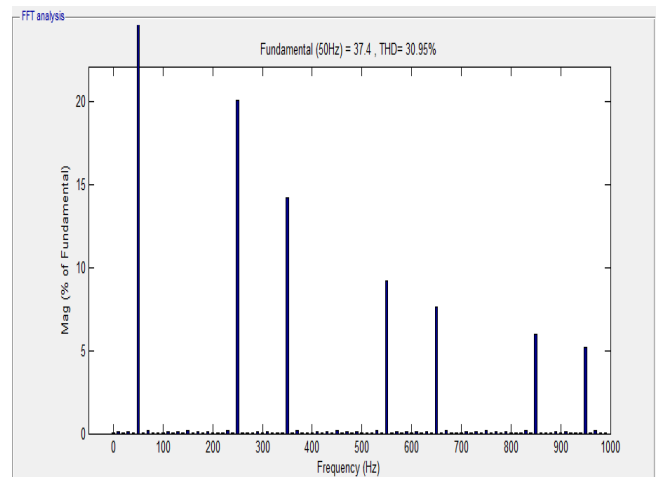

Fig 11: The FFT analysis for output waveform of five level cascaded inverter.
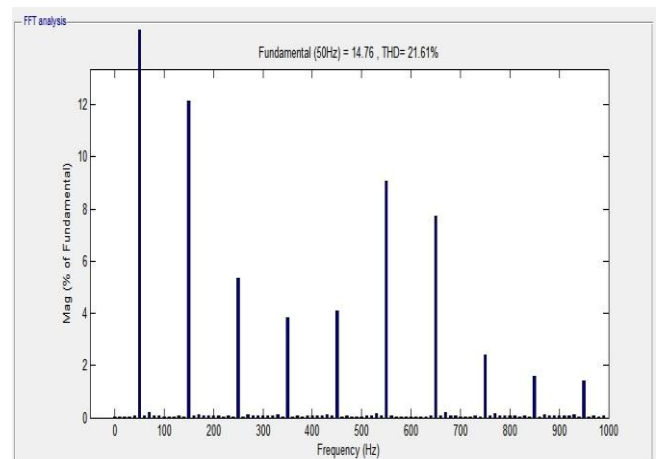

Fig 12: The FFT analysis for output waveform of seven level cascaded inverter
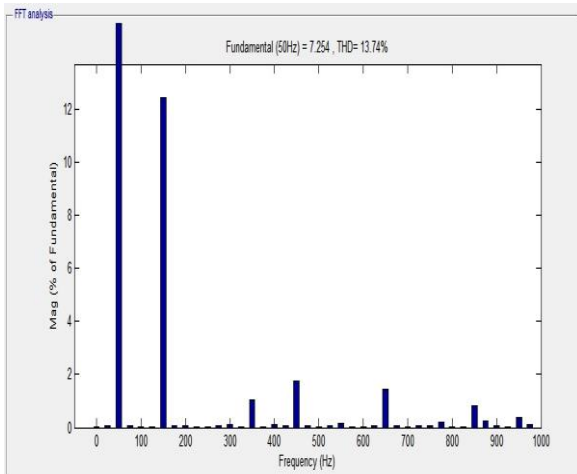
Fig 13: The FFT analysis for output waveform of seventeen level inverter

It is found that the THD for five level inverter is 30.95%, the THD for seven level inverter is 21.61%, and the THD for five level inverter is 13.74%. thus we can see there is a gradual reduction in THD as we increase the levels of the cascaded inverter.

VI. CONCLUSION

As we increase the level of inverter we see that the THD is significantly reduced, this is good as it reduces the ripples in the output. So as we go on increasing the level of inverter towards infinity we get a better sinusoidal wave, but as we increase the level cost of inverter also increases. So it is necessary to insure that we get a better and smother waveform for lower level inverters also.

Cascaded multilevel inverters are thus found to be very suitable for the medium voltage drive operation. Higher level inverters provide better performance as compared to lower level inverters.

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