

A Three Legged DC/DC Converter with Wide and Variable Output Voltage Capability

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Abstract— A new three legged DC/DC converter with reduced circulating current, small output filter, and low conduction loss of the rectifier diode for high DC current and a wide DC voltage application is proposed in this paper. It solves drawbacks like large circulating current, large output filter, narrow zero voltage switching range and large duty cycle loss. Two phase shift full bridge (PSFB) are placed on the primary side which works in a phase shifted manner, thus regulating output voltage. A capacitor called a boost capacitor is placed to reduce the circulating current. Two full bridge rectifiers sharing two low current rating diodes are placed at the rectifying stage. This proposed converter configuration helps eliminate all the problems of a traditional PSFB converter thus making it suitable for high power applications.

Keywords—Phase shift full bridge (PSFB), Zero voltage switching (ZVS), circulating current.

I. INTRODUCTION

Zero voltage switching (ZVS) and Zero current switching (ZCS) are the soft switching technique that are used for PWM full bridge converter. The traditional Phase shift full bridge (PSFB) converter discussed in [1] requires no additional active device and utilizes leakage inductance of the power transformer to achieve ZVS. The gating signals are such that, instead of turning on the diagonally opposite switches in the bridge simultaneously, a phase shift is introduced between the switches in the left leg and those in the right leg. The zero voltage turn on is achieved by using the energy stored in the leakage inductance of the transformer to discharge the output capacitance before turning them on. A conventional phase-shift full-bridge (PSFB) converter is an attractive topology for the high-power and wide-output-voltage applications, since it has some desirable features such as low current/voltage stress, the ZVS operation of all primary switches, and variable output regulation capability by the phase-shifted control signal. A full bridge PWM converter permits all switching devices to operate under Zero Voltage Switching (ZVS) by using circuit parasitic to achieve resonant switching. To achieve ZVS, the two legs of the bridge are operated with a phase shift. This operation allows a resonant discharge of the output capacitance of the MOSFETs and subsequently forces the conduction of each MOSFET's antiparallel diode prior to the conduction of the MOSFET [2].

The proposed switching control technique [3] controls the full-bridge converter by pulse width modulated (PWM) switching technique under light-load condition and burst

PWM switching method under standby condition. However, such a converter has several serious problems. The ZVS range of lagging-leg switches is very narrow under load variation. A new PSFB converter with maximum duty operation is proposed in [4]. The proposed converter eliminates freewheeling period by simply replacing the clamp diodes in the conventional converter with MOSFET switches and dividing primary turns into N_{P1} and N_{P2} . A full-bridge dc/dc converter using a series boost capacitor (SBC) controlled by pulse-frequency modulation (PFM) is proposed in [5]. The proposed converter has a similar circuit configuration to the conventional series resonant converter (SRC). However, it uses a resonance between the magnetizing inductance L_m and the resonant capacitor C_r , whereas the SRC employs a resonance between the leakage inductance L_k and the resonant capacitor C_r . In high-output-voltage applications, a very large output inductor is required to reduce the large ripple current, which results in low power density and high cost [5].

In converter present in [6], it has advantages of the incorporating a saturable resonant inductor. The size of the saturable inductor is very small since magnetic material with very high permeability can be employed. However using a saturable reactor on the primary side to increase the ZVS range increase the amount of heat generated in the reactor thus making it bulky [7]. In converter presented in [8] and [9] it uses an auxiliary transformer winding to the ZVS PWM full-bridge converter to be in series with the resonant inductance. The introduced winding not only makes the clamping diode current decay rapidly and reduces the primary side conduction losses, but also can make the current ripple of the output filter be smaller; hence the output filter capacitor can be reduced. Even though with all the said modifications it still has the drawback of a large output inductor when used for high output voltage applications and the current stress on all the switches is higher than the traditional PSFB converter due to the assistance of current source for a wide ZVS range which may even lead to increased conduction losses [10] - [14]. In paper presented in [15], [16] an improved current-doubler rectifier with coupled inductors is proposed. In comparison with the conventional current-doubler rectifier (CCDR) the component counts of the proposed rectifier are identical, while the proposed rectifier can adjust the turns ratio of the coupled inductor to extend the duty ratio range,

which can reduce the peak current through the isolation transformer and switches and can lower output current ripple. A ZVS and soft-commutating two transformer full-bridge PWM converter using the voltage ripple is proposed as shown in [17]. In the proposed converter, the ZVS operation of lagging leg is achieved along the whole load range using the energy stored in the magnetizing inductor of transformers. In PSFB converter with series-connected two transformers however due to the use of two transformers, the ZVS operation in the converters is achieved under entire load conditions. However, for ZCS operation and counter measures to side effects such as high secondary-voltage stress and primary-current overshoot, they require many additional components, which results in high cost and a complex structure [18], [19].

The active clamp method [20]-[23] can solve the efficiency degradation problem and the voltage overshoot can be clamped, but it increases system complexity and degrades system reliability. A novel Energy Recovery Clamp Circuit (ERCC) employs a simple auxiliary circuit in which neither lossy components nor active switches are used. Therefore, the efficiency and reliability of the dc-dc converter can be improved with this ERCC. But using IGBTs to suit ZCS operation precludes the use of high switching frequency to realize smaller magnetic components and capacitors. Also, its large output inductor in high-voltage applications is an additional drawback.

PSFB converters with the ZVS capability in a wide load range and reduced output filter was presented in [24]. It is well suited for applications in the range of a few hundred watts to a few kilowatts. It is essentially a hybrid combination of an uncontrolled half-bridge section and a phase-shift controlled full-bridge section, realized with just four switches. The main features of the proposed topology are zero-voltage-switching down to no-load without serious conduction loss penalty, constant frequency operation and near-ideal filter waveforms. The improved filter waveforms result in significant savings in the input and output filter requirement, resulting in high power-density. The new topology requires two transformers and two dc-bypass capacitors. The combined VA rating of the two transformers is more than that of the single transformer of conventional full-bridge converters, for variable-input applications. But the primary circulating current is still in the controlled full-bridge inverter. The PSFB converter designed for server power system can always operate with a maximum duty cycle under all line conditions. This operation minimizes the circulating current and reduces the filter requirement. Yet, two additional main switches in the primary side increase the cost and circuit complexity.

If the converter presented in [25] is to be modified than we can achieve its implementations on various applications. The existing circuit topology has few drawbacks when used for applications that require output voltage variation like primary conduction losses, large circulating current exists on the primary side during the freewheeling period. Beside, the size of the output filter is highly increased due to small

duty operation and it results in low power density and high cost.

II. DESCRIPTION OF THE PROPOSED CIRCUIT

The circuit diagram of the proposed converter. As shown in Fig. 1, the proposed converter is composed of two Phase Shift Full Bridge converters PSFB₁ and PSFB₂ that are placed in parallel on the primary side. One of PSFB converters PSFB₁ consists of switches S₁, S₂, S₃, S₄ and a transformer T₁. The other converter PSFB₂ consists of switches S₂, S₄, S₅, S₆, a small capacitor, C_B and a transformer T₂. Both PSFB converters share switches S₂ and S₄. In order to eliminate the circulating current of T₂, C_B is connected in series with T₂ as shown in Fig. 1.4. Due to the voltage across this capacitor, which is called the boost capacitor, the circulating current of T₂ is reset during the freewheeling period. In the secondary side, both main transformers T₁ and T₂ are connected in series and a full-bridge rectifier consisting of D₁, D₂, D₃, D₄ and low voltage diodes D_{L1} and D_{L2}.

OPERATING PRINCIPLE

In order to illustrate the operation of the proposed converter, several assumptions are made:

- 1) All switches are ideal except for output capacitor, C_{oss} and the internal antiparallel diode of it.
- 2) The output inductor L_O is large enough to be considered as a constant current source during a switching period.
- 3) The blocking capacitor C_B is large enough to be considered as a constant voltage source of V_{IN}/2.
- 4) The output capacitor C_O is large enough to be considered as a constant voltage source of V_O.
- 5) The magnetizing inductance L_{m2} of the transformer T₂ is large enough to ignore the effect of the magnetizing current during a switching period.
- 6) The main switches are all MOSFETs with parasitic diodes of D_{b1}, D_{b2}, D_{b3} and D_{b4}.
- 7) The output capacitances of all MOSFETs have the same capacitance of C_{oss}
- 8) The transformers of T₁ and T₂ have the same turns ratio of $n = N_{S1}/N_{P1} = N_{S2}/N_{P2}$

The switching period is in 2 half cycles i.e., (t₀-t₈) and (t₈-t₁₆). Due to the symmetrical operation of the converter only one half cycle is discussed.

Mode 1 (t₀ to t₁):- Switches S₁, S₂ and S₅ are ON in this mode and the remaining switches are OFF. During this mode, positive input voltage V_s is applied to the primary voltage v_{pri1}(t) of T₁ i.e., V_s = v_{pri1}(t) and - (V_s - v_{Cb}(t)) is applied to the primary voltage v_{pri2}(t) of T₂. v_{pri2}(t) = - (V_s - v_{Cb}(t)). Since i_{pri2}(t) charges the boost capacitor C_B, the voltage v_{cb}(t) of C_B is linearly increased in this mode. The energy stored in transformers T₁ and T₂ is transferred to the output through D₁ and D₂. The output voltage of rectifier stage v_{rec}(t) is the sum of reflected voltage v_{sec1}(t) of T₁ and reflected voltage v_{sec2}(t) of T₂.

$$V_{rec} = n (V_s - 0.5 V_{CB})$$

Mode 2 (t_1 to t_2):- At time t_1 , S_5 is turned OFF. The output capacitors C_{oss} of switches S_5 and S_6 are linearly charged and discharged, respectively, by the energy stored in the output inductor L_o . $v_{pri2}(t)$ is linearly decreased to zero and the primary $v_{pri1}(t)$ is continuously maintained at V_s .

$$v_{pri2}(t) = 0$$

$v_{pri1}(t) = V_s$. Hence, $v_{sec2}(t)$ is decreased to zero voltage.

Mode 3 (t_2 to t_3):-Switch S_6 is turned ON. $v_{pri1}(t)$ is still maintained at V_s during this mode. Hence, $v_{rec}(t)$ is maintained at $0.5nV_s$ and $i_{pri1}(t)$ is continuously increased. During mode 3, since the commutation between D_2 and D_6 is progressed, total $v_B(t)$ is applied to L_{lk2} and $i_{pri2}(t)$ starts to decrease rapidly.

$$v_{pri1}(t) = V_s$$

$$v_{rec}(t) = 0.5nV_s$$

$$V_b = (1/C_B) \int I_{pri2}$$

Mode 4 (t_3 to t_4):- When the commutation between D_2 and D_6 is completed, mode 4 begins. Since $i_{pri2}(t)$ is in the zero state, the input power is transferred to the output stage through only T_1, D_1 and D_6 . The voltage of boost capacitor $v_B(t)$ remains its maximum value and the secondary voltage $v_{sec2}(t)$ of T_2 is decreased.

$$V_b = (1/C_B) \int I_{pri2}$$

Mode 5 (t_4 to t_5):-At time t_4 , S_1 and S_2 are turned OFF and mode 6 begins. Since $v_{sec1}(t)$ remains in the positive side. The output current still flows through T_1, D_1 and D_6 during this mode. Hence, C_{oss} of S_1, S_2, S_3 and S_4 are linearly charged and discharged, respectively.

Mode 6 (t_5 to t_6):-When the sum of $v_{sec2}(t)$ and $v_{sec1}(t)$ reaches at zero voltage, mode 6 starts. At time t_5 , D_4 starts to conduct and the commutation between D_1 and D_4 is progressed. The C_{oss} of S_1, S_2, S_3 and S_4 is charged and discharged, respectively.

$$Z_o = \sqrt{\frac{L_{lk1} + L_{lk2}}{4C_{oss}}} \text{ and } w_o = \frac{1}{\sqrt{4(L_{lk1} + L_{lk2})C_{oss}}}$$

$$i_{pr1} = I - Z_o \cos(w_o)$$

$$i_{pr2} = -Z_o \cos(w_o)$$

$$V_{p1} = 2i_{pr1} Z_o \sin(w_o)$$

$$V_{p2} = 2i_{pr1} Z_o \sin(w_o)$$

Mode 7 (t_6 to t_7):- After $v_{pri2}(t)$ and $v_{pri1}(t)$ reach $-V_s$, the antiparallel diode of S_3 and antiparallel diode of S_4 start to conduct. The ZVS operation of S_3 and S_4 is achieved. During this mode, the commutation between D_1 and D_4 is still progressed. The sum of the input voltage V_s and divided voltage of V_B is applied to both leakage

inductor L_{lk1} of T_1 and leakage inductor L_{lk2} of T_2 so that $i_{pri1}(t)$ and $i_{pri2}(t)$ are rapidly decreased to the negative side.

$$i_{pr1} = -\frac{V_{lk1}}{L_{lk1}}$$

$$i_{pr2} = -\frac{V_{lk2}}{L_{lk2}}$$

Mode 8 (t_7 to t_8):-At this time, since the commutation between D_3 and D_6 is progressed, V_s is applied to the L_{lk1} and $i_{pri1}(t)$ is continuously decreased to the negative side. The negative

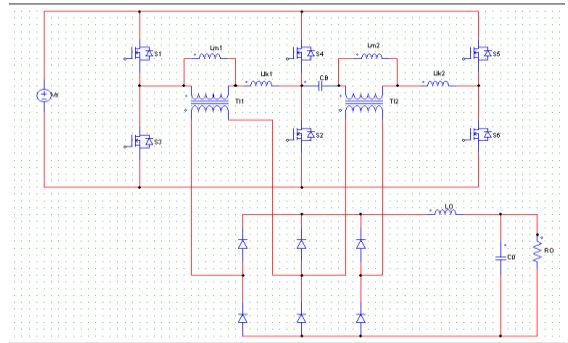


Fig 1:- Circuit diagram of the proposed converter

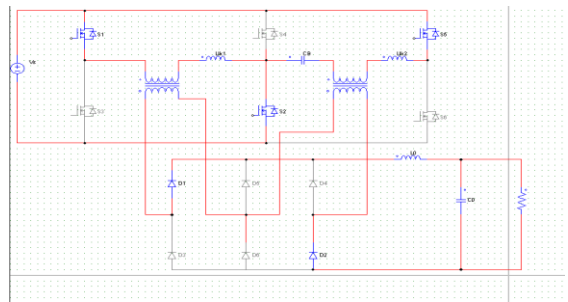


Fig 3:- Mode 1 (t_0 to t_1)

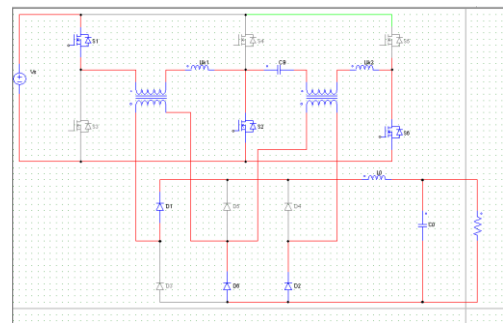


Fig 5:- Mode 3 (t_2 to t_3)

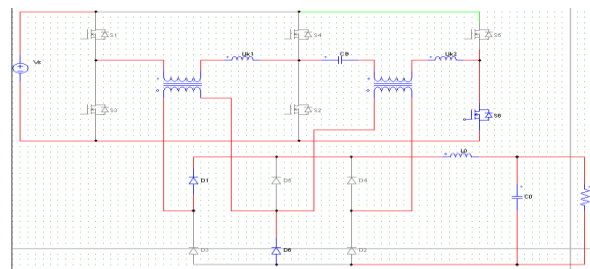


Fig 7:- Mode 5 (t_4 to t_5)

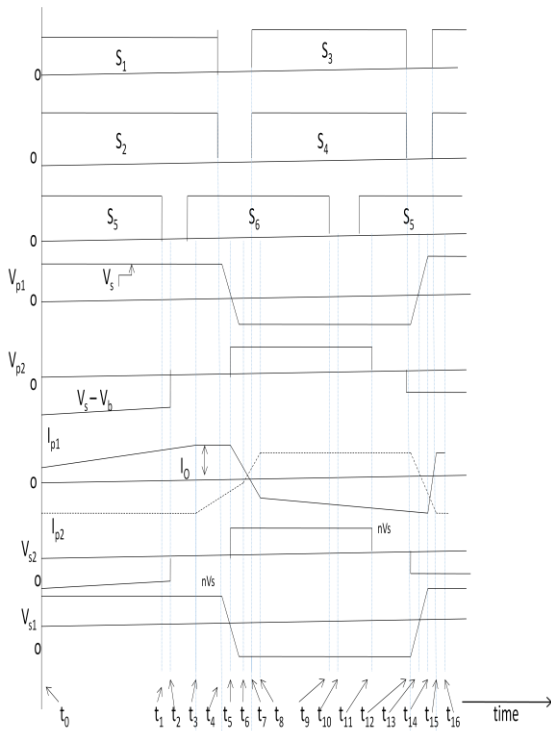


Fig 2: - Key operating waveform during various mode.

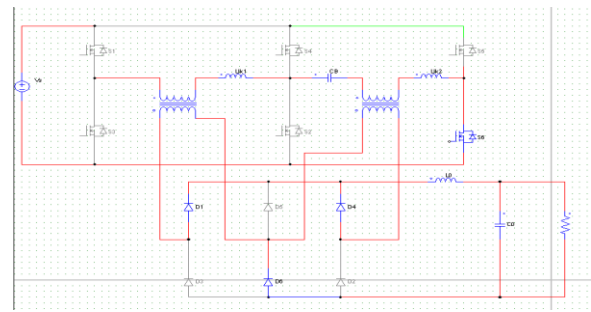


Fig 8:- Mode 6 (t_5 to t_6)

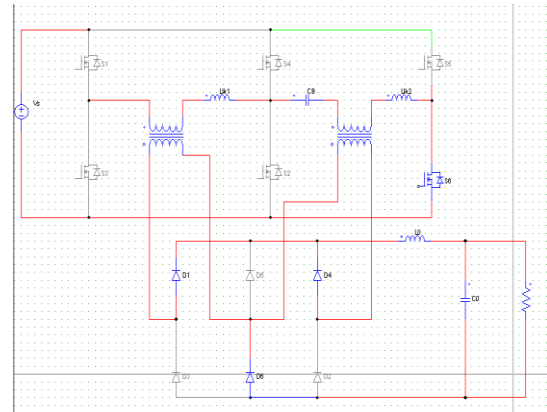


Fig 9:- Mode 7 (t_6 to t_7)

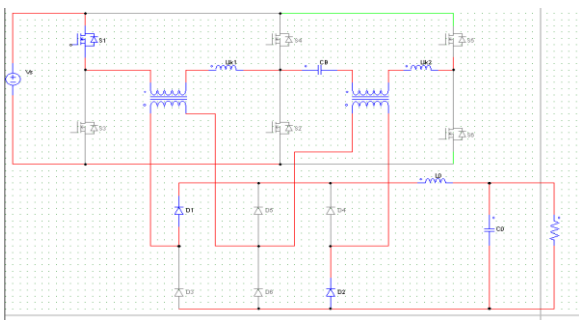


Fig 4:- Mode 2 (t_1 to t_2)

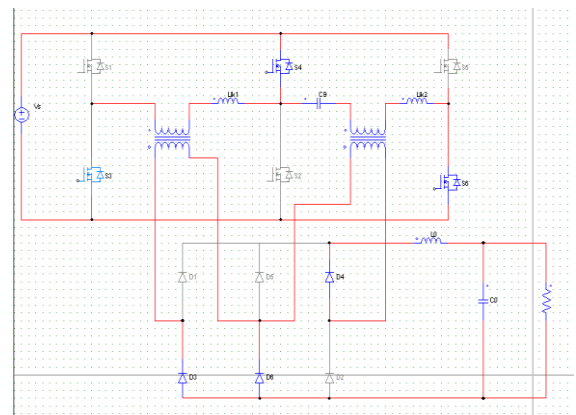


Fig 10:- Mode 8 (t_7 to t_8)

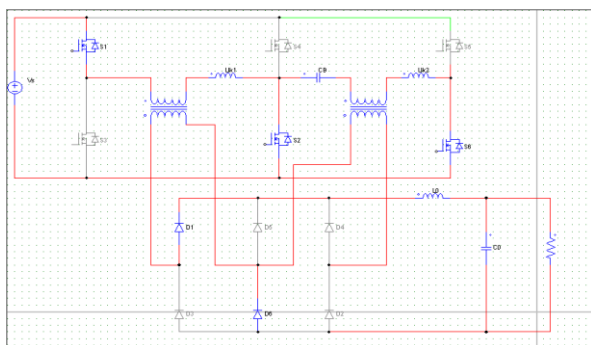


Fig 6:- Mode 4 (t_3 to t_4)

voltage $-V_s + v_B(t)$ is applied to $v_{pr2}(t)$. The input energy is transferred to the output through T_2, S_4, S_6, D_6 and D_4 .

$$i_{pr1} = -\frac{V_s}{Llk1}$$

$$i_{pr2} = -0.5nI_o$$

$$v_{pr1} = -V_s + v_B$$

IV. DESIGN CONSIDERATION

1. Choose D_{max} . D_{max} should be chosen as large values as possible in order to maximize (N_p/N_s) and for the reduction of conduction losses.

2. Choose V_{sec} . The minimum value should be chosen to maximize (N_p/N_s) . When (N_p/N_s) is increased, it reduces the primary current and increasing the leakage inductor value. The initial choice of V_{sec} is somewhat arbitrary and the final value is obtained after several iteration. V_{sec} should satisfy,

$$V_{sec} \geq \frac{V_{out}}{D_{max}}$$

3. Voltage Conversion Ratio:- The voltage conversion ratio of the proposed converter without considering the effect of boost capacitor can be expressed by averaging the rectifier output voltage.

$$M = \frac{V_o}{V_s} = (D + 0.5) n$$

The voltage conversion ratio of the proposed converter at dual full-bridge mode without considering the effect of the boost capacitor is the same as that of the circuit in [24]. However, when considering the effect of the boost capacitor, the turns ratio of transformer T_2 can be slightly changed. The voltage conversion ratio of the proposed converter can be slightly increased and turns ratio of transformer T_2 can be designed as a smaller value [26].

$$C_B \geq \frac{T I_o D n}{4 V_s}$$

4. A full-bridge rectifier is employed on the secondary side. However, due to the oscillation of parasitic circuit elements the rectifier diodes still suffer from high voltage stress. Therefore, a high-voltage-rated diode has to be used for the rectifier stage. In the rectifier stage of the proposed converter, the diodes D_5 and D_6 are placed at the midpoint of both transformers T_1 and T_2 with a full-bridge rectifier.

5. The magnetizing inductor L_{m1} of T_1 is designed as a small value, increased magnetizing current can increase the conduction loss of primary components, the effect of magnetizing current on primary RMS current is negligible at heavy load condition as already discussed in [25] and the leakage inductor is given by.

$$\frac{1}{2} L_{lk2} (n I_o)^2 \geq 1.33 C_{oss} (0.5 V_s)^2$$

6. The voltage across the output inductor is given by $(n V_s - V_o)$ $(V_o/n V_s - 0.5)$ and the change of the converter that is flowing through the inductor is ΔI_{L_o} . The value of the output inductor filter is given by,

$$L_o = \frac{n V_s - V_o}{\Delta I_o} \left(\frac{V_o}{n V_s} - 0.5 \right) \frac{1}{f}$$

V. SIMULATION:-

The figure below shows the circuit arrangement of fig 1 in MATLAB simulation package. The performance of the proposed converter is verified for the input DC voltage of 350 V and the dc output of 205 V is obtained.

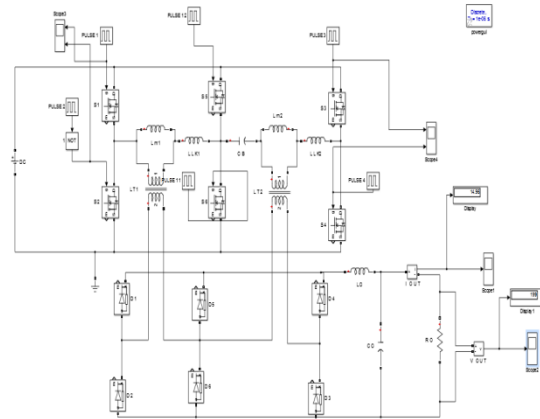


Fig 11: Circuit Arrangement in MATLAB Simulation Package

SPECIFICATION

| PARAMETERS | VALUES |
|-------------------------|-----------------|
| Input DC Voltage | 350V |
| Switching Frequency | 100 KHz |
| Output Power, P_o | 1025W |
| Output Inductor, L_o | 26.5 μ H |
| Output Capacitor, C_o | 300 μ F |
| C_B | 500 nF |
| L_{lk1} | 0.0043 μ H |
| L_{lk2} | 0.00226 μ H |
| L_{M1} | 302 μ H |
| L_{M2} | 407 μ H |

Fig 12:- Component lists
SIMULATION RESULTS

The simulation of the proposed converter was verified using MATLAB-SIMULINK, a simulation software widely used. The simulations shown below represent the various quantities as mentioned below.

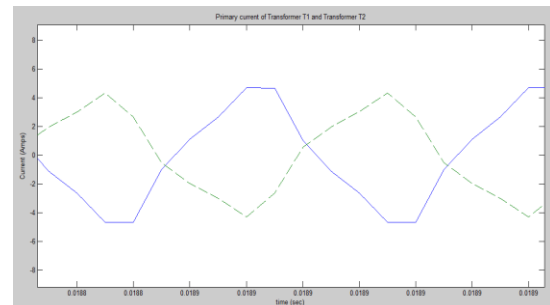


Fig. 13:- Primary current of transformer T_1 and transformer T_2 . Scale: X-axis:- Time (Each division = 0.00001 sec) Y-axis:- Magnitude (Each Block = 2 A)

The primary current of transformer T_1 and transformer T_2 are denoted by solid and dotted lines respectively, as shown above. Mode 1 results in increase of the transformer T_1 primary voltage, likewise the primary current of transformer T_1 increases till mode 5 and then decreases till mode 8 and then the symmetric operations occurs thereafter, while the primary current of transformer T_2 increases in negative side and as the voltage across primary of the transformer T_2 goes to positive side, the current also becomes positive.

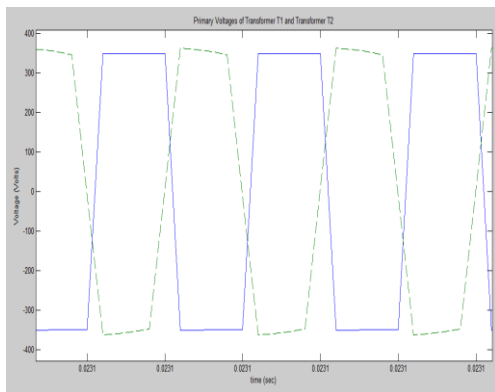


Fig. 14:- Primary transformer voltage of T_1 and T_2

Scale: X-axis:- Time (1 division= 0.00001),

Y-axis:-Magnitude (Each Block= 100 V)

The primary voltage of transformer T_1 and transformer T_2 are denoted by solid and dotted lines respectively, as shown above. The figure above shows the waveform of primary transformer voltage of T_1 and T_2 . As we have already discussed the waveform of primary current to transformer T_2 , so as long as the current in the primary winding of the transformer T_2 is positive, the voltage across it is also positive. Likewise, when the current in the primary winding of the transformer T_2 is negative it is seen the voltage of the transformer also to be negative. Same goes with transformer T_1 .

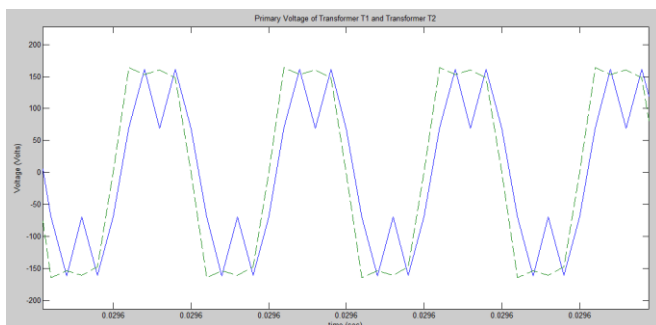


Fig 15:-Waveform of secondary voltages of the transformers

Scale: X-axis:- Time (Each division=0.00001 sec) Y-axis:-Magnitude (Each Block= 50 V)

The waveform shown above is the waveform of secondary voltage of transformer T_1 and transformer T_2 The secondary voltage of transformer T_1 and transformer T_2 are represented by Solid and Dotted lines respectively, as

shown above in the figure. As long as the voltage across the transformer T_1 and transformer T_2 remains positive values the secondary voltage also remains positive and the same happens when the voltage of the transformers goes to its negative value. Maximum value of secondary voltage of transformer T_1 and transformer T_2 is nV_s i.e., 154 Volts.

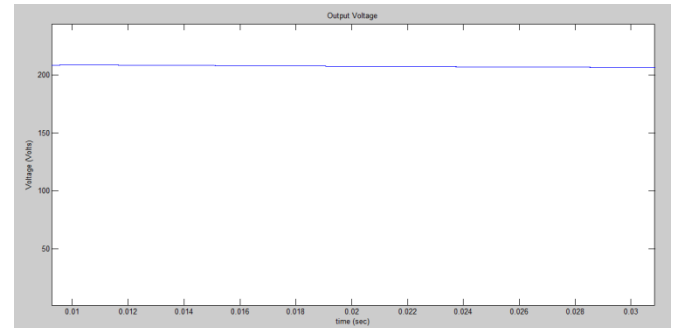


Fig 16:-Waveform of output voltage.

Scale: X-axis:- Time (Each division=0.002 sec) Y-axis:-Magnitude (Each Block= 50 V)

The figure above shows the simulation results of output voltage of the proposed converter for the input DC voltage of 350 V. The output voltage is 205 V. Similarly the output current waveform is shown below with the same value of load. The current obtained is 5 A direct current.

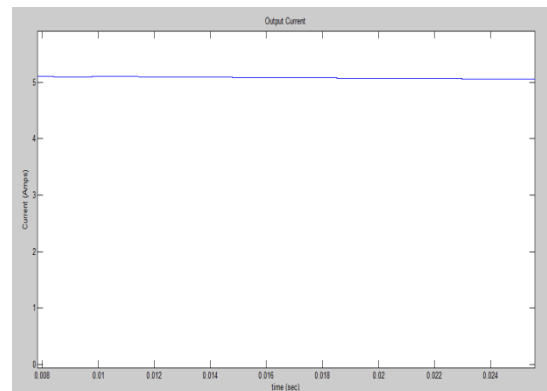


Fig 17:-Waveform of output current.

Scale- X axis:-Time (Each division=0.005 sec) Y-axis:-Magnitude (Each Block= 2 A)

APPLICATIONS

- Used in hybrid vehicle system that use high voltage starter/generator.
- Used in Telephone exchange communication.
- Used in street LED lightening, 48V.
- Used in SMPS power supplies for Desktop, LED TV, LCD displays.
- Used in Industrial control and Process control instrument set up.
- Used in telecom applications – 230V/48V.
- Used in high power applications and various applications that uses high DC current and DC voltage.

CONCLUSION

A new three legged DC/DC converter with reduced circulating current, small output filter, and low conduction loss of the rectifier diode for high DC current and a wide DC voltage application is proposed. Connecting a capacitor in series with one transformer T_2 , it is seen that the circulating current is greatly reduced. The ZVS operation of all switches is well achieved even though the circulating current is reduced. The waveform of the rectifier output voltage is improved with size reduction of the output inductor. Since the load current is distributed to the additional low voltage rated diode, the reduction in the secondary conduction loss in the proposed topology is seen. With all these advantages, it results greatly in improvement of efficiency over wide output voltage. Therefore, the proposed converter has advantages and is suitable for a wide output voltage applications as mentioned earlier.

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