International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 4 Issue 07, July-2015

An AC-AC Power Converter for Mitigation of Voltage Disturbances in Three Phase System based on Characterization of Algorithm

Sk. Ghouse Modin[1]
Asst. Professor, Dept. of EEE
A.I.T.S. Kadapa

M. Bala Siva Prasad[2]
Asst. Professor, Dept. of EEE
A.I.T.S. Kadapa

C. Moulali[3]
PG Student, Dept. of EEE
A.I.T.S. Kadapa

Abstract- **In this paper a versatile ac-ac power converter is proposed based on characterization of algorithm that can be utilized as a control device for Custom Power applications. The converter has the ability to regulate bus voltage through voltage sags. The dynamic voltage restorer is a definitive solution to address the voltage-related Power Quality problems. Conventional topologies operate with a dc link, which makes them bulkier and costlier; it also imposes limits on the compensation capability of the DVR. In the proposed scheme there is no storage device is employed, these topologies require improved information on instantaneous voltages at the point of common coupling and need flexible control schemes depending on these voltages. Therefore, a control scheme for DVR topologies with an ac–ac converter, based on the characterization of algorithms is proposed in this paper to mitigate voltage sags with phase jump. The proposed converter connected in three phase system in interconnected manner. The scheme is tested on an interphase ac–ac converter topology to validate its efficacy. Detailed simulations to support the same have been carried out in MATLAB, and the results are presented.**

Index Terms – AC-AC Converter, Power Quality, Voltage Disturbances, Transposed Connection, DVR.

I.INTRODUTION

Among different types of disturbances occurring in power system, voltage sag is known to produce the most devastating impact on the loads. Studies show that 92% of all disturbances in the electrical power distribution systems are voltage sags, transients, and momentary interruptions [1], [2]. More than 1500 distinct events studied by "i-grid.com" (mostly from large industrial plants located around the U.S. and Canada) were analyzed in detail [3]. the statistical survey of the measured events, and indicates that 63% of the disturbances were single line-to-ground (SLG) faults and 11% were line-to-line (LL) faults [4]. Though symmetrical faults (Symm) were 6%, deep symmetrical three-phase voltage sags were very rare [1]. Most of the three-phase symmetrical faults create symmetrical sag depth less than 50%. Increasing use of loads supplied by electronic power converters in industry has led to growing problems with the reliability of the power supply. Computers, adjustable speed drives, and automated manufacturing processes are very susceptible to voltage sags and brief outages. The need for greater power quality has prompted the end-users to install uninterruptable power systems and or other electronic power conditioning means to maintain the voltages within the susceptibility levels of the critical equipment. Advances in power semiconductor devices are making it possible for utilities to use a variety of power control equipment to raise power quality levels to meet these requirements [10]. A schematic diagram of the DVR incorporated into a distribution network is shown in Fig. 1.Vs is the source voltage, $V_1$is the incoming supply voltage before compensation,V_2 is the load voltage after compensation, $V_{dvr,}$ is the series injected voltage of the DVR, and is the line current. The restorer typically consists of an injection transformer, the secondary winding of which is connected in series with the distribution line, a voltage-sourced PWM Inverter Bridge is connected to the primary of the injection transformer and an energy storage device is connected at the dc-link of the inverter bridge [3].

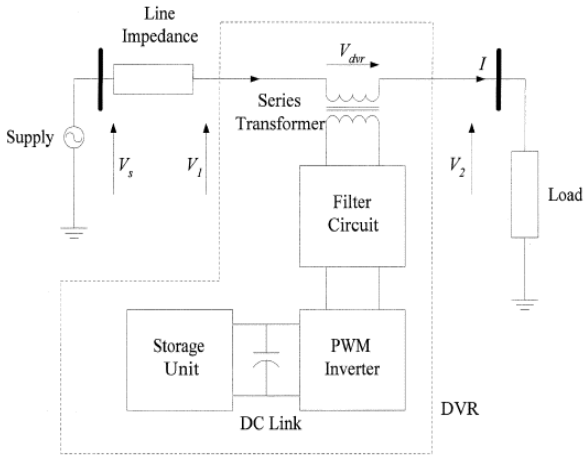


Fig. 1. Typical schematic of a power distribution system compensated by a DVR.

However, the development in the DVR topologies, with direct converters, is not matched with that of the control algorithms. Most of them are controlled either by instantaneous comparison of the voltage at the PCC with a unit reference vector or simple feed forward control to adjust the duty cycle.

Since these topologies eliminate the dc link, the compensation depends directly on the voltage at the PCC, and each type of unbalance in the voltage at PCC imposes a limit on the compensation capability distinctly. Therefore, in this paper, a control scheme based on characterization of voltage sag is proposed for the topologies.

Characterization of voltage sags has not received due attention, though more developments have come with mitigation of voltage sags. The applications of classification and characterization of voltage sag have been limited to assessing the performance of various systems under sag and to present statistics. This paper demonstrates that characterizing can aid in efficient compensation. It helps in knowing the compensation capability of the topologies, since they are dependent on the input voltage waveforms. Insight on this capability helps in a flexible operation between the compensation schemes, that is, presag and inphase compensation.

II. PROPOSED TOPOLOGY

The schematic diagram of the proposed interphase ac–ac voltage sag supporter for correcting voltage sag in phase a *is* shown in Fig. 2. This voltage sag supporter is connected between the point of common coupling (PCC) and the load.

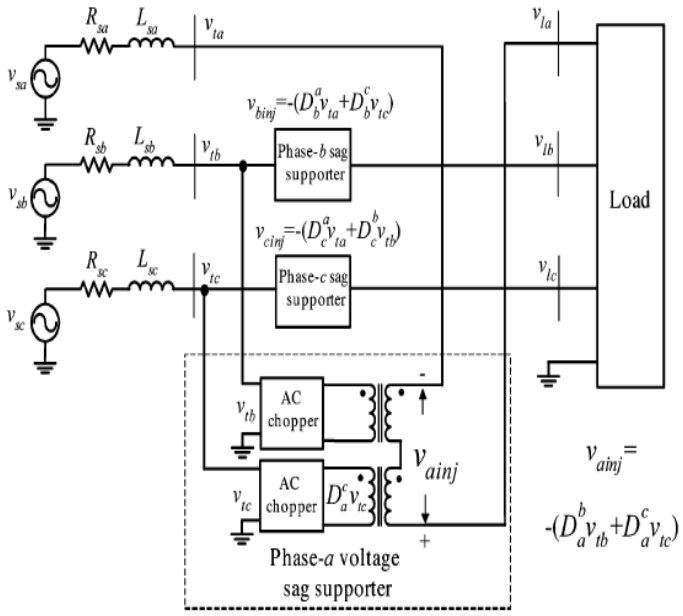


Fig. 2. Schematic diagram of the proposed interphase ac–ac voltage sag supporter.

When the PCC experiences voltage sag, the compensator injects an appropriate voltage in series with the supply voltage to deliver the desired load voltage. This topology consists of two ac choppers and two isolation transformers in each phase. The transformers are connected such that the two chopper output voltages are added and isolated.

The required voltages from phase *b* and phase *c* are obtained by individual ac chopper and connected to primary of the each transformer. The added secondary voltage is then injected in series with the line to compensate the sag in phase *a*. Similarly, for phase *b* and phase *c*, individual sag supporters are provided.

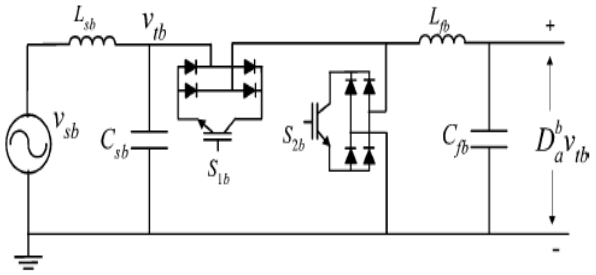


Fig. 3. AC–AC chopper circuit with input and output filters.

III.CHARACTERIZATION OF ALGORITHM

The proposed algorithm combines the merits of instantaneous symmetrical component theory and Fourier transform. The fundamental symmetrical components are calculated by taking Fourier transform of the instantaneous symmetrical components of the supply voltage at PCC. Instantaneous symmetrical components reflect the instantaneous changes in the supply voltage and so it is used to detect the disturbance in power system [9]. Instantaneous positive and negative sequence components are calculated by (1),

$$\begin{bmatrix} \bar{V}_{a0} \\ \bar{V}_{a1} \\ \bar{V}_{a2} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \qquad (1)$$

Where, $a = 1\angle 120o$, v_{a0}, v_{a1} and v_{a2} are the instantaneous symmetrical components, v_a, v_b and v_c are instantaneous supply voltages. The detection time however, varies with the number of phases affected. The sag in three phases is detected instantly. Sag in two and one phase takes atmost quarter and half cycle respectively. Being instantaneous in nature, error associated with the noise in voltage is more and the algorithm gives erroneous results in case of sags with unbalance in both magnitude and phase. The fundamental symmetrical component ($\bar{V}_{ak}$) is calculated from its corresponding instantaneous values ($\bar{V}_{ak}$) as follows:

$$Vak = \frac{\sqrt{2}}{\frac{Ts}{2}} \int_0^{\frac{Ts}{2}} \bar{V}_{ak}(t) e^{-j\left(\omega t - \frac{\pi}{2}\right)} dt \qquad (2)$$

Where K= 0, 1, and 2 represent zero, positive, and negative sequence, respectively; is the fundamental frequency in radians per second and Ts is the system time period in seconds. Here, a half-a-cycle window is used (assuming that the even harmonics are negligible).The algorithmic flow chart as shown in figure 4.

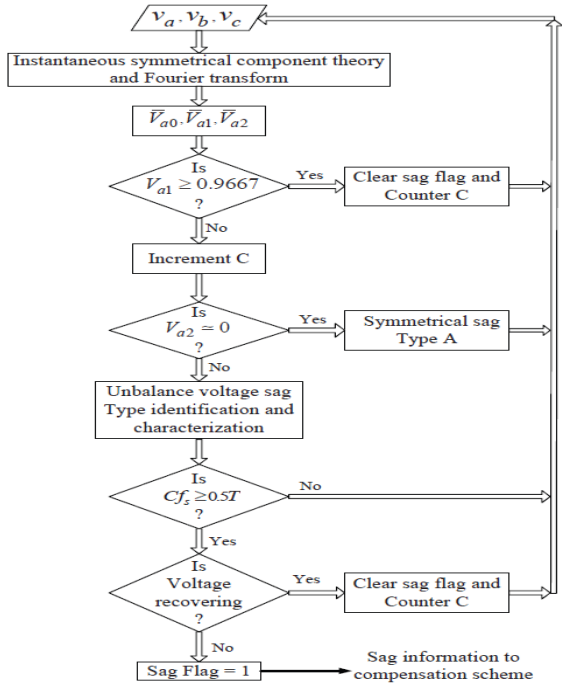


Fig.4.Algorithm flow chart sag type detection

a) Types of faults

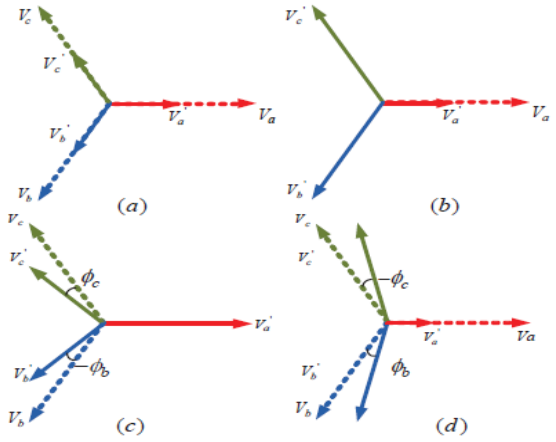


Fig.5. Types of Sag: (a) Sag Type A, (b) Sag Type B, (c) Sag Type C, (d) Sag Type D.

An intuitive method of classification of voltage sags, based on faults [2], assorts the sag into four basic types as shown in Fig. 6. In the figure, the presag load voltages are given by, V_j And c the during sag load voltages by V_j, where J=a b, and represent three phases. A single-phase fault causes voltage sag in one phase (type B) at the terminals of a star-connected load, while a symmetrical fault causes type A sag with equal voltage sag in all phases. A phase-to-phase fault causes type C sag at the terminals of a star-connected load and type D sag at the terminals of a delta-connected load as shown in Fig. 5.Each sag type is further classified into three subtypes based on the phase(s) that is/are affected. For instance, sag type Da. has phase-A affected; while for sag type Ca, the line voltage is affected and phase- voltage is healthy.

TABLE I
NUMERIZING SAG TYPES

Type Indicator(Ty)	0	1	2	3	4	5	7
Sag Type	C_a	D_c	C_b	D_a	C_c	D_b	A

TABLE II
MATHEMATICAL EQUATIONS OF THE FOUR SAG TYPES

Type A	Type Ba
$\bar{V}'_a = \bar{V}'_{ch}$ $\bar{V}'_b = -\frac{1}{2}\bar{V}'_{ch\text{-}j}\frac{\sqrt{3}}{2}\bar{V}'_{ch}$ $\bar{V}'_c = -\frac{1}{2}\bar{V}'_{ch+j}\frac{\sqrt{3}}{2}\bar{V}'_{ch}$	$\bar{V}'_a = \bar{V}'_{ch}$ $\bar{V}'_b = -\frac{1}{2}\bar{V}_{\text{-}j}\frac{\sqrt{3}}{2}\bar{V}$ $\bar{V}'_c = -\frac{1}{2}\bar{V}_{+j}\frac{\sqrt{3}}{2}\bar{V}$
Type C_a	**Type D_a**
$\bar{V}'_a = \bar{V}$ $\bar{V}'_b = -\frac{1}{2}\bar{V}_{\text{-}j}\frac{\sqrt{3}}{2}\bar{V}'_{ch}$ $\bar{V}'_c = -\frac{1}{2}\bar{V}_{+j}\frac{\sqrt{3}}{2}\bar{V}'_{ch}$	$\bar{V}'_a = \bar{V}'_{ch}$ $\bar{V}'_b = -\frac{1}{2}\bar{V}'_{ch+j}\frac{\sqrt{3}}{2}\bar{V}$ $\bar{V}'_c = -\frac{1}{2}\bar{V}'_{ch+j}\frac{\sqrt{3}}{2}\bar{V}$

While for sag type C_a, the line voltage is affected and phase-voltage is healthy. The sag type is identified using SCA by using the fact that a unique angle relation exists between positive- and negative sequence components for each type of sag [9], [10]. For sag, the angle between and is zero. Similarly, for C_b and C_c, the angle is 120 and -120, respectively. The different sags are tabulated in table I. The sag-type indicator is calculated using (3), [5] as given by

$$Ty = \frac{\lfloor \bar{V}'a2 - \lfloor \bar{V}'a1}{60^0} \qquad (3)$$

Where Ty is rounded to the nearest integer.

B. Characteristic Voltage

The characteristic voltage defines the three-phase voltage sag. For sag-type C due to a phase-to-phase fault, characteristic voltage is along the affected line voltage; for other sag types, it is the affected phase voltage (sag types A ,B and D have the affected phase voltage as their characteristic voltage), as shown in Fig. 5. The characteristic voltage can be calculated from the sequence components and the sag-type indicator using (4).

$$\bar{V}'_{ch} = \bar{V}'_{a1} - b^{(6-Ty)}\bar{V}'_{a2} + a^{(6-Ty)}\bar{V}'_{a0} \qquad (4)$$

Where $a = 1\lfloor 120^0; b = -a^2 = 1\lfloor 60^0$; and

$\bar{V}'_{a1}, \bar{V}'_{a2}$ *and* $\bar{V}'_{a0}$ are the complex positive, negative and zero-sequence components, respectively. These components are extracted using (2). The moving-average technique is employed in (2) to have better dynamic response. The sag detection by the algorithm is done by tracking the magnitude of characteristic voltage. From Table II, it can be observed that except for sag type C, is the worst affected phase voltage. Therefore, when value goes below 0.9 p.u., SF is set. For the sag typeC, since the characteristic voltage is along the line voltage, the phase voltages can be calculated using triangle properties involving the characteristic voltage, and

the characteristic phase angle ¢ , that is, the angle of as shown in Fig. 6. Using the cosine rule, the magnitudes of phase voltages are calculated as follows:

$$(\bar{V}_b)^2 = 0.25V^2 + 0.75\bar{V}'^2_{ch} - 0.867V\bar{V}'_{ch}\sin\emptyset \quad (5)$$

$$(\bar{V}_c)^2 = 0.25V^2 + 0.75\bar{V}'^2_{ch} + 0.867V\bar{V}'_{ch}\sin\emptyset \quad (6)$$

Using the sine rule, the phase jump information is derived from (5) and (6)

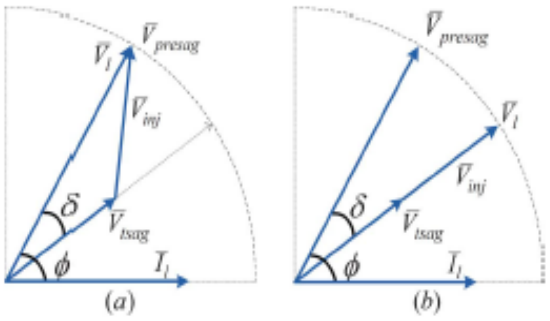
$$\emptyset_b = -60 + \sin^{-1}\left(\frac{\sqrt{3}\bar{V}'_{ch}}{2V'_c}\right)\cos\emptyset$$

$$\emptyset_c = 60 - \sin^{-1}\left(\frac{\sqrt{3}\bar{V}'_{ch}}{2V'_c}\right)\cos\emptyset$$

Generally, the algorithm takes, at most, half-a-cycle to detect sag. However, the detection time varies with sag depth, that is, deeper sag can be detected even before half-a-cycle.

IV. REFERENCE VOLTAGE GENERATION

The reference voltage required to be injected at the affected phase is derived from the characteristic voltage. Fig. 5 shows the phasor diagram for presag compensation and in-phase compensation schemes.



$\bar{V}_l = \bar{V}_{presag} = \bar{V}_{tsag} + \bar{V}_{inj}$ $\bar{V}_l = \bar{V}_{tsag} + \bar{V}_{inj}$

Fig. 6. Compensation scheme. (a) Presag compensation. (b) Inphase compensation.

The phasor diagram for presag compensation and in-phase compensation schemes. In the phasor diagram, and are the PCC phase voltages before and during sag; and are the load terminal voltage and current during sag; is the load power factor angle; and is the phase jump. For presag compensation, the sag is compensated back to the presag condition (i.e., $\bar{V}_l = \bar{V}_{presag}$) by eliminating the phase jump. While for an inphase sag compensation, the sag is compensated in magnitude only (i.e., $|\bar{V}_l| = |\bar{V}_{presag}|$) [8].For sag types except type C , the characteristic voltage is the phase voltage and, therefore, the reference voltage is calculated for presag compensation as follows(7)

$$\bar{V}_{ref} = \bar{V}_{presag} - \bar{V}'_{ch} \quad (7)$$

For the inphase compensation, the reference voltage is inphase with the characteristic voltage, and so only the magnitude is derived by (10) For sag type C , since characteristic voltage is along the line voltage, the reference voltage is calculated by using (8)

$$|\bar{V}_{ref}| = |\bar{V}_{presag}| - |\bar{V}'_{ch}| \quad (8)$$

Where is the characteristic voltage before sag. The reference voltage for the inphase compensation is derived similarly. Knowing the reference voltage to be injected, the approximate voltage corresponding to it is generated by the sag supporter.

$$\bar{V}_{ref} = \frac{\sqrt{3}}{2}(\bar{V}_{ch} - \bar{V}'_{ch}) \quad (9)$$

Here, an interphase ac–ac converter topology [1] is used for the study, since it accounts for phase-jump correction also. The switching scheme for the topology based on the characterization is discussed in the next section. The characteristics voltages for different types of sags are tabulated in table II.

V. SWITCHING LOGIC

The generation of switching logic for interphase ac–ac converter topology, which draws energy from the other two phases to compensate voltage dip in a phase, is elucidated here. There are three sectors I, II, and III as in Fig. 7(a), each comprised of two inverted phase voltages, and they represent phase- a,b ,c and sag supporters, respectively. The phase- sag supporter (sector I) with active vectors and reference voltage is shown in Fig. 7(b).

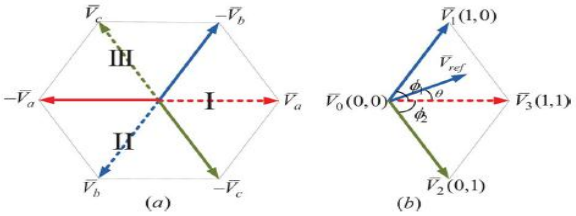


Fig. 7. Switching sequence. (a) Sectors of operation. (b) Sector I.

The active vector can be realized by switching ON the phase-chopper and OFF the phase- chopper; while vector can be realized by switching OFF the phase- chopper and ON the phase- chopper. If both the choppers are ON, the resulting vector lies over the active vector [11]. The fourth vector, zero vectors, is placed at the origin and is obtained by withdrawing the switching pulses from both choppers.

$$d_1\bar{V}_1 + d_2\bar{V}_2 = \bar{V}_{ref} \quad (10)$$

Where and are duty cycles of the choppers corresponding to the active vectors and. The duty cycles are calculated as in (11) and (12), by resolving (10) in rectangular coordinates

$$d_1 = \frac{|\bar{V}_{ref}|}{|\bar{V}_1|}\frac{\sin(\emptyset_2+\theta)}{\sin(\emptyset_1+\emptyset_2)} \quad (11)$$

$$d_2 = \frac{|\bar{V}_{ref}|}{|\bar{V}_2|}\frac{\sin(\emptyset_1-\theta)}{\sin(\emptyset_1+\emptyset_2)} \qquad (12)$$

Where is phase angle of the reference voltage, and
are phase angles of the active vectors with respect to the active vector . Since, a buck ac–ac chopper is employed to realize the injected voltage, a limit is imposed on and as given by

$$0 \le d_1 \le 1 \text{ and } 0 \le d_2 \le 1$$

The calculated duty cycles and are given to series switches of the choppers across the phase voltages corresponding to the active vectors and, that is, phase- and voltages, for a phase-sag supporter.

VI. SIMULATION STUDIES

To test the efficacy of the algorithm, two asymmetrical sags, and symmetrical sag are simulated using MATLAB, and the results are shown in Figs. 8–10. As discussed in the aforementioned sections, the magnitudes of the symmetrical components (V_{a1} ,V_{a2} , and V_{a0}), sag-type indicator , characteristic voltage , reference voltage in the affected phases, and the duty cycle of the choppers (d_1 and d_2) in the corresponding sag supporters are estimated for three sag types, and their corresponding per-unit values are listed in [11].

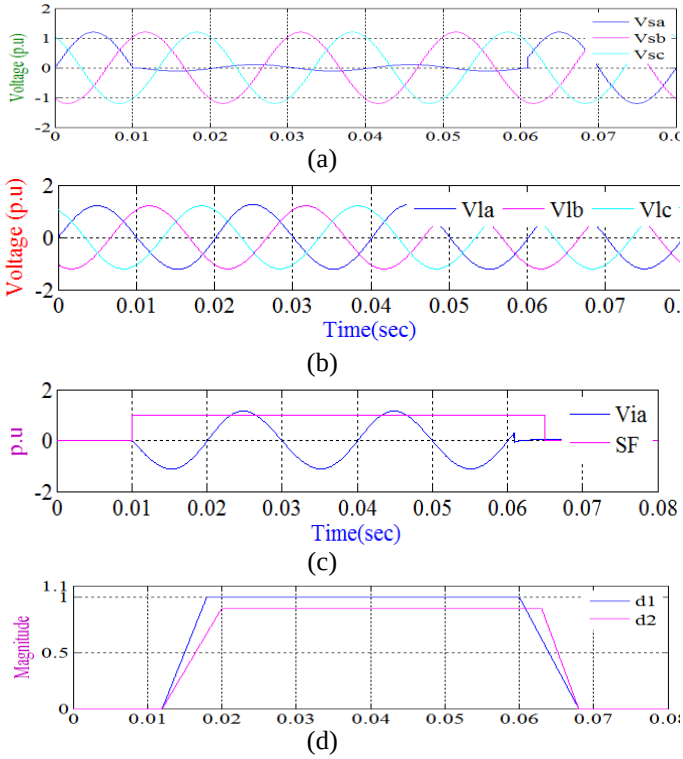


Fig. 8. Compensation of a sag typeB_a : (a) Phase voltage at the PCC with sag.(b) Load voltage. (c) Injected voltages with the sag flag (SF). (d) Duty cycle of the choppers in phase- sag supporter.

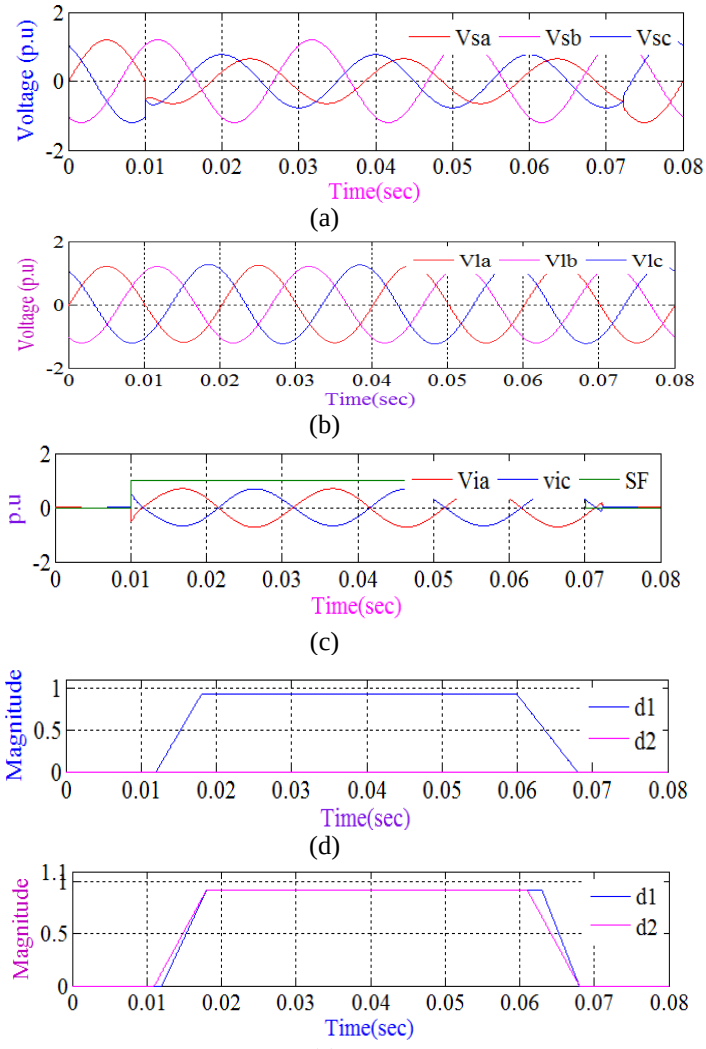
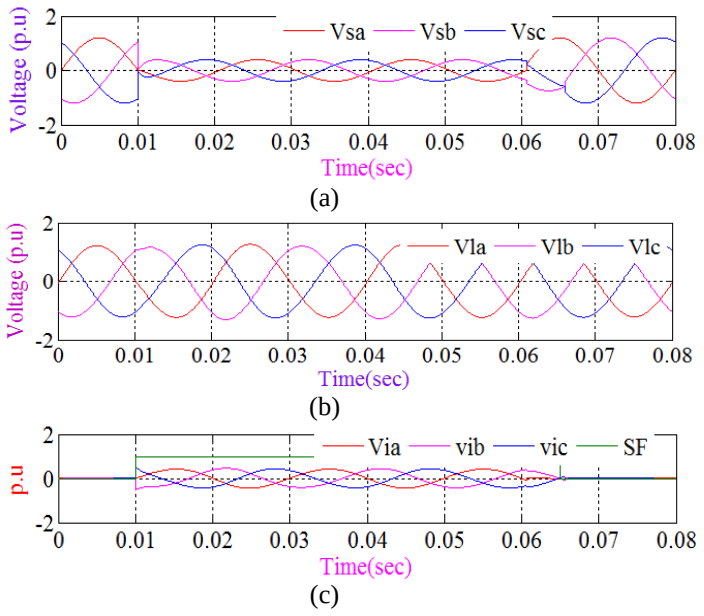
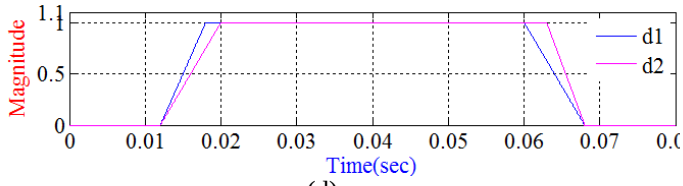


Fig. 9. Compensation of a sag type C_b : (a) Phase voltage at the PCC with sag. (b) Load voltage at the PCC. (c) Injected voltages with the SF. (d) The duty cycle of voltages in phase- sag supporter. (e) The duty cycle of choppers in phase- sag supporter.





(d)

Fig. 10. Compensation of a sag type A : (a) Phase voltage at the PCC with sag.(b) Load voltage at the PCC. (c) Injected voltages with the SF. (d) The duty cycle of choppers in all sag supporters.

Figure 9(a) to 9(d) will shows the simulation studies of single phase to ground fault .only phase a is effected and remaining two phase are healthy .that two phase sag supporters will compensate the sag. The results will show efficacy of algorithm in mitigation of voltage disturbance with 100% compensation capability in case of single line to ground fault.fig. 9(c) will shows injected voltage and fig. 9(d) will shows duty cycle of the ac chopper. It can be observed that the scheme takes half-a-cycle to compensate sag.

A type C_b sag with a characteristic voltage of 0.6 at angle - 30 is considered. Since phases are affected, both phase- and sag supporters are activated. From the characteristic voltage, the corresponding reference voltages are calculated from (11).Fig. 10(b) shows compensated voltages at the PCC, and it can be observed that the phase-voltage is compensated to the presage condition, eliminating the 29 phase jump. Fig. 10(c) shows injected voltages with SF, which is set in 1/4th of a power cycle for the case. Fig. 10(d) and (e) shows the duty cycles of the choppers in sag supporters- b and c respectively. Figure 10(a)to 10(d) will shows the simulation results of sag type A.10(a) will shows the magnitude is decreased by 50% of nominal voltage fig. 10(c) will shows the I njected voltage .the algorithm efficacy will be observed at fig. 10(b) at load side voltage .

VII.CONCLUSION

In this paper, a control scheme based on the characterization of voltage sag is proposed. It is tested on inter-phase ac–ac converter topology and it is found that the scheme besides compensation gives insight on the limits on compensation imposed by various sag types. Therefore, it aids in the flexible compensation by switching between pre-sag and in-phase compensation. The scheme provides 100% compensation for type sag, and for all other types, compensation up to 50% sag magnitude with phase jumps ranging from 60^0 to 60^0 for inter phase ac–ac topology. The algorithm takes; at most, half a cycle to compensate and it works in the presence of harmonics and unbalance, since the Fourier transform is employed to extract the fundamental component.

REFERENCES

[1] G. Venkataramanan, B. K. Johnson, and A. Sundaram, "An AC-AC power converter for custom power applications," *IEEE Trans. Power Del.*, vol. 11, no. 3, pp. 1666–1671, Jul. 1996.

[2] S. M. Hietpas and M. Naden, "Automatic voltage regulator using an AC voltage-voltage converter," *IEEE Trans. Ind. Appl.*, vol. 36, no. 1, pp. 33–38, Jan./Feb. 2000.

[3] E. C. Aeloíza, P. N. Enjeti, L. A. Morán, O. C. M. Hernandez, and S. Kim, "Analysis and design of a new voltage sag compensator for critical loads in electrical power distribution systems," *IEEE Trans.Ind. Appl.*, vol. 39, no. 4, pp. 1143–1150, Jul./Aug. 2003.

[4] S. Subramanian and M. K. Mishra, "Interphase AC-AC topology for voltage sag supporter," *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 514–518, Feb. 2010.

[5] A. Prasai and D. M. Divan, "Zero-energy sag corrector with reduced device count," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1646–1653, Jun. 2009.

[6] J. Suma and M. K. Mishra, "Instantaneous symmetrical component theory based algorithm for characterization of three phase distorted and unbalanced voltage sags," in *Proc. IEEE Int. Conf. Ind. Technol.*, Feb.2013, pp. 845–850.

[7] M. Bollen, "Algorithms for characterizing measured three-phase unbalanced voltage dips," *IEEE Trans, Power Del.*, vol. 18, no. 3, pp. 937–944, Jul. 2003.

[8] L. D. Zhang and M. H. J. Bollen, "Characteristic of voltage dips (sags) in power systems," *IEEE Trans. Power Del.*, vol. 15, no. 2, pp.827–832, Apr. 2000.

[9] *IEEE Recommended Practice for Emergency and Standby Power Systems for Industrial and Commercial Applications*, IEEE Standard 446-1995, Jul. 3, 1996.

[10] D.M. Vilathgamuwa, A. A. D. R. Perera, and S. S. Choi, "Voltage sag compensation with energy optimized dynamic voltage restorer," *IEEE Trans. Power Del.*, vol. 18, no. 3, pp. 928–936, Jul. 2003.

[11] Suma Jothibasu, MaheshK.Mishra "A Control Scheme for Storageless DVR Based on Characterization of Voltage Sags" *IEEE Transactions On Power Delivery*, VOL. 29, NO. 5, OCTOBER 2014.pp 2261-2269.

SK.GHOUSE MODIN, he was born in 1988. His obtain bachelor degree in electrical & electronics engineering in 2009 from MEC, kadapa. His obtain post graduation in Power & Industrial Drives in 2011from NCET, Vijayawada. Currently his working as a assistant professor in AITS, kadapa. His published varies 14 international Conferences / Journals. His interested areas are application of power electronic devices to power systems, drives, generation of non-conventional energy and grid interconnected systems.

His also Life Member of Indian Society for Technical Education

M.BALA SIVA PRASAD, he was born in 1986. His obtain bachelor degree in electrical & electronics engineering in 2007 from SSITS, Rayachoti. His obtain post graduation in Electrical Power Systems in 2012 from SKDEC, Gooty. Currently his working as a assistant professor in AITS, kadapa. His published varies 05 international Conferences /Journals. His interested areas are power systems, generation of non-conventional energy and grid interconnected systems, Electrical Machines.

C.MOULALI, he was born in 1992.his obtain bachelor degree in electrical & electronics engineering in 2013 from ssit, Anantapur. Currently his pursuing post graduation in electrical power systems in AITS, kadapa. His interested areas are Power Systems.