International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 3 Issue 7, July - 2014

An Advanced Multilevel Inverter with Reduced Switches using Series Connection of Sub Multilevel Inverters

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Abstract—This paper presents an improved multilevel inverter with reduced switches using series connection of sub multilevel inverters. It is popularly adapted for high power applications and is partly because of high quality output waveform of multilevel inverter when compared to two level inverters. In this paper a new topology for sub multilevel inverters is proposed as an improved or advanced multilevel inverter. The proposed multilevel inverter uses reduced number of switching devices. Special care is needed to obtain optimal structure regarding criteria such as number of switches, standing voltage on the switches, number of DC voltage sources and etc. The proposed multilevel inverter is simulated for a symmetric thirteen level inverter, asymmetric thirty one level inverter using MATLAB software. The main attention behind the objective of proposed asymmetric thirty one level inverter topology is to achieve the high power quality, low total harmonic distortion, less electromagnetic interference and better power factor.

Keywords- Multilevel inverter, sub multilevel inverter, optimal structure, cascaded H-bridge inverter (CHB).

I INTRODUCTION

The proposed multilevel inverter includes an array of power semiconducting devices and dc voltage sources; it generates the output voltage with stepped waveforms. Compared to conventional multilevel inverters, proposed multilevel inverter is used to synthesize the output voltage and current with reduced harmonic distortion and lower electromagnetic interference (EMI). By increasing number of levels in the output of multilevel inverter, the output voltage will have more number of steps in generating a staircase waveform, which results in reduced harmonic distortion. However, the generation of large number of levels in the output will increase the number of devices and that will be controlled or compensated by the proposed multilevel inverter topology. That means the complexity of the equipment is minimized.

Conventional multilevel inverter like cascaded H-bridge inverter (CHB), it uses series connected H-bridge cells with an isolated DC voltage sources connected to each cell. Number of capacitors and switching devices will be increased for high level output in cascaded H-bridge inverter. To avoid this problem, a new multilevel inverter topology is proposed. In which, the proposed sub multilevel inverter is as shown in Fig.1; this topology consists of n dc voltage sources. In general, the dc voltage sources may have different values. In this paper 31-level inverter is introduced using series connection of sub multilevel inverters.

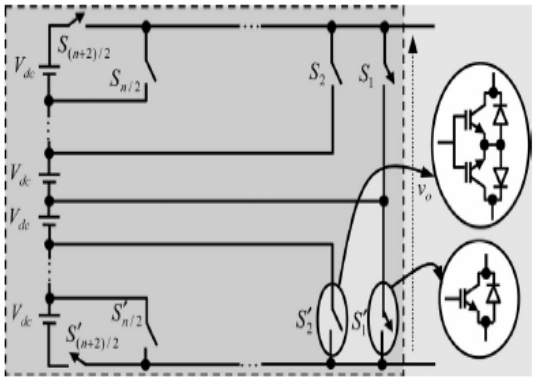

Fig.1 Proposed sub multilevel Inverter.

II PROPOSED MULTILEVEL INVERTER

The multilevel inverters can be divided into two groups from the view point of the dc voltage sources amplitudes: the symmetric and the asymmetric topologies. In the symmetric topology, the values of all of the dc voltage sources are equal. This characteristic gives the topology with good modularity. However, the number of the switching devices will be increased by increasing the

number of output voltage level. In order to increase the number of output voltage level, the values of the dc voltage sources are selected to be different, these topologies are called asymmetric.

In this chapter, we will discuss about two categories of inverters; one is 13-level inverter and based on the proposed symmetric level inverter and another one is 31-level inverter based on the proposed asymmetric topology. In 13-level inverter with proposed terminology, six DC voltage sources each of them 25V are used to generate the maximum output voltage of 150V (Number of voltage sources P=3 for each sub multilevel inverter). The number of IGBTs used in the proposed 13-level inverter is 19. But from literature knowledge, the number of IGBTs required for CHB is 24. That means cost of the switching devices can be curtailed. Its circuit diagram is as shown in Fig. 2, a designed multilevel inverter with peak voltage amplitude of 150V having 31-levles of output voltage.

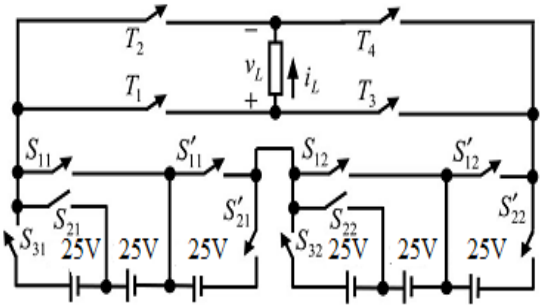

Fig. 2 Thirteen level inverter with proposed symmetric inverter topology, P=3 and Q=2.

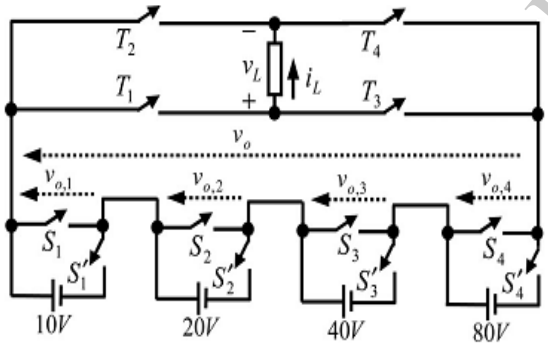

Fig. 3 proposed asymmetric thirty one - level inverter topology, P=1 and Q=4.

The proposed multilevel inverter is optimal for P= 1 (n means number of input DC sources for sub multilevel inverter) from different points of view. In order to get the number of output voltage to be higher, the number of cascaded sub multilevel inverters should be 4 (Q=4). Therefore a 31-level 150V inverter based on the proposed multilevel inverter is as shown in Fig. 3. In this topology voltage magnitude of the DC voltage sources is distinct for each sub multilevel inverter.

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III OPERATION PRINCIPLES

Multilevel inverter can be formed by series connection of sub multilevel inverters. If we consider a sub multilevel inverter with 'P' number of input DC voltage sources, it uses (P+2) switches.

During the operation of proposed multilevel inverter topology, some of the switches are unidirectional and other switches are bidirectional. The unidirectional switches consist of an IGBT (Insulated Gate Bipolar Transistor) with an antiparallel diode.

In this chapter, we will analyze the generalized sub multilevel inverter because the number of input DC sources is not common for symmetric and asymmetric topologies. The switches S_1, S_1^1 and $S_{(P+2)/2}$, $S_{(P+2)/2}^1$ are unidirectional and other are bidirectional. Hence, these switches have to withstand both positive and negative voltages. At instance, when $S_{(P+2)/2}$ is turned ON, the voltage equal to $-V_{dc}$ is on the switch $S_{P/2.}$ The same analysis will be applied for the other switches. Therefore, the switches have to withstand both positive and negative voltages. In addition to this, the switches have to conduct backward current as a result of inductive characteristic of the load. It concludes that the switches must be bidirectional.

TABLE I
Output voltages for states of switches

STATE	Switching states									V_o
	S_1	S_1^1	S_2	S_2^1	…	$S_{P/2}^1$	$S_{P/2}$	$S_{(P+2)/2}$	$S_{(p+2)/2}^1$	
1	1	1	0	0	…	0	0	0	0	0
2	0	1	1	0	…	0	0	0	0	V_{dc}
3	0	0	1	1	…	0	0	0	0	$2V_{dc}$
:	:	:	:	:	…	:	:	:	:	:
P-1	0	0	0	0	…	1	1	0	0	(P-2) V_{dc}
P	0	0	0	0	…	0	1	0	1	(P-1) V_{dc}
P-1	0	0	0	0	…	0	0	1	1	PV_{dc}

There are several circuit configurations for bidirectional switches. In this paper, the common mode emitter topology is used as it needs one gate driver for a switch. Considering the types of the switches, 2P number of IGBTs is required in the proposed sub multilevel inverter. The number of diodes would be 2P, because diodes are connected in parallel to IGBTs. The proposed sub multilevel inverter will generate zero and positive voltage levels. The zero voltage level is obtained when the switches S_1 and S_1^1 are turned ON simultaneously. The other voltage levels can be generated by the proper switching of the switches. Table I shows the states of switches for each output voltage value. In the above table, 1 indicates ON state and 0 indicates OFF state of the switches.

Referring Fig.1, for each value of the output voltage of sub multilevel inverter, two switches must be turned ON, in which one from the upper switches and other from the lower switches. For example, to get an output voltage of V_{dc}, the switches S_1^1, S_2 are turned ON. In order to obtain the output voltage of $(P-1)V_{dc}$, the switches $S_{P/2}$ and $S_{(P+2)/2}$ should be turned ON.

In this paper we will analyze simulation results for proposed topologies and are given below.

A.SYMMETRIC TOPOLOGY

The proposed 13-level symmetric inverter with P=3 as shown in Fig. 2. Six DC voltage sources each of them 25V are used to get the maximum output voltage of 150V. Fig. 5 & Fig. 6 show the load voltage and load current of 13-level inverter. Expected results are obtained with this topology.

B. ASYMMETRIC TOPOLOGY

For the asymmetric topology, proposed 31-level inverter is given and is simulated for results. The aim is to design a peak 150V using proposed 31-level inverter. In this topology, the assumptions are P=1, Q=4.The values of voltages are shown in Fig. 3 and this topology uses twelve IGBTs. Simulated results for output voltage and output current are shown in figures 9 & 10 respectively.

IV SIMULATION RESULTS

A.THIRTEEN LEVEL INVERTER BASED ON PROPOSED SYMMETRIC TOPOLGY

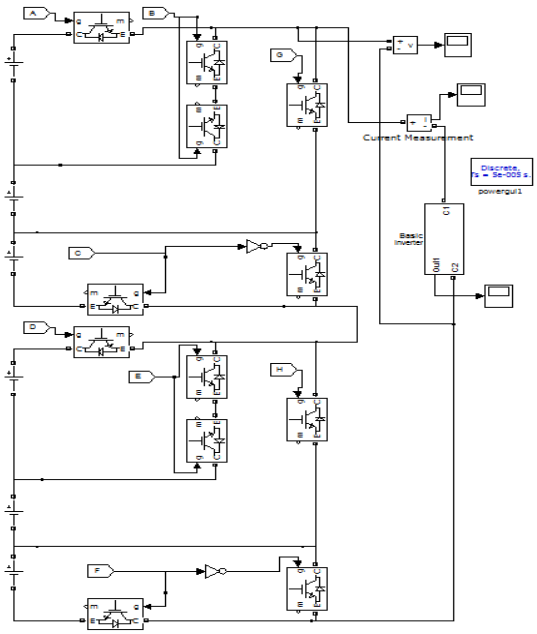

Fig.4 Simulation circuit for proposed 13-level inverter

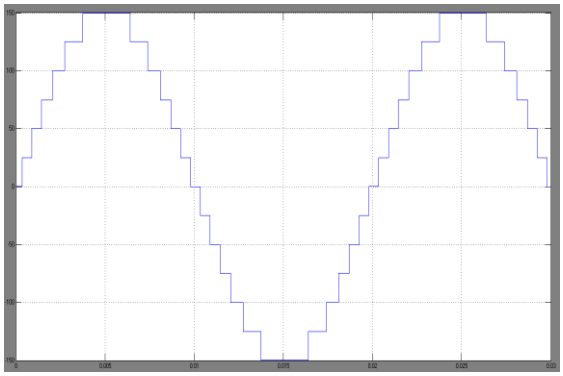

Fig.5 Output voltage of proposed 13-level inverter

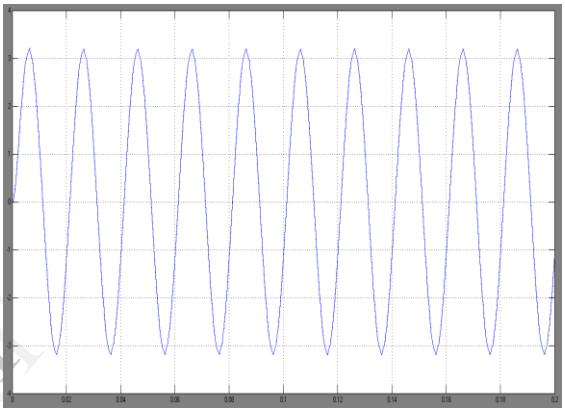

Fig. 6 Output current of proposed 13-level inverter

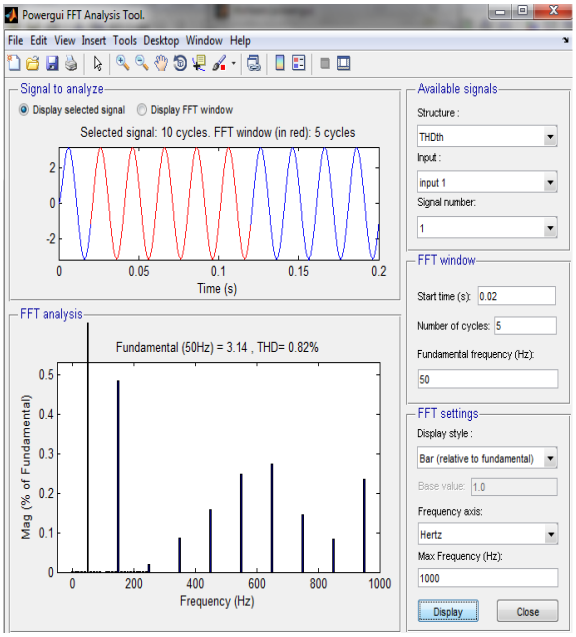

Fig. 7 THD (Total Harmonic Distortion) of output current for proposed 13-level inverter

B.THIRTY ONELEVEL INVERTER BASED ON PROPOSED ASYMMETRIC TOPOLGY

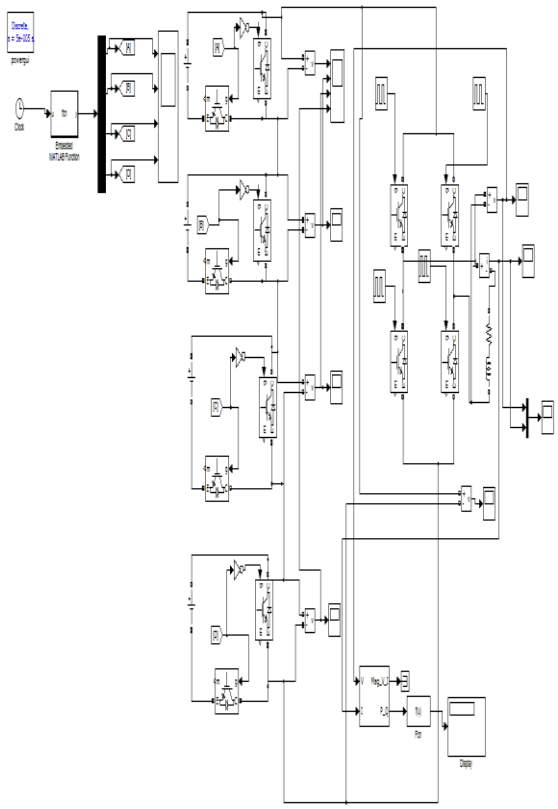

Fig. 8 Simulation circuit for proposed 31-level inverter

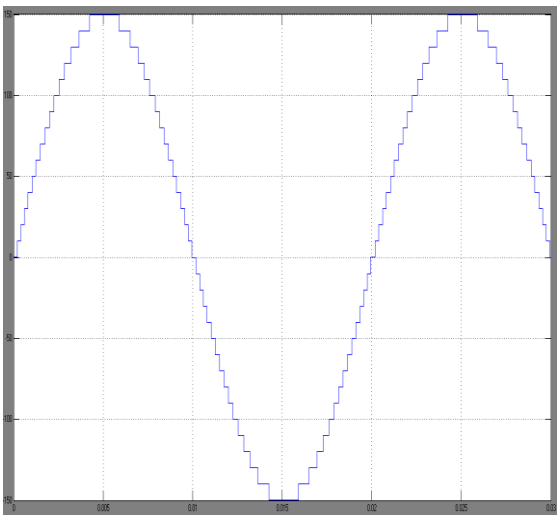

Fig. 9 Output voltage of proposed 31-level inverter

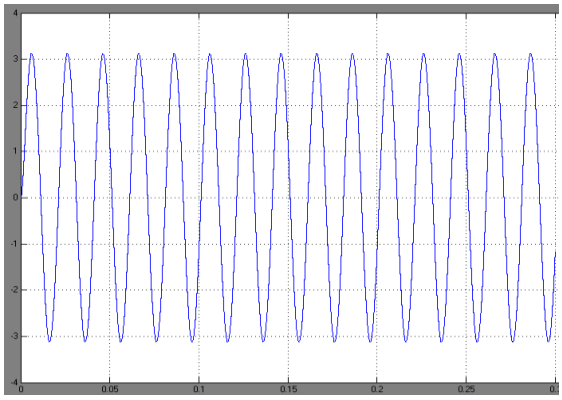

Fig. 10 Output current of proposed 31-level inverter

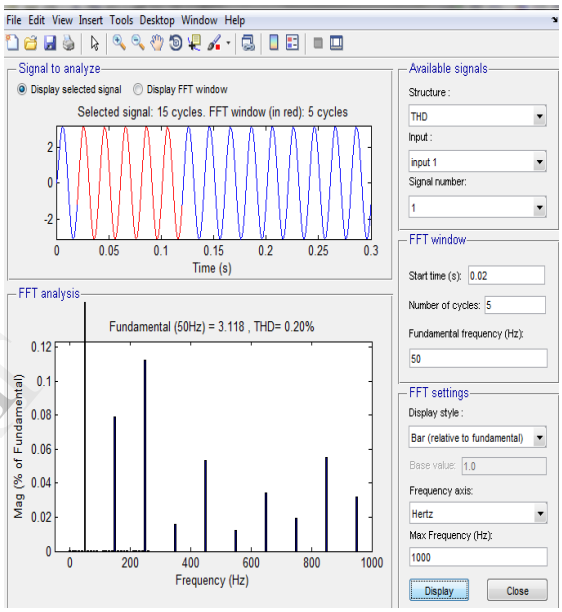

Fig. 11 THD (Total Harmonic Distortion) of output current for proposed 31-level inverter

These are the results obtained for 13-level inverter, 31-level inverter using series connection of proposed sub multilevel inverters. As we observe the results, THD for output current of 13-level inverter and 31-level inverter is 0.82% and 0.20% respectively. That means the percentage value of THD is less for the proposed system and it will be reduced further with increased number of levels in output. The power factor is improved with these proposed topologies and is measured as 0.9 that means approximately unity. Required switching devices are reduced compared to conventional multilevel inverters. Therefore, the proposed inverter topologies based on proposed sub multilevel inverter provided best performance results with impressive manufacturing cost.

V. CONCLUSION

A sub multilevel inverter is proposed initially and then a cascaded sub multilevel inverter with 13-level and 31-level inverter topologies is considered in both symmetric and asymmetric conditions. The comparison between both the proposed topologies is presented with

simulation results. The role of the proposed sub multilevel inverter is described in the generation of desired output voltage. Finally we can conclude that best performance is achieved with the proposed inventions at economic conditions.

VII. REFERENCES

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