An Area Efficient Low Power TG Full Adder Design using CMOS Nano Technology

[1]Shivani Singh
[1]M.tech, Digital Communication,
RTU, KOTA

[2]Buddhi Prakash Sharma
[2]ME Scholor, Electronics & Comm., NITTTR, Chandigarh, India

[3]Sanjay Kumar Singhal
[3]Assistant Professor, Elect. & Commu.
RIET, Jaipur

Abstract: Full adders are the basic building block of ALU and ALU is an essential unit of the microprocessors and DSP. In the world of technology it has become necessary to develop various new design methodologies to reduce the power and area consumption. In this paper transmission gates have been used to develop the proposed full adder using 4 transistors XOR and XNOR gates. The carry logic has been efficiently implemented using 2:l MUX to reduce transistor count. The reduction in Transistor count results in improved area and power consumption. The proposed full adder has been designed using 10 transistors using 32 nm CMOS technologies. The developed adder with 10 transistors XOR/XNOR have shown an improvement of 65.63%/44.08% in power and 38.106% in area so as to implement adder efficiently in digital signal processors.

Keywords- DSCH, full adder, transmission gate (TG), Mux, XOR/XNOR.

IJERT

I. INTRODUCTION

In VLSI design methodologies power reduction is one of the primary aspects because a long battery life is required for cell phones and portable devices, Power dissipation is increasing as number of transistors increases on a single chip. The electronics industry has achieved a phenomenal growth over the last couple of decades, mainly due to the rapid advances in integration technologies (IC) and large scale systems design. The level of integration as measured by the number of logic gates in a monolithic chip. Adder is one of the most critical components of a processor, as it is used in the arithmetic logic unit (ALU), in the floating point unit, and for address generation in case of cache or memory access [1]. Digital CMOS (Complementary Metal Oxide Semiconductor) integrated circuits (ICs) have been the driving force behind Very Large Scale Integration (VLSI) for high performance computing and other scientific and engineering application CMOS logic families are an obvious choice for low-power logic due to their simplicity and the fact that simply scaling the supply voltage can allow the same circuit to be used under a wide performance range in terms of speed and power consumption. Increasing demand for mobile electronic devices such as mobile phones, PDA's, and laptop computers requires the use of power efficient VLSI circuits. The Full Adder is a combinational circuit with three inputs, i.e. Bitl (X),Bit2 (Y), and Carry in (Z) and two outputs i.e. Sum and Cout (Carry). The Boolean expressions for some and carry is given bellow:

$$\left.\begin{aligned} Sum &= X \oplus Y \oplus Z \\ Carry &= XY + YZ + ZX \end{aligned}\right\}$$

Where X, Y, Z are the inputs.

In any CMOS VLSI circuit design dynamic power plays most important role. Thus, for analyzing Full Adder cell only dynamic power is of interest. During a transition from either low to high (‘0’ to ‘1’) or alternatively from high to low (‘1’to ‘0’) both PMOS and NMOS transistors are ON for a short span of time. This results in short current pulse from VDD to GND. Current is also required in charging and discharging the output capacitive load. The current pulse from VDD to GND results in a “short circuit” dissipation that is dependent on the input either rise time or fall time as well as the load capacitance and the gate design. Condition having no load capacitance, the “short circuit” current is noticeable. As the capacitive load is increased, the charging or discharging current starts to dominate the current drawn from the power supplies. The dynamic power dissipation can be modeled by assuming that the rise time and fall time of the unit step input is much less than the repetition period. The average dynamic power ($P_{dynamic}$), dissipated during switching for a square wave input (V_{in}), having a repetition frequency of $f_p=1/t_p$, is given by

$$P_{dynamic} = \frac{1}{t_p}\int_0^{t_p/2} i_n(t)V_{out}dt + \frac{1}{t_p}\int_{t_p/2}^{t_p} i_n(t)(V_{DD}-V_{OUT})dt \quad (1)$$

For unit step input & with $i_n=C_L(dV_{OUT}/dt)$, where C_L is load capacitance. Now we obtain the following expression for dynamic power $P_{dynamic}$:

$$P_{dynamic} = \frac{C_L}{t_p}\int_0^{V_{DD}} V_{OUT}.dV_{OUT} + \frac{C_L}{t_p}\int_{V_{DD}}^{0}(V_{DD}-V_{OUT})d(V_{DD}-V_{OUT}) = \frac{C_L}{t_p}V_{DD}^2 \quad (2)$$

with $f_p=1/t_p$ results $P_{dynamic}=C_L V^2_{DD}.f_p$ (3)

or repetitive step input, the average power dissipation is proportional to the energy required in charging and discharging the circuit capacitance. The important factor is that eq. (3) shows power to be directly proportional to switching frequency but

independent of the device parameters [2]. A transmission gate has three inputs called source, n-gate and p-gate. It also has one output called drain. A CMOS transmission gate [3] can be constructed by parallel combination of NMOS and PMOS transistors, with complementary gate signals like X, Xbar as shown below. As such, the CMOS TG operates as a bidirectional switch between the nodes IN and OUT which is controlled by signal X. If the control signal X is equal to VDD, then both transistors are turned on and provide a low-resistance current path between the nodes IN and OUT. If, on the other hand, the control signal X is low, then both transistors will be off, and the path between the IN and OUT will be an open circuit. The main advantage of the CMOS transmission gate compared to NMOS transmission gate is to allow the input signal to be transmitted to the output without attenuation in the threshold voltage. The schematic diagram and symbol of transmission gate is shown in Fig 1 shown below.

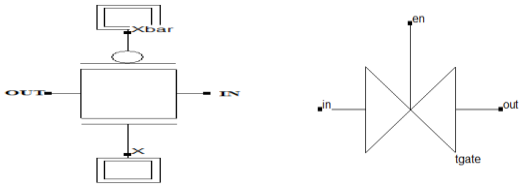

Figure 1 Schematic diagram & Symbol of Transmission gate

When the voltage on node X is a Logic 1, the complementary Logic 0 is applied to node active low X, allowing both transistors to conduct and pass the signal at IN to OUT. When the voltage on node active-low X is Logic 0, the complementary Logic 1 is applied to node X, turning both transistors off and forcing a high-impedance condition on both the IN and OUT nodes.

II. PREVIOUS WORKS

Various full adder circuits have been presented in literature [4] - [7]. 28 transistors conventional full adder is given in Fig.2 [4].In this adder design PMOS network is same as NMOS network. Due to high number of transistors, its power consumption is high. Large PMOS transistor in pull up network results in high input capacitances, which cause high delay and dynamic power. One of the most significant advantages of this full adder was its high noise margins and thus reliable operation at low voltages.

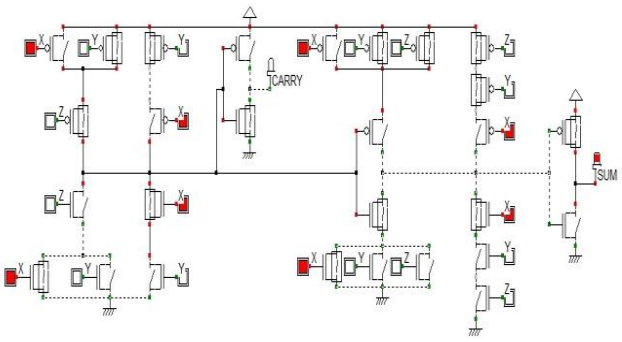

Figure 2: The conventional design of CMOS Full Adder with 28 Transistor [1]

26 transistors transmission gate full adder is shown in Fig-3 [5] .Schematic of this circuit is simple as compared to previous one. This full adder consists less transistors count as compared to conventional one.

26 transistors transmission gate full adder is shown in Fig-3 [5] .Schematic of this circuit is simple as compared to previous one. This full adder consists less transistors count as compared to conventional one.

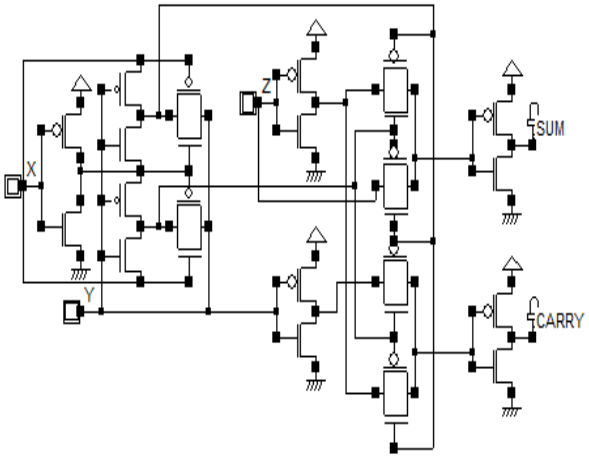

Figure 3: TG Full Adder by 26 transistors

20 transistors full adder by using pass transistor logic is shown in Fig-4 [6]. Although the transistor count is less as compared to previous one but the circuit consume more power and give the slower speed due to threshold loss problem.

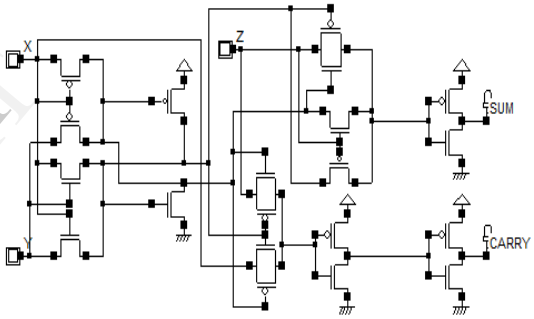

Figure 4: Pass transistor based Full Adder by 20 transistors

III. PROPOSED FULL ADDER

The proposed full adder uses pass transistor logic and transmission gate. Which follows the Boolean equation as shown below where X, Y, Z are the inputs and SUM and CARRY are the outputs of full adder.

$$SUM = \overline{X}\,\overline{Y}Z + \overline{X}Y\overline{Z} + X\overline{Y}\,\overline{Z} + XYZ$$
$$CARRY = \overline{X}YZ + X\overline{Y}Z + XY\overline{Z} + XYZ \qquad (4)$$

The exclusive–OR (XOR) and exclusive–NOR (XNOR) gates are the basic building blocks of a full adder circuit. The XOR/ XNOR gates can be implemented using AND, OR, and NOT gates with high redundancy [8]. Optimized design of these logic gates increases the performance of VLSI systems as these gates are utilized as sub blocks in larger circuits. XNOR/XOR design with less number of transistors, lesser power dissipation and delay are highly desirable for efficient implementation of the large VLSI system.

IJERT

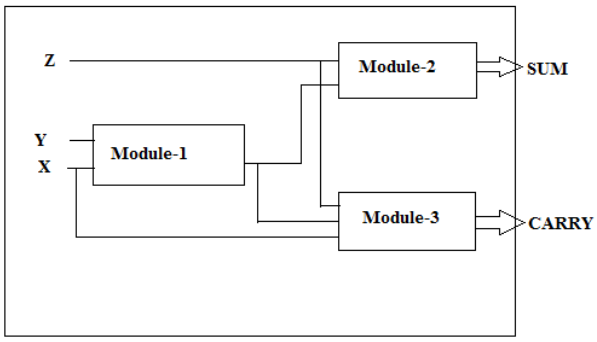

Figure 5: Structure of single bit Full Adder

Structured approach for implementation of single bit full adder using XOR/XNOR has been reported [9] as shown in Figure5. With decomposition of full adder cell into smaller cells with the help of modules. Module-1 represent the XOR gate, which perform XOR operation on two bit X, Y can also be known as half sum. Module-2 again represent XOR gate but having inputs bit Z and output of module-1. It gives the output which is known as sum of full adder. Module-3 works as a 2:1 multiplexer, having inputs bit X, Z and gives output which is known as carry of full adder. CMOS transmission gate Figure 6 shows an eight-transistor implementation of the logic XOR function, using two CMOS TGs and two CMOS inverters.

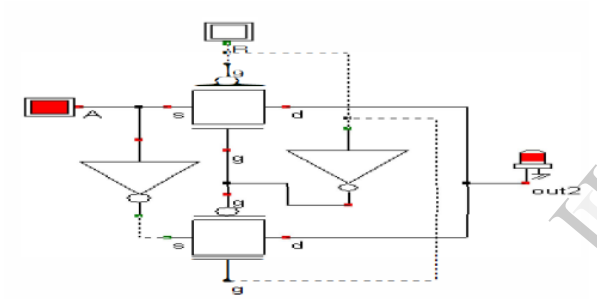

Figure 6: Eight-transistor CMOS TG implementation of the XOR function [10].

The same function can also be implemented using only six transistors, as shown in fig. 7

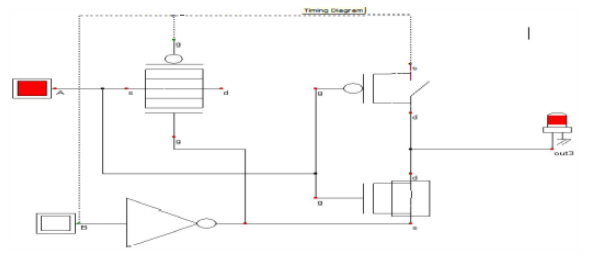

Figure 7: Six-transistor CMOS TG implementation of the XOR function [10].

We further reduced the number of transistors in proposed XOR/XNOR cell as shown in fig. 8.

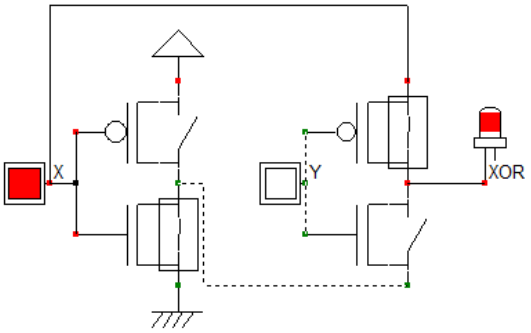

Figure 8: Proposed 4-Transistor XOR cell

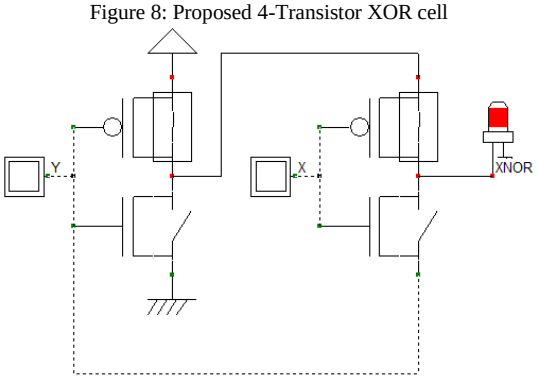

Figure 9: Proposed 4-Transistor XNOR cell

Comparisons of area and power of this design fig. 6,7,8,9 is shown below in table below.

Table 1: Comparison of different XOR/XNOR cell

XOR/XNOR CELL	AREA um^2	POWER uw
8 transistor TG	12.5	1.697
6 transistor TG	9.6	1.085
4 transistor xnor	8.3	0.705
4 transistor xor	8.3	0.689

IV SCHEMATIC DESIGN OF TG FULL ADDER

A. TG full adder circuit with 2:1 mux

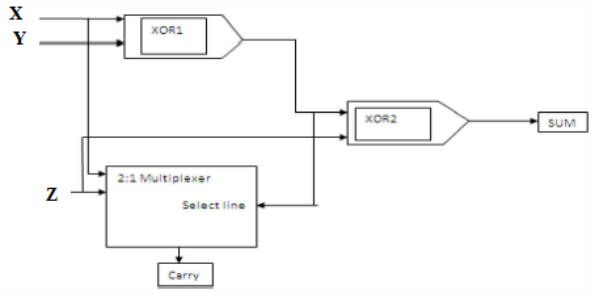

Figure 10: Proposed FA cell with 2:1 mux

Figure 10 indicates a full adder design using 2 XOR cells and one 2:1 mux which are shown below in fig. 11.

IJERT

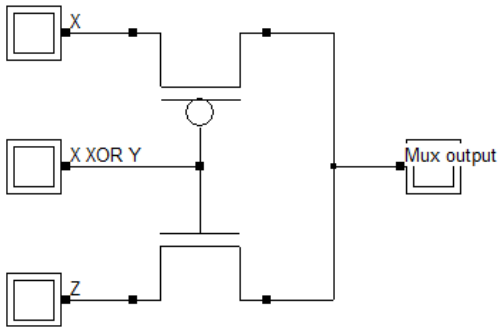

Figure 11: Proposed 2:1 multiplexer

B.TG full adder block diagram by using proposed 4T XOR/XNOR

TG Full adder design of full adder by using 10 transistors is shown in fig. 12. This full adder circuit is made by using 4 transistor XOR circuit shown in fig-8. Area and power consumed by this circuit is less as compared to full adder circuit made by XOR circuit in fig -6, 7 and having same area as 4 transistor xnor cell but consumes less power than xnor cell based full adder shown in fig. 13.

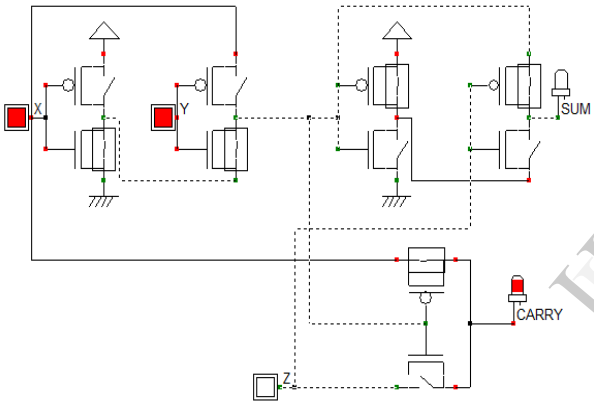

Figure 12: Proposed 10TG FA design based on XOR cell

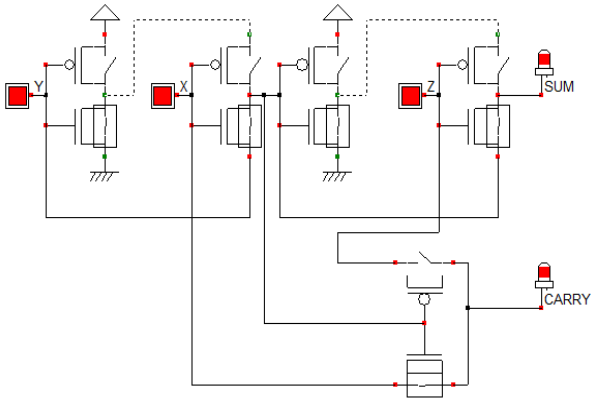

Figure 13: Proposed 10TG FA design based on XNOR cell

IV. SIMULATION AND LAYOUT

Reduction of power consumption provides a great improvement to an adder circuit. Power consumption issues can lead to over consumption of resources when devices are added serially. This reduction in power would come at the expense of overall speed and increased delay.

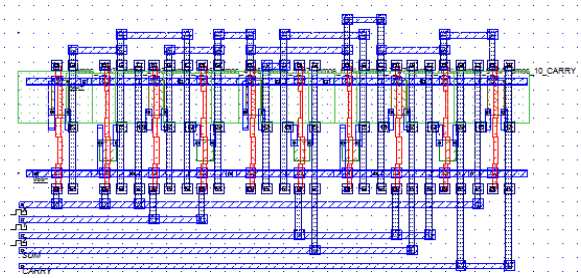

Figure 14: Layout design of Proposed 10TG XOR FA

This section presents the layout and analog simulation of various designs. These designs are simulated using Microwind 3.l tool. The simulation is performed using schematic entry and its functionality is verified in DSCH 3.5. After verification VERILOG file is generated. VERILOG is compiled to get physical layout of schematic designs.

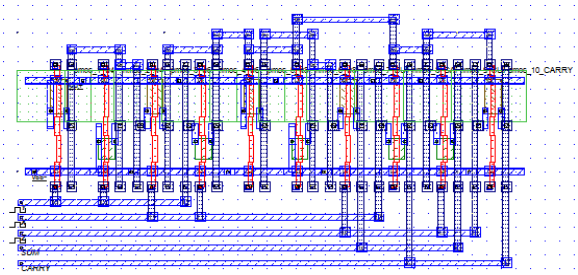

Figure 15: Layout design of Proposed 10TG XNOR FA

Using layout of circuit values like power, resistance, Capacitance, node voltage and current can be estimated. Layout and analog simulation of various designs are shown in figs 14,15,16,17. Layout shows the various metal layers and their interconnection through via. Fig. 14 and 15 shows the layout and 16 and 17 shows the analog simulation of various designs.

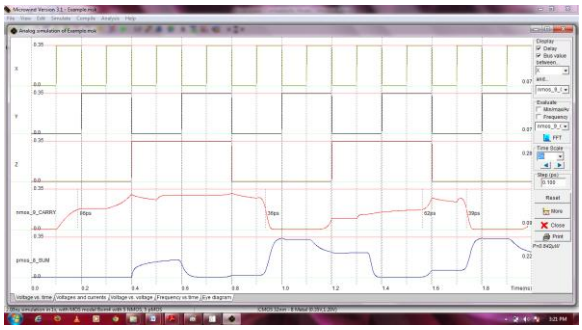

Figure 16: Analog simulation result of proposed 10TG XOR FA

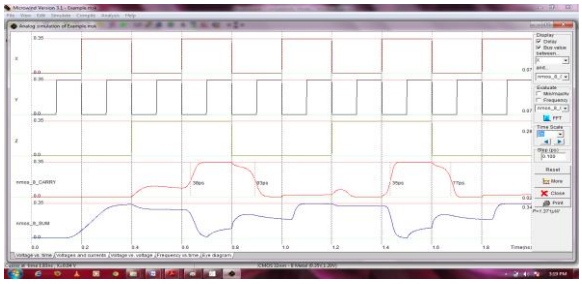

Figure 17: Analog simulation result of proposed 10TG XNOR FA

On the basis of MICROWIND designing tool we make the performance comparison between of area and power of CMOS

IJERT

full adder, TG full adder by 27T, TG full adder design with 2xl MUX which consist 18 transistors and TG proposed full adder. Different full adder structure comparison is shown in table2 below.

Table 2: COMPARATIVE STUDY OF AREA AND POWER OF VARIOUS TG FULL ADDER DESIGNS

Design	Power	Area	Transistor Count
18 TG FA	3.68uw	58.4um^2	18
14 TG FA	2.45uw	41.2um^2	14
10 TG XNOR FA	1.371uw	25.5um^2	10
10 TG XOR FA	0.842uw	25.5um^2	10

Power consumed by each design is 3.68uw, 2.45uw, 1.371uw, 0.842uw respectively. Power consumed by 10TG XOR full adder is 0.842 less then 10TG XNOR full adder.

V. CONCLUSION

This paper presents an area and power efficient technique to design a full adder, using transmission gate and 2:1 mux in order to reduce transistor count. Most of the conventional CMOS adders have been designed using 28 transistors which are very high. As number of transistors increases results in high power consumption. To overcome this problem, the proposed full adder has been designed using less number of transistors (10T) to improve the power and area simultaneously. Two full adders have been designed using 10 transistors with XOR and XNOR cell. The full adder using 10 TG XOR/XNOR consumes power and area respectively 1.371uw/0.842uw and 25.5um^2 each. All the results are simulated using MICROWIND3.1.

IJERT

REFERENCES

[1] R. Shalem, E. John, L. K. John, "A Novel Low Power Energy Recovery Full Adder Cell," in Proc. IEEE Great Lakes VLSI Symp., Feb. 1999, pp. 380-383.

[2] A. M. Shams and M. A. Bayoumi, A framework for fair performance evaluation of 1-bit full adder cells, In *Proceedings of the 42nd Midwest Symposium on Circuits and Systems*, vol. 1, pp. 6-9, IEEE Computer Society Press, August 1999.

[3] D. Markovic, B. Nikolic, V.G. Oklobdz, "A general method in synthesis of pass-transistor circuits," Microelectronics Journal 31 (2000).

[4] N. Weste and K. Eshraghian, "Principles of CMOSVLSI Design", A System Perspective. Reading, MA: Addison-Wesley, 1993.

[5] N. Zhuang and H. Wu, A new design of the CMOS full adder," IEEE Journal of Solid-State Circuits, vo1. 27, No. 5, pp. 840-844, May 1992.

[6] K.-H. Cheng and c.-S. Huang, "The novel efficient design of XORlXNOR function for adder applications," in Proc. of the 6th IEEE International Conference on Electronics. Circuits and System, vo1. 1 ,pp.29-32, 1999 .

[7] Chiou-Kou Tung; Yu-Cherng Hung; Shao-Hui Shieh; Guo-ShingHuang," A Low -Power High-speed Hybrid CMOS Full Adder For Embedded System," IEEE transactions on Design and Diagnostics of Electronic Circuits and Systems ,vo1. 13 , No.6, pp.-1 - 4, 2007

[8] Y. Leblebici, S.M. Kang, CMOS Digital Integrated Circuits, Singapore: Mc Graw Hill, 2nd edition, 1999.

[9] Ahmed M. Shams and Magdy A, "A structured approach for designing low power adders," Conference Record of the Thirty-First Asilomar Conference on Signals, Systems & Computers, vol.1, pp.757-761, Nov. 1997.

[10] Anjali Sharma, Richa Singh, Rajesh Mehra, "Low Power TG Full Adder Design Using CMOS Nano Technology", 2nd IEEE International Conference on Parallel, Distributed and Grid Computing, pp. 210-213, 2012