An Efficient Design Approach of BCD to Excess-3 Code Converter Based on QCA

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Abstract— **A new hierarchical design is built by using Quantum dot Cellular Automata (QCA) [1] [2] [7] circuits. Now a day, the world is running towards the digital life and meanwhile the electronic devices are becoming very lesser in size. Presently, the digital circuits are implementing through one of the high performance complementary metal-oxide semiconductor (CMOS) technologies i.e. Nanotechnology. Quantum dot is a Nano-scale device and ultra-low power consumption compared with transistor-based technologies, it's a very powerful tool which intern makes the design smarter to the further level i.e., Quantum dot Cellular Automata (QCA).Quantum dot Cellular Automata is one of the emerging technologies and it is a new architecture which transfers information only through the interaction between the cells. This paper represents the fundamental concepts of QCA which also includes the basic cells, wires and its types, majority gates, clocking levels, basic logic gates and its significance. The main motto of this project is to introduce an efficient design approach of BCD to Excess-3 code converter which is having nine (three input) majority gates, two inverter gates, in which combinedly includes 164 cells had been implemented and better simulation results are obtained by making use of QCA designer tool.**

Keywords— Quantum dot, Quantum-dot Cellular Automata, Complementary metal-oxide semiconductor, Binary coded decimal, Nano-scale, QCA designer tool.

I. INTRODUCTION

In the past few decades, complementary metal oxide semiconductor (CMOS) is consistently played a vital role in digital designs for achieving the important parameters like implementing high density, high speed and low power consumption in very large scale integrated systems. In general, the CMOS technologies are better to scaling the size and it supports the integration. However, many studies have been predicted that these technologies are fulfilling the fundamental physical limits, but the current technologies are facing more challenging problems. Quantum dot Cellular Automata (QCA) [6] [10] is the better alternatives. Quantum dot Cellular Automata were introduced in 1993 by lent et al, and later experimentally rectified in 1997.

The QCA offers a new transistor-less computing paradigm in nanotechnologies. This phenomenon will set to achieve very high switching speeds, extremely low power consumption, high switching speeds. QCA [4] structures are constructed as an array of quantum cells within which every cell has an electrostatic interaction with its neighboring cells. QCA applies a new way of computation, where polarization rather than the electric current, contains digital information. In this fashion, instead of interconnecting the wires, the Quantum cells have to transfer the digital information throughout the circuit. The basic logic elements used in this technology are the three input majority gates, inverter gates, and basic logic gates etc., the other logic structures are designed by using these basic elements.

The paper is organized as follows in section 2, describes QCA Overview, and in section 3, provides the efficient design of BCD to Excess-3 code converter. In section 4 represents simulation results followed by observations in section 5. In section 6, is conclusion and followed by Acknowledgement.

II. QCA OVERVIEW

A high-level [3] diagram of a four-dot QCA cell appears in four quantum dots is positioned to form a square. Exactly two mobile electrons are loaded in the cell and can move to different quantum dots in the QCA cell by means of electron tunneling. Tunneling paths are represented by the lines connecting the quantum dots in Columbic repulsion will cause the electrons to occupy only the corners of the QCA cell resulting in two specification polarizations. For an isolated cell there are two energetically minimal equivalent arrangements of the two electrons in the QCA cell, denoted cell polarization P= +1 and cell polarization P= -1. Cell polarization P= +1 represents a binary 1 while cell polarization P= -1 represents a binary 0.
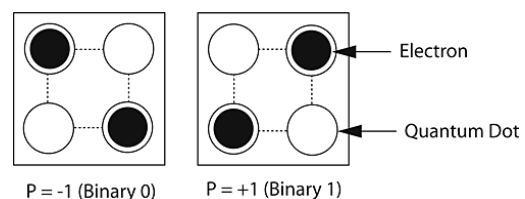

Fig -1: QCA cell polarization

1. QCA Devices

In a QCA wire, the way of transfer the binary information from source end to destination end just by means of electrostatic interactions between the cells. The propagation in a 90 degree wire is shown in Fig.2.Another one is 45 degree wire is as shown in Fig.3
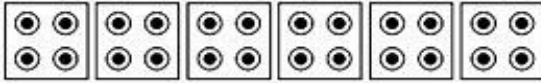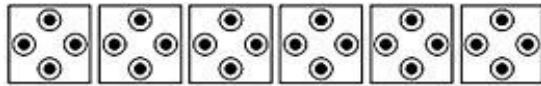

Fig -2: 90 degree QCA wire

Fig -3: 45 degree QCA wire

2. QCA Inverter Gate

And the inverter logic gate [9] arrangements are two different types in QCA. In that, commonly used inverter is shown in Fig.4a. Another one is larger robust inverter is shown in Fig.4b
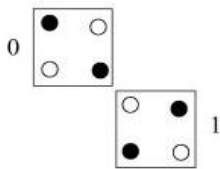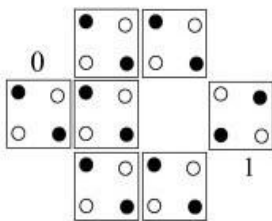

Fig -4a: Simpler two cell inverter

Fig -4b: Larger robust inverter

3. QCA Majority Gate

The fundamental QCA [7] [1] logic device, a three input-majority gate, is shown in Fig.5 from which more complex circuits can be built. In QCA, a three input majority gate consist five cells in that, three cells are meant for inputs and one cell is for output and the centered cell is polarized by as per the given inputs.

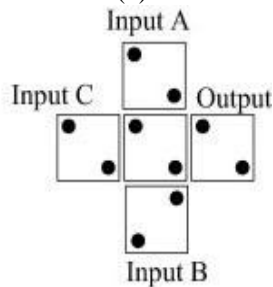$$M (A, B, C) = AB + BC + CA - (1)$$

Fig -5: Three input majority gate

Even though, a five input majority gate is also available in this QCA, the structure is shown in Fig.6. May this five input majority gate is mainly used to build complex sequential circuits.
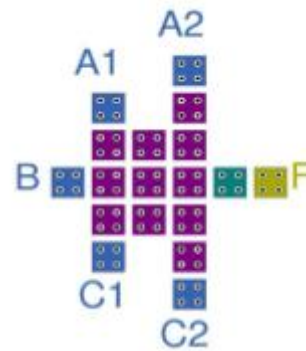

Fig -6: Five input majority gate

4. QCA Clocking

The QCA circuits require a clocking, not only for synchronization and control the flow of information but also to provide the power to run the circuit since there is no external way to provide the power to the cells. Here we are using four level clocking scheme, the propagation modes are represents as shown in Fig.7. This [6] clocking method makes the design of QCA is different from CMOS methodology. In the below figure we can observe that, for any zone clock cycle is having four stages which are framed as Switch, Hold, Release, Relax. Each clock cycle is going to start at their time slots. So, we can say that some lesser delay will be having between different clock cycles.
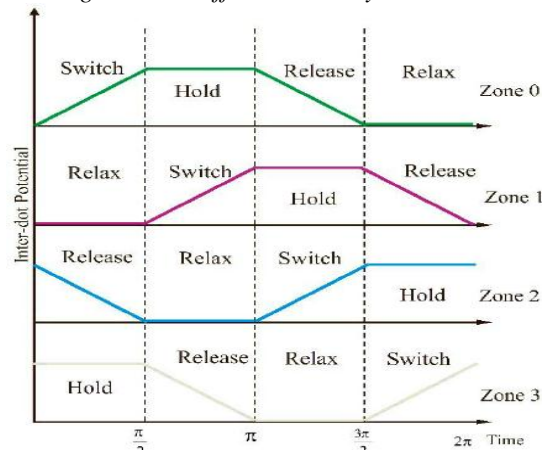

Fig -7: The four stages of QCA clock

5. QCA Designer Tool

QCA Designer tool [5] is capable of simulating complex QCA circuits to make more standard. After the circuit was designed in terms of majority gate and NOT gates we need a simulator to simulate the results based on the layout and inputs given to the logic circuits. The most popular simulator used for designing circuits in Quantum-dot Cellular Automata is QCA Designer which is an open source free tool to download. After building the layout in the QCA Designer the layout can be saved and results will be displayed in the form of graphs

QCA Designer is the simulation tool used for efficient simulation of QCA circuits. In order to understand the process of working in QCA Designer some of the key features and the functionalities of this simulator must be studied

III. EFFICIENT DESIGN OF BCD TO EXCESS-3

In a BCD to Excess-3 code converter it consists of nine possible combinations of BCD inputs namely B0, B1, B2 and B3 respectively. And the output of the design gives the Excess-3 code namely X1, X2, X3 and X4 respectively. The truth table is depicted in Fig.8. And the circuit diagram of the BCD to Excess-3 code converter is as shown in Fig.9 and the output logic functions in equations (2, 3, 4 & 5)

$$X4 = B3 + B2\,(B1 + B0) - (2)$$
$$X3 = B2\ \text{XOR}\ (B1 + B0) - (3)$$
$$X2 = B1\ \text{XNOR}\ B0 - (4)$$
$$X1 = \text{NOT}\ B0 - (5)$$

Decimal	BCD B3 B2 B1 B0	Excess-3 X4 X3 X2 X1
0	0 0 0 0	0 0 1 1
1	0 0 0 1	0 1 0 0
2	0 0 1 0	0 1 0 1
3	0 0 1 1	0 1 1 0
4	0 1 0 0	0 1 1 1
5	0 1 0 1	1 0 0 0
6	0 1 1 0	1 0 0 1
7	0 1 1 1	1 0 1 0
8	1 0 0 0	1 0 1 1
9	1 0 0 1	1 1 0 0

Fig -8: Truth table

The combinations of input 1010, 1011, 1100, 1101, 1110, 1111 are invalid BCD they treated as don't cares.
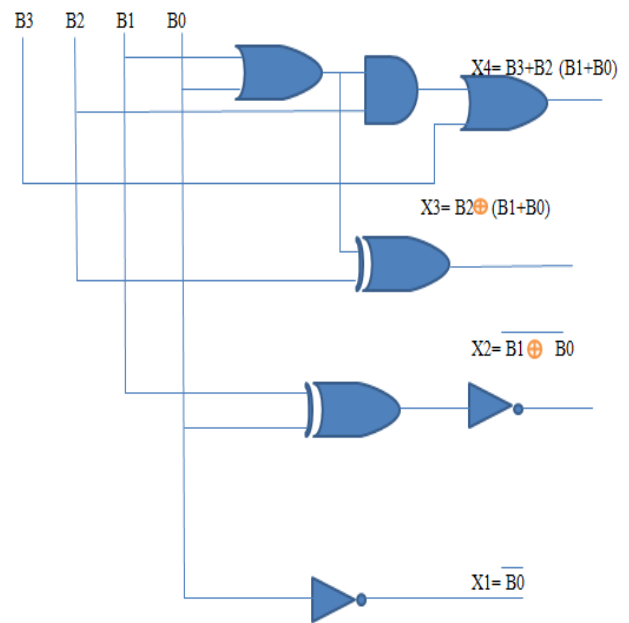

Fig -9: Circuit diagram

IV. SIMULATION RESULTS

These simulation results are obtained for An Efficient design approach of BCD to Excess-3 code converter using QCA is depicted in Fig.10. From the results, input B0 is giving as inverted output at X1 is depicted in Fig.11. The combination of two inputs B0 and B1 are giving as XNOR output at X2 is depicted in Fig.12.

The combination of B0, B1 and B2 are giving as XOR output at X3 is depicted in Fig.13. Similarly, all the inputs are combinedly doing relevant operations and get output at X4 is depicted in Fig.14.

From the figure-9, the BCD to Excess-3 code converter circuit diagram and their respective outputs are exactly simulated by using QCA designer tool. The goodness in this design is that no distortion occurs in the waveform simulations.
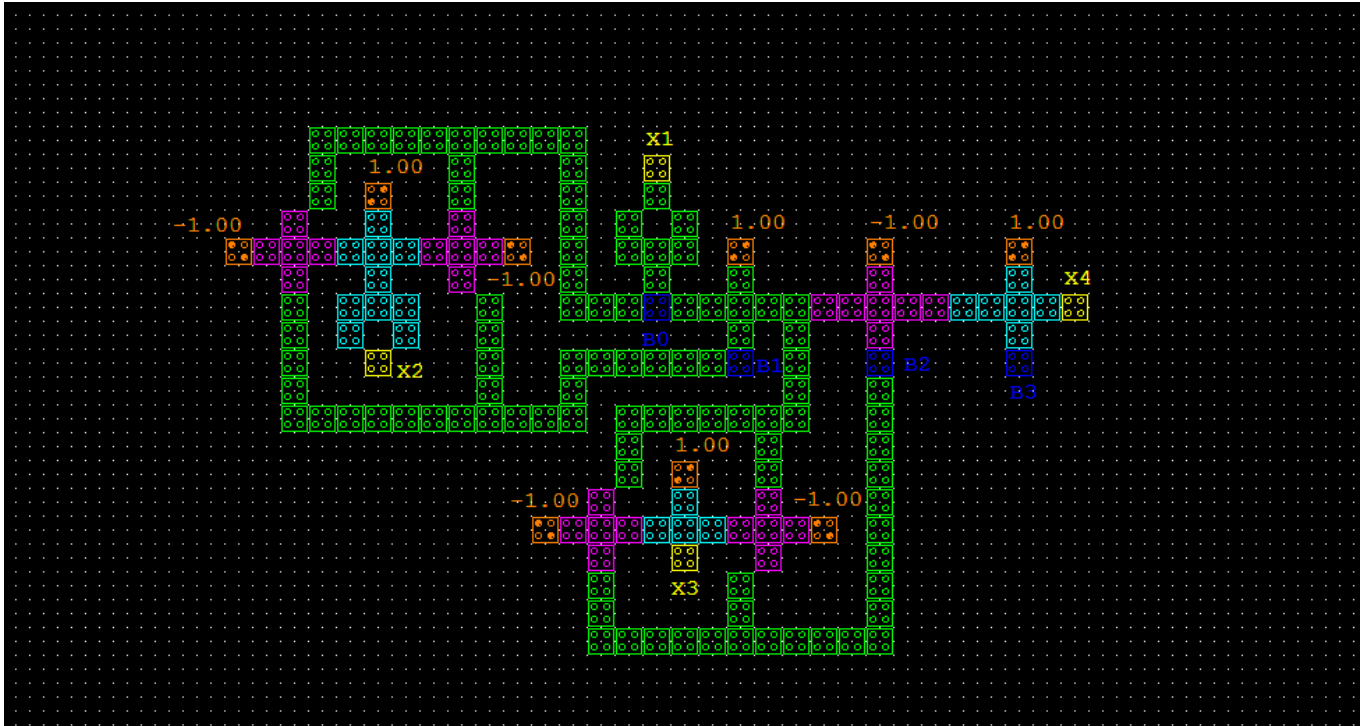
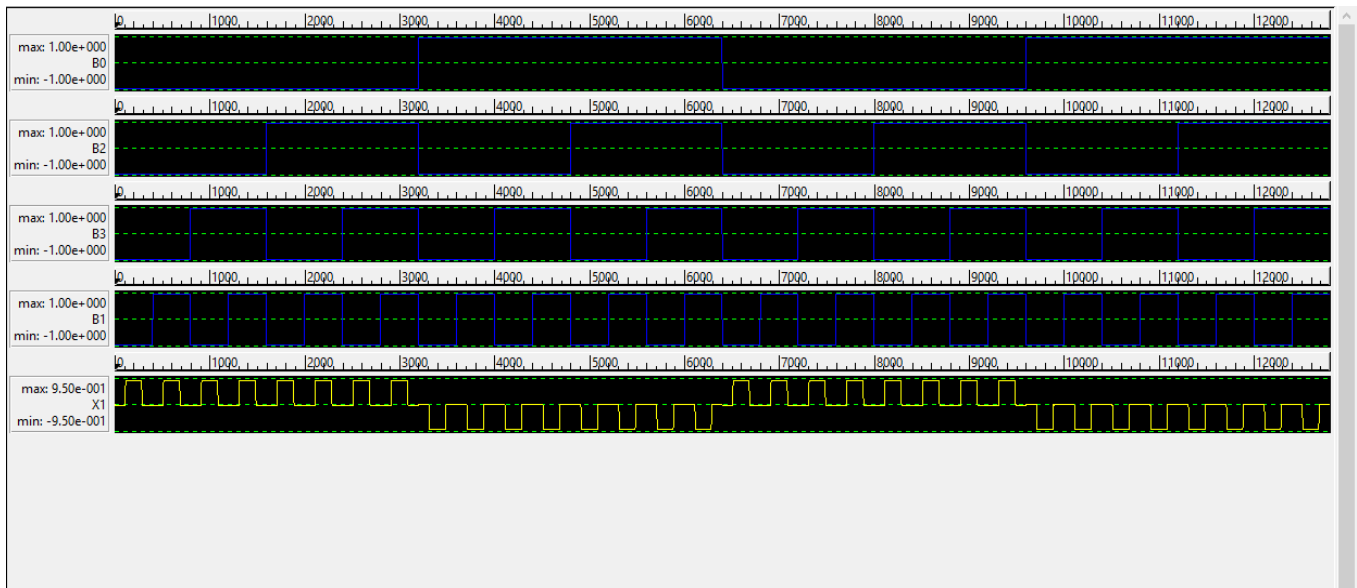Fig -10: An Efficient Design Approach of BCD to Excess-3 Code Converter

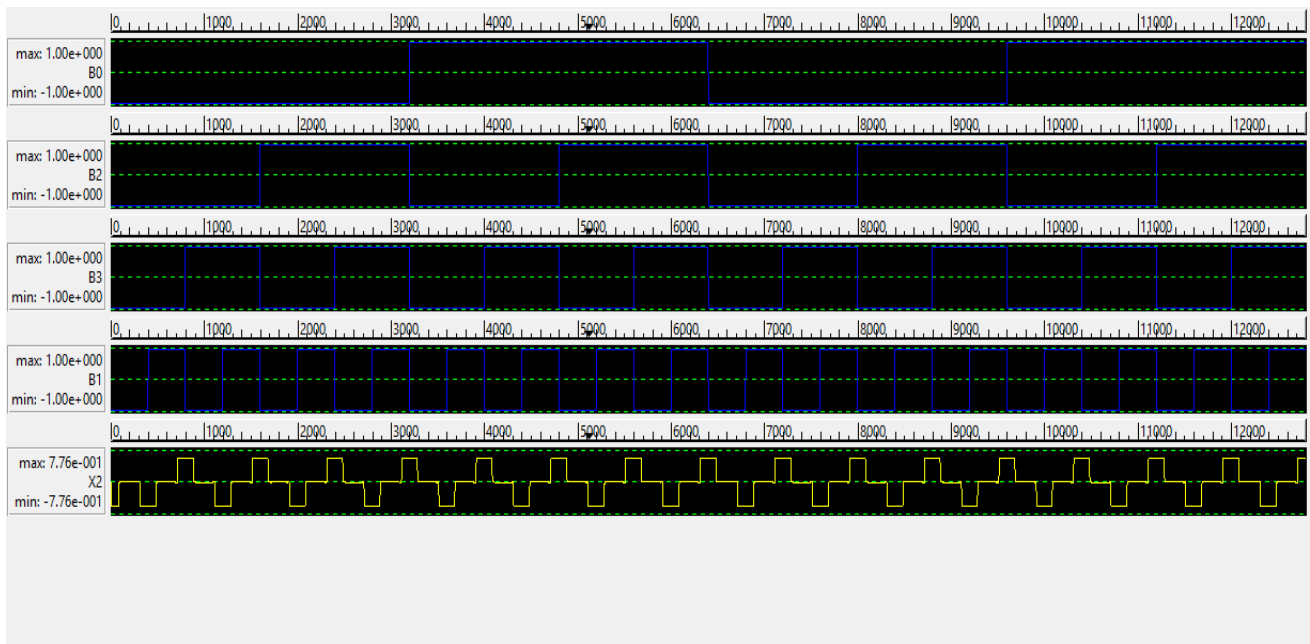Fig -11: Simulation Results of Output X1
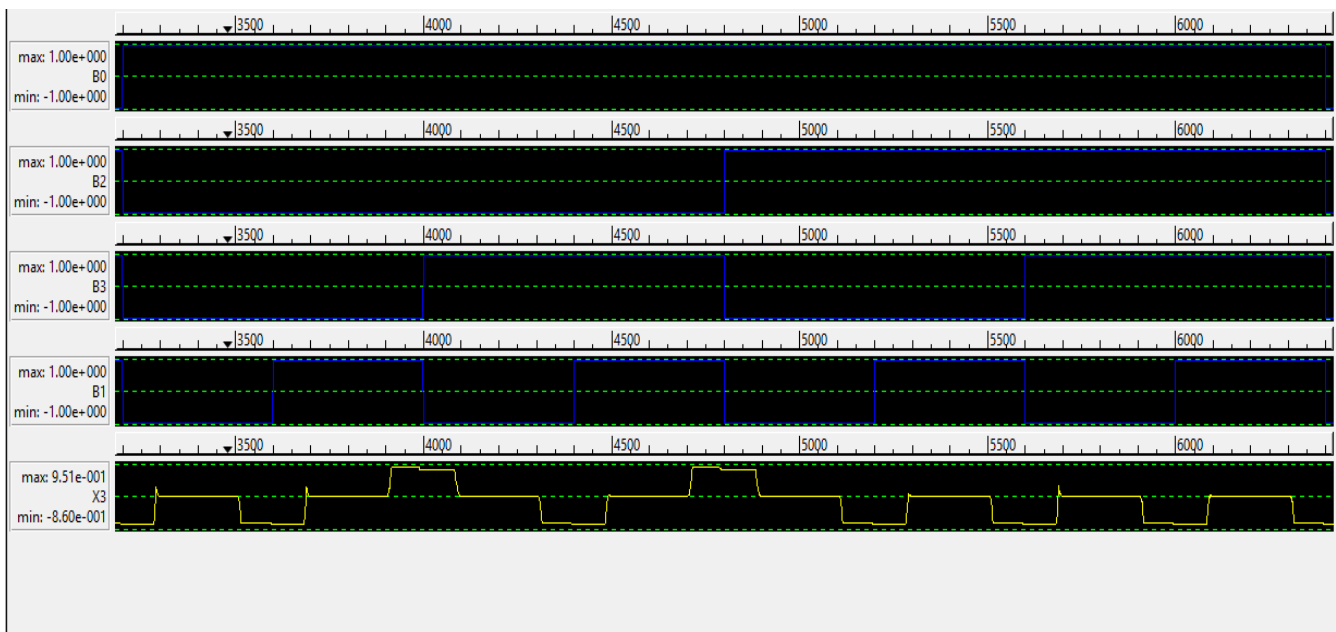
Fig -12: Simulation Results of Output X2
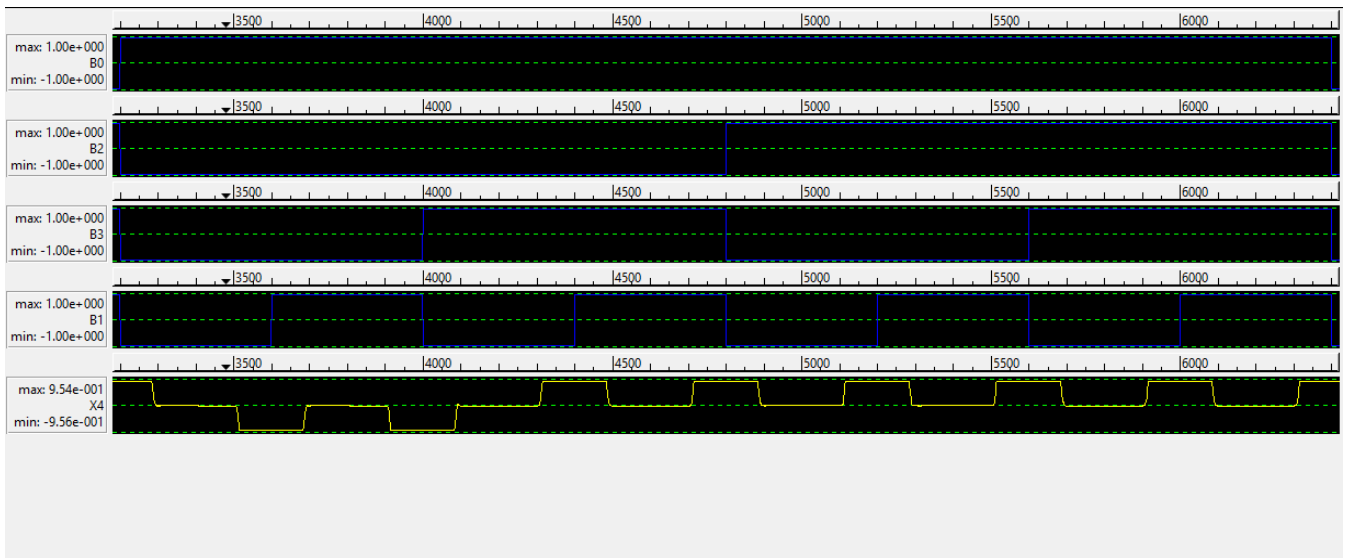

Fig -13: Simulation Results of Output X3

Fig -14: Simulation Results of Output X4

V. OBSERVATIONS

Thus we can confirm that the proposed design functionality matches with the original functionality of the circuit diagram. The scope of this project is to compare the proposed BCD to Ecess-3 code converter with its CMOS counterpart in terms of the area occupied and power consumption and finally we have to arrive at a conclusion. The proposed QCA of an efficient design approach of BCD to Excess-3 code converter consists of 164 quantum cells and the area occupied by these cells in the design of BCD to Excess-3 code converter is approximately 0.252984.00 Sq. Microns. (i.e. 0.25 μm^2). If you consider the CMOS counterpart for this BCD to Excess-3 code converter it consists of a AND gate, two OR gates, two Ex-or gates, and two NOT gates. Along with this there will be interconnects that consumes lot of area. In a simple, AND gate there will be many transistors along with interconnects. So this will increase the area by a large factor. While coming to the power consumption, the excitation used in the CMOS logic varies from 5-12 volts and also interconnects made by copper and current physically travels from one device to other in case of CMOS. The current in inter connects leads to very high power dissipation and thus the devices become more power hungry. The All designs are carefully clocked and were functionally verified using QCA Designer; a layout and simulation tool for QCA. Finally, in Table -1, designs are compared according to number of cells, area, and delay.

Parameter	Value
Number of cells	164
Covered area (μm^2)	0.25
Time delay (clock cycle)	1

Table -1: Result Analysis of Proposed design

VI. CONCLUSION

A project on An Efficient Design Approach of BCD to Excess-3 Code Converter using QCA have been realized effectively and tested by QCA Designer Tool. In this project we have discussed the basic concepts of the quantum dot cellular automata and discussed the core component of the simulation QCA Designer Tool. By these basic layouts further complicated layouts can be designed with less number of cells and area comparatively. The operation of the structures has been verified according to the circuit diagram. This design works efficiently and produces required results.

VII. ACKNOWLEDGEMENT

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