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An Efficient Method to Implement Optimized Adder in ALU

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***Abstract*-Carry select Adder (CSLA) is known to be the fastest adder among the other adder structures. This work uses an area efficient carry select adder by reducing redundant operations. The proposed CSLA method has been developed efficient gate level modification to significantly reduce the area, Power and delay. In the existing adder system, the multiplexer is used to select the exact output according to the logic states of carry-in signal. In the proposed work, the redundant operations are reduced by optimizing the selection unit and this proposed adder is implemented in Arithmetic and Logic Unit(ALU). The result analysis shows that the proposed architecture achieves the three folded advantages in terms of area, power and delay.**

Keywords—Carry select adder, Redundant operations, Area efficient,gate level modification ,Arithmetic and Logic Unit.

I INTRODUCTION:

VLSI is the process of Integrating thousands of transistors (1000 to 100000) into a single chip for the purpose of creating Integrated circuits. This high level integration will lead to fewer packages and interconnections and also beneficial effect on cost and reliability of the system.

This is the field which involves packaging more number of logic devices into smaller areas [2]. In this rapidly growing technology and scaling of devices not only faster but also smaller and low power circuits are demanded.

There is more number of research going on to reduce the consumption of power in VLSI circuits.Over the past several years, silicon CMOS technology has become the dominant fabrication process for relatively high performance and cost effective VLSI circuits.In electronics, adder is a common digital circuit that performs addition operation[2]. Adders are used in computer for adding data in the processor. There are various electronic applications of adders such as digital signal processing to perform various algorithm like FIR, IIR etc.An arithmetic logic units(ALU) acts as a heart of the central processing unit of a computer. It consists of electronic components which are used to perform arithmetic and logic operations.

The challenge of VLSI designer is to reduce the size of the chip by using efficient optimization techniques. Then the second phase is to decrease the delay of operation to achieve fast calculation. There are three performance parameters on which a VLSI designer has to concentrate i.e., Area, delay, power. An efficient adder design improves the performance of the complex system[1].

In general ripple carry adder(RCA) uses a simple design but suffers from a long carry propagation time.Carry look ahead adder(CLA)gives fast design compared to RCA is used in several applications that consider area, delay and power.

In the carry select adder the N bits adder is partitioned into M equal parts. Each part of adder consists of two ripple carry adders with cin=0 and cin=1, respectively. In this paper, we proposed an area efficient adder by reducing redundant operation using optimized CSLA.

The existing adder system is introduced in section 2; in section 3, proposed CSA architecture is discussed. In section4 simulated results and comparison of proposed with other conventional CSLA are discussed. Finally this paper ends with conclusion.

II EXISTING ADDER SYSTEMS

A. Conventional CSLA

The carry select adder in general consists of two ripple carry adder and two multiplexers. The two blocks of ripple carry adders are used to perform the calculation twice, one with the assumption of carry being zero and other assuming one. The resultant sum is then selected with the multiplexer once the current carry is known. The circuit diagram of (full adder) conventional CSLA is shown in fig. 1.The logic operation of ripple carry address is performed in four stages such as

1.Half sum generation (HSG)
2. Half carry generation (HSG)
3. Full sum generation (FSG)
4. Full carry generation.

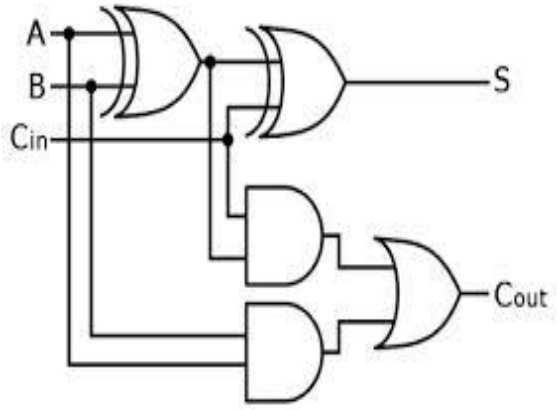

Fig.1. Full adder circuit.

The AOI (And, or, Inverter) Implementation of EXOR gate is shown in fig.2

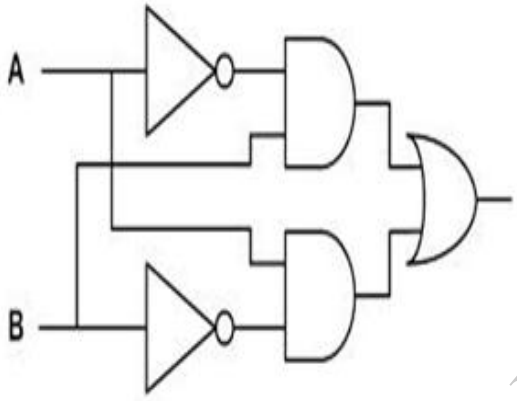

Fig.2.AOI Implementation of EXOR.

Similarly the AOI implementation of 2:1 Multiplexer is shown in fig.3

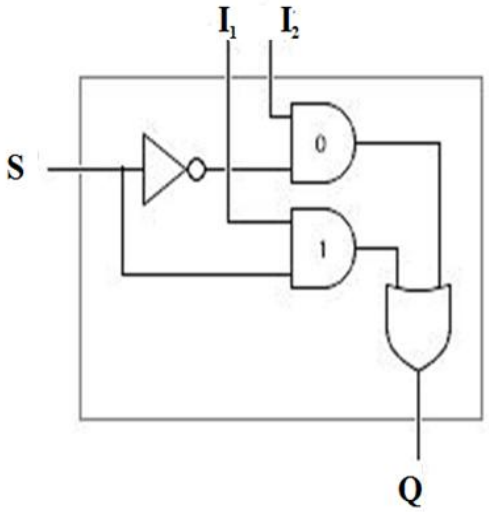

Fig.3. AOI Implementation of Multiplexer.

In8 bit conventional CSLA, the number of gates present in the circuit is calculated as follows.
One half adder
15 full adders
16 multipliers
TOTAL NO. OF GATES= 265
The AOI implementation of half adder and full adder is shown in fig.4 and fig.5.

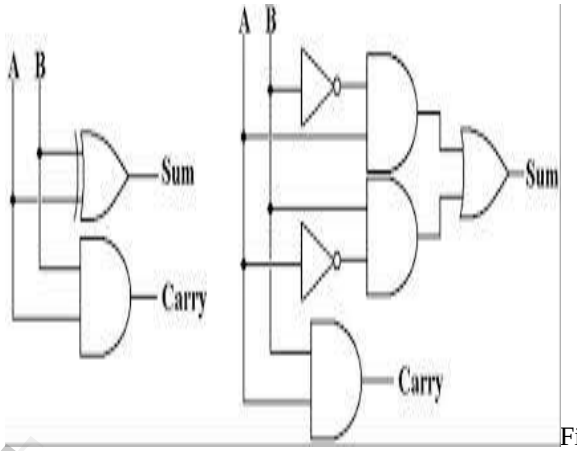

Fig.4. AOI Implementation of Half Adder.

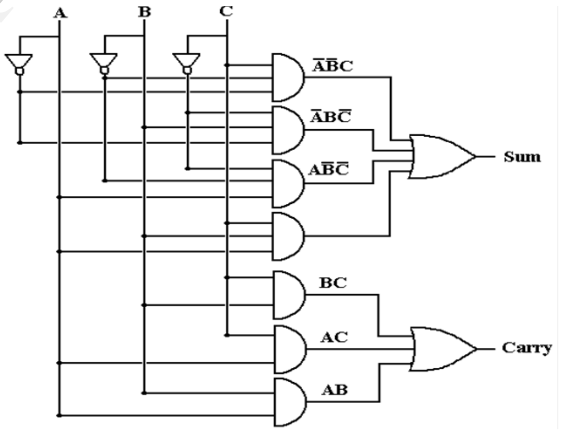

Fig.5.AOI Implementation of Full Adder.

B. BEC based CSLA

The BEC based CSLA has one block of ripple carry adder with binary to excess one converter, which replace the other block of ripple carry adder having cin=1. The multiplexer is used to select either the BEC output or the direct inputs according to the control signalcin. The circuit diagram for BEC based CSLA is shown in fig.6.
Comparing the conventional with BEC based CSLA, it is clear that BEC based CSLA reduces the area and power.

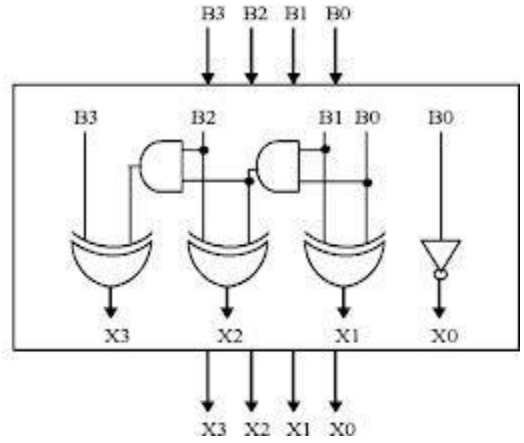

Fig.6. BEC-based CSLA.

But the disadvantage is that the delayis increasing than the conventional CSLA.

The Boolean expressions of the 4-bit BECis listed as (note the functional symbols - NOT,& AND,^ XOR)

X0 = - B0
X1 = B0^B1
X2 = B2^(B0 & B1)
X3 = B3^(B0 & B1 &B2)

The number of gates in 4 bit BEC based CSLA is reduced comparing to conventional CSLA which is calculated below.

One half adder
7 full adders
9 multipliers
7 EXOR and AND gates
One NOT gate

TOTAL NO. OF GATES= 176

C.COMMON BOOLEAN LOGIC

In CBL method , an area efficient CSLA is achieved by sharing common Boolean logic term to remove the duplicated adder cells present in the conventional carry select adder. The reduced transistor counts and low power is achieved using CBL method.

The sum is obtained by using XOR & NOT gate and the carry is obtained by using AND ,OR gate .The sum generation by sharing common Boolean logic term is illustrated in fig.7.

Once the carry in signal is ready ,then the multiplexer is used to select the correct carry output depending on the logic state of carry in signal.

As compared with BEC based CSLA, this CBL method has reduced area but the speed or carry propagation delay is nearly equal to the conventional CSLA.

The number of gates used in the 8 bit CBL based CSLA is calculated as

AND gates=56
OR gates=32
NOT gates=40
TOTAL NO. OF GATES= 128

III. PROPOSED CSLA

The speed in the CBL based CSLA is nearly equal to the conventional CSLA. To increase the speed, optimization of logic units is to be carried out.

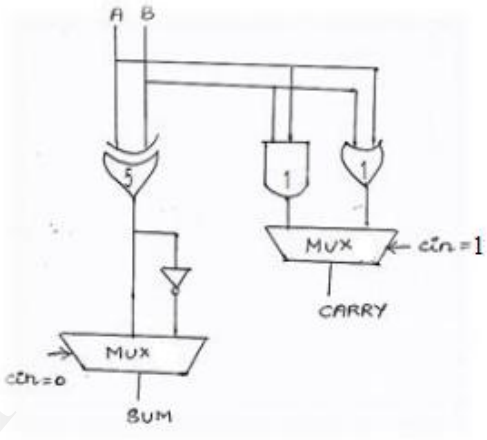

Fig.7.CBL-based CSLA.

In proposed CSLA method,CSLAhas two units.

(1) Sum and carry generator unit (SCG)

(2) Sum and carry selection unit (SCS)

Most of the logic resources of CSLA is consumed by the SCG unit .For efficient implementation ofSCG unit different logic designs have been suggested .Using this method one can have the advantages of

(1) The n bit select unit is required instead of the (n+1) bit.

(2) The small output carry delay.

These features results in an area-delay-power efficient design for CSLA.

The calculation for the number of gates present in the 8 bit ADP efficient proposed CSLA is as follows.

AND gates=48
OR gates=24
NOT gates=32
TOTAL NO. OF GATES=104.

A.comparison of existing and proposed adder system for 8-bit.

CSLA	CONV	BEC	CBL	PROP
Gates	256	176	128	104
Area (μm²)	1438.1	1282	906.5	951.2

Table.1.output comparison.

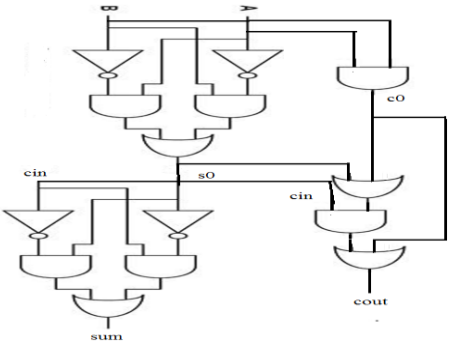

Fig.8.Proposed circuit Design

As compared with CBL method, this method involves significantly less area and delay which is shown in fig.8.

IV. SIMULATION AND RESULTS

The proposed CSLA achieves an outstanding performance in power consumption .power consumption can be reduced in our proposed CSLA because we need only two EXOR gates for summation operation as well as two AND gates and two OR gates for carry-out operation. We also simulated the proposed consumption in the proposed adder in 0.18μm CMOS technology. The power consumption can also be saved through the removal of redundant logic operations .The circuit were simulated using XILINX ISE design suite 12.1 and implemented in VHDL language. The area consumed by the circuit depends only on the gate counts.

By reducing the number of gates in the circuit ,the area of the circuit can be reduced. Hence the computational speed is increased by minimizing the area of the circuit.

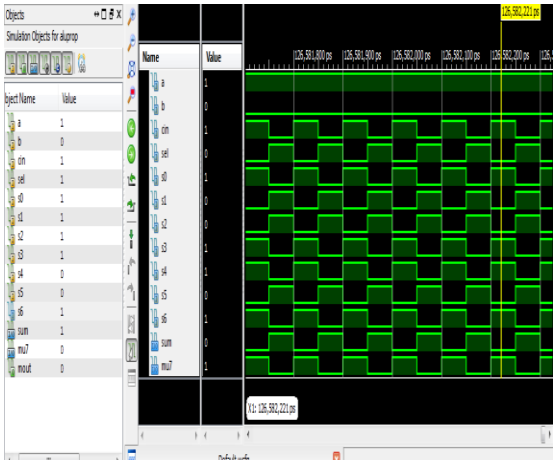

Fig.9. proposed ALU

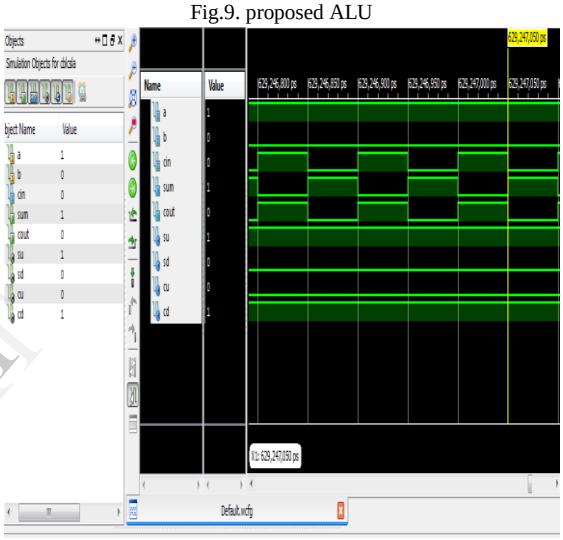

Fig.10. logic output of proposed ALU

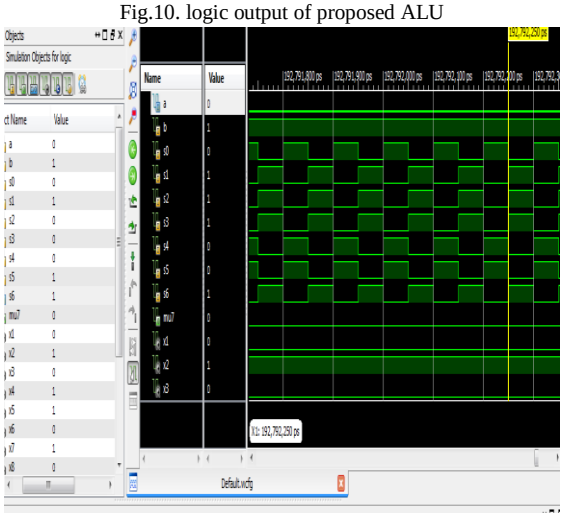

Fig.11.Proposed CSLA

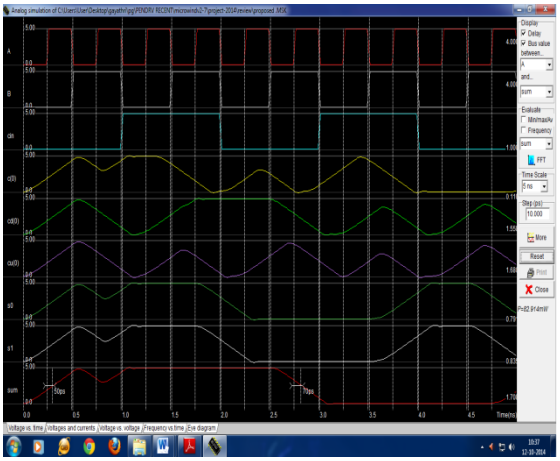

Fig.12.Power dissipation of proposed CSLA

V. CONCLUSION

We have analysed the existing CSLAs to study the data dependence and the redundant logic operation. The redundant logic operations involved in existing CSLAs are eliminated. The scheduling of carry selection operation is carried out before the final-sum calculation. The specific bit pattern for carry generation is used for logic optimization of carry selection unit. The carry generation unit with fixed input bits are also used for logic optimization of the circuit. The reduced number of gates offered the great advantage in reduction of area, power and delay. The proposed architecture with low power ,low area and low delay is efficient for VLSI hardware implementation.The efficient design for the proposed CSLA is obtained by using optimized logic units.The proposed CSLA consumes 50% less energy than the existing (CBL-based) CSLA ,for different bit-widths.

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