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An Implementation of a WiMAX based Digital Down Converter

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***Abstract*—A Digital Down Converter is an important front end signal processing unit in any communication system. It converts intermediate frequency to baseband by scaling down the sampling frequency of the signal. In this paper, an area and power efficient architecture for the DDC has been described and is realized on a Spartan 3e FPGA.**

***Keywords—DDC, NCO, CORDIC, Unfolded FIR architecture, Folded FIR architecture, FPGA*.**

I. INTRODUCTION

Over the past two decades, a huge advancement in the field of technology has been witnessed due to the constant need of efficiency. Many attempts have been made to help a common man to improve his lifestyle [1], [2]. Numerous contributions have been made to aid the physically challenged through developing fast algorithms to commute and communicate. Researchers all around the world have contributed to this growth by either enhancing the algorithms [3], [4], [5] involved or by improvising the architecture concerned to the hardware [6], [7], [8]. One of the most recent contributions to the mankind is the introduction of 4G systems. 4G systems are gaining limelight due to its high speeds and high data rates. Along with the series of advantages, 4G systems' major drawbacks are high area and power consumption. Thus, in order to overcome these shortcomings, several architectures for different components of the 4G systems have been proposed.

Worldwide Interoperability for Microwave Access (WiMAX) belongs to the family of 4G standards. The main units of the communication unit are the radio frequency section, the intermediate frequency section and the baseband section. The unit which converts digitized intermediate frequencies to baseband frequencies is known as a Digital Down Converter [9].

A digital down converter consists of 3 sections: a numerically controlled oscillator (NCO), mixers and series of decimating FIR filters. NCO generates sine samples, which are multiplied with the incoming IF signal. The output of the mixer is then fed to a chain of decimating filters, to reduce the sampling rate of the signal as well as to filter out the spectral replications obtained during multiplication of incoming and carrier signals to attain baseband spectrum of interest [10].

The DDC works at high frequencies. It is a well known fact that the power consumption of any system is directly proportional to its working frequency. Since, the working frequency of the DDC of WiMAX systems id very high, the power consumption is proportionally high. Thus, in this paper, an approach for reducing the power consumption of the DDC Unit has been summarized.

The paper has been divided into six sections. Section 2 deals with approaches explained by several papers and journals for improvised DDC circuitry. Section 3 deals with architecture of DDC. Section 4 discusses about the implementation. Section 5 sums up the results. The conclusion of the paper has been mentioned in Section 6.

II. EXISTING METHODS

Numerous proposals have been placed in front of the world to deal with the inefficiency of the DDC architecture. A few of them have been mentioned in this section.

According to [11], a single stage implementation of decimation filter produces high computational complexity and the power consumption is also high. Thus as a solution to this problem, a multistage implementation approach for the same is suggested.

[12] deals with the performance of NCO and the filters. CIC filters are used here as the decimating filters. A direct digital frequency synthesizer (DDS) is implemented as the NCO, which produces a signal with a specified frequency and phase (adjustable at run time). It has been also specified in the work that the CIC filters often include the re-samplers that interpolate or decimate the signal to achieve desired sample rate, depending upon the application.

The authors in [13] discuss an efficient method of designing wideband DDC, which is used in the application where confidential data is to be transmitted. In the DDC design, a variable decimation is implemented in order to extract the actual signal from the received band of signals and multistage filtering is employed to obtain an efficient response. The CIC filter is taken into consideration in their research as this filter has the ability to achieve high decimation factor and also it can be used for high speed application. This design was implemented on an FPGA.

In the paper [14], the authors have explained the DDC application in RADAR Communication. In RADAR systems, once the reflected RADAR signal is obtained by the receiver, it has to be pre-processed by the DDC and later the signal should be fed to the signal processing stage. The author has elucidated a way to control the working of DDC through commands over ETHERNET LAN. Also, the author has implemented an optimized architecture with respect to power dissipation, speed and complexity of the DDC architecture on an FPGA.

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In [15], the DDC implemented on the FPGA is compared with the traditional ASIC DDC device. The paper states that the DDC implemented on FPGA has more flexible frequency and phase characteristics and higher precision computation. The main feature of the DDC designed in the paper is that the DDC utilizes two clock scopes and has a

FIFO interface. That is, the data from DDC module is transferred to a FIFO, which plays a role of forming the new data flow and sending them to the next processing unit. And the benefit of the DDC is efficiency in terms of resource consumption. Finally a flexible, programmable and high-efficiency architecture of DDC is implemented on Xilinx FPGA SX95T.

The paper [16] introduces a digital IF module, which is applied to a Broadband Wireless Ad hoc Network (BWANET) system. Its main function is to carry out bit rate conversion and spectrum shifting. The IF module consists of DDC. The filter design is one of the key factors in improvising the efficiency of the unit. A multistage signal filtering DDC is utilized in the paper. After a comparative analysis, this paper presents an IF filter structure which requires minimum hardware resource usage. The IF module introduced in this paper consists of a down conversion mixer and a decimation filter. The down-conversion mixer can be realized easily by using the IP Core in Xilinx ISE, thus this section puts the emphasis on the design and implementation of the filter architecture. The test result indicates that the IF module has advantages of low distortion, good orthogonality and amplitude coincidence of I/Q data. It also can be used in other similar systems by changing several parameters in mixer and filters.

The authors of [17] propose a programmable digital up and down converter (DUC and DDC) structure, which can be used in digital transmitters and receivers that meet IEEE 802.16d standard in wireless communication system. The structure is based on the idea of software radio technology and the theorem of multi-rate signal processing. The SignalMaster40000-lspsmquadc6713 (QC6713) is employed to implement the DDC.

In [18], the DDC application at the Wideband Radar Receiver has been explained. In a conventional radar receiver, errors are introduced due to mismatch between the ADCs and gain and the phase mismatch in the I/Q demodulation. By performing I/Q demodulation in the digital domain some of these errors can be lessened. Three filter structures suitable for digital I/Q demodulation are evaluated in this paper. The first case uses FIR filters for both stages. For the second case, an FIR filter is considered for the Hilbert transform and bi-reciprocal LWDF is used for the high pass filter. Finally, for the third case, bi-reciprocal LWDFs are considered for both stages. For all three cases the data word length is 12 bit. The results from the logic synthesis give that the FIR-WDF case is the most efficient for implementation

III. ARCHITECTURE OF DIGITAL DOWN CONVERTER

The block diagram of the existing architecture of the DDC is shown in Fig.1.

The IF signal sampled at f_s is multiplied with the sine waveform of carrier frequency f_c. The product results in a sum component ($fc + f_r$) and a difference component ($fc - f_r$), where f_r is the frequency of the received signal. The difference component is retained and the rest of the signal replications are filtered out. This is attained with the help of a 35 tap FIR. The filtered signal is then decimated by 4, which results in a distorted signal. This signal is further filtered using a 63 tap FIR filter to smoothen the signal. This signal is then decimated by 2 and a smoothening filter of 111 coefficients is employed to get distortion free signal. The signal obtained after filtering with 111 tap filter has to be fed to the next stage of the receiver system.

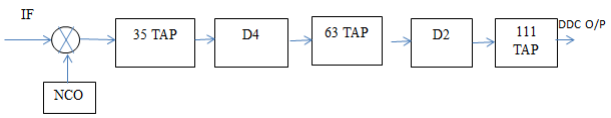

Fig. 1. DDC Architecture

The NCO is the unit that generates the carrier signal that has to be multiplied with the incoming signal. The Look Up Table approach is one of the most commonly used approaches for developing NCOs. It is preferred mostly for its high speed. In this approach the sampling frequency values are stored in prior and can be accessed when required. In spite of its high speed, the LUT approach falls short in terms of memory. In case of huge frequency as in case of WiMAX, large sampling frequency is obtained and hence large areas are to be allocated accordingly. LUT method usually stores values in terms of Sample or Hold Circuit.

Another major drawback of the LUT approach is that all the values of to be pre-calculated for the given frequency specifications and stored. This can pose a hitch, if the frequencies change. Thus, there arises a need to utilize an NCO, which can be adaptive with respect to the changes on frequencies. This can be achieved by incorporating the CORDIC algorithm for sine wave generation.

The CORDIC (COordinate Rotation DIgital Computer) algorithm also known as Volder's algorithm, is a set of iterative equations mentioned below that uses vector rotation to compute the trigonometric functions by using shift and add technique. The iterative equations have been mentioned below as equations (1), (2) and (3).

$$\alpha_{k+1}=\alpha_k-\beta_k*d_k*2^{-k} \quad (1)$$

$$\beta_{k+1}=\beta_k+\alpha_k*d_k*2^{-k} \quad (2)$$

$$z_{k+1}=z_k-d_k*\tan^{-1}(2^{-k}) \quad (3)$$

Here α_k and β_k indicate the value of sine and cosine values of k^{th} iteration respectively, z_k represent the angle of rotation and d_k indicates the direction of angle rotation, as shown in equation(4).

$$d=\begin{cases} 1 & \text{if } z>\delta \\ 0 & \text{otherwise} \end{cases} \quad (4)$$

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The final value of sine obtained from the iterations should be multiplied with a gain factor of 0.6073 to obtain correct values of sine for the given theta value.

The architecture FIR filter consists of multipliers, adders and D-Flipflops. An unfolded architecture with N coefficients requires N-1 delay units, N number of multipliers and N-1 adders. Fig.2 demonstrates the unfolded FIR architecture.

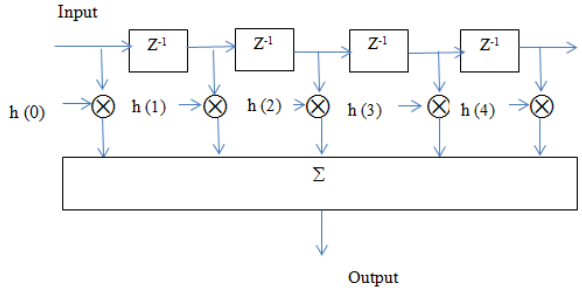

Fig. 2. Unfolded FIR filter architecture for 5 taps

The power and area consumption of a multiplier is very high. Since the Unfolded FIR Architecture requires a large number of multipliers, this architecture becomes infeasible with respect to efficiency.

The FIR coefficients are symmetric in nature. Using this property, only half the coefficients can be utilized, thus reducing the number of multipliers to just N/2. The power and area consumption by adder is negligible when compared to multiplier, and hence it can be said that both the parameters can be reduced by 50%. Figure 3 shows the folded FIR architecture.

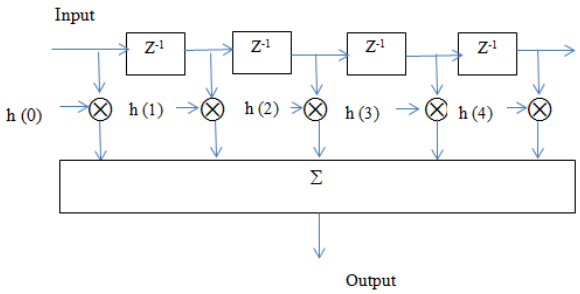

Fig. 3. Folded FIR filter architecture for 5 taps

IV. IMPLEMENTATION AND SPECIFICATIONS

In order to test the working of the architectures, a transmitter is implemented first. A signal of 200kHz, sampled at 11.2MHz is interpolated with a factor of 8, thus the sampling frequency increases to 11.2MHz x 8, which results in 89.6MHz. The up-sampled signal is then multiplied with a carrier of 2MHz, sampled at 89.6MHz. The product is then transmitted. Figure 4 illustrates the transmitter section.

A channel is created to add noise interference to the signal, which is received by the receiver.

The received IF signal is multiplied with the sine samples generated by an NCO. The CORDIC approach is applied for the NCO. The NCO generates samples of carrier frequency 2MHz and sampling frequency 89.6MHz. The product is then fed to a series of decimating FIR filters [9].

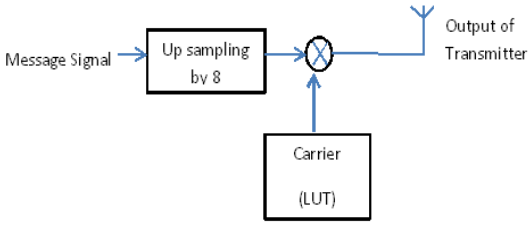

Fig. 4. 1 Block diagram of Transmitter Section

The first filter in the series is a 35tap FIR filter, whose pass band frequency is 5MHz, the stop band frequency is 15MHz, sampling frequency is 89.6MHz and the attenuation is -100dB. The magnitude response of the 35 tap filter is depicted in Fig 5.

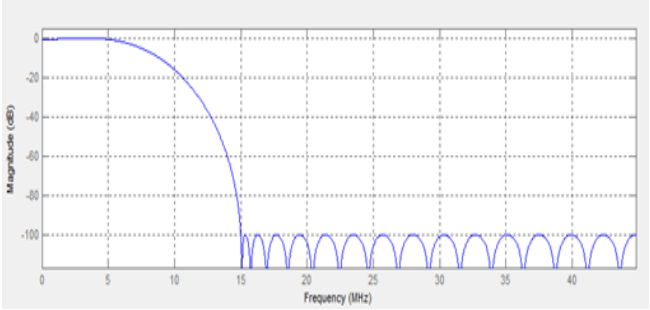

Fig. 5. Magnitude Response of 35 tap FIR filter

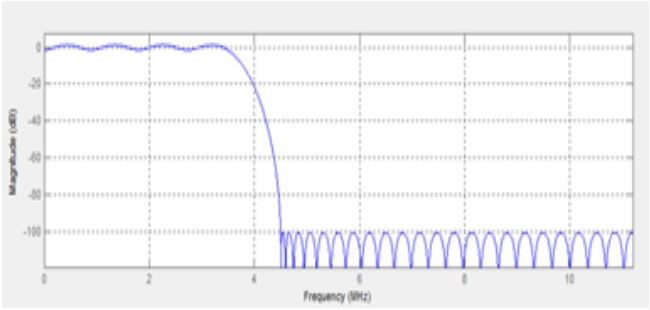

Fig. 6. Magnitude Response of 63 tap FIR filter

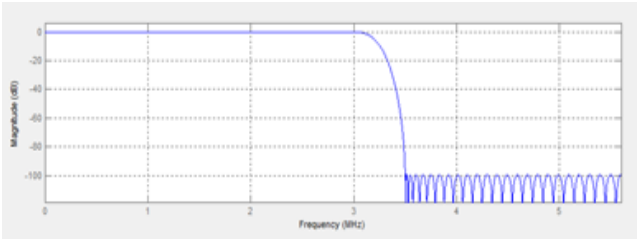

Fig. 7. Magnitude Response of 111 tap FIR filter

The filtered signal is then decimated by 4, which results in a distorted signal. This signal is further filtered using a 63 tap FIR filter to smoothen the signal. Its pass band and stop band frequencies are 3.5MHz and 4.5MHz, 22.4MHz sampling frequency and attenuation of -100dB. This signal is further decimated by 2 and a smoothening filter of 111 coefficients is employed to get distortion free signal. The frequency specifications of the filter are 3MHz pass band, 3.5MHz stop band, 11.2MHz sampling frequency and -100dB attenuation. The signal obtained after filtering with 111 tap filter has to be

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fed to the next stage of the receiver system. Fig 6 and Fig 7 indicate the magnitude response of the 63 tap filter and 111 tap filter respectively.

The output of FIR filter with 111 taps subjected to frequency response, as shown in Fig 8. The highest peak of the spectrum corresponds to the 200kHz frequency, which is the same as the message frequency transmitted. The highest peak is zoomed in as illustrated by Fig 9.

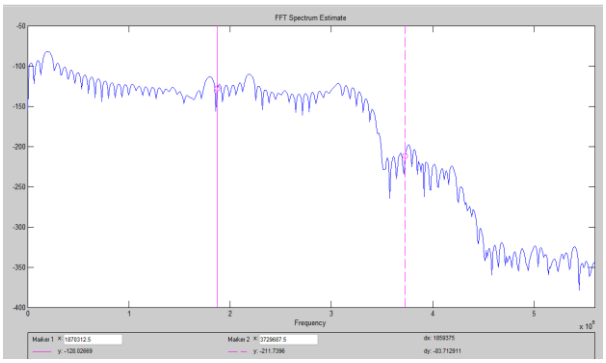

Fig. 8. Spectrum of Final DDC output

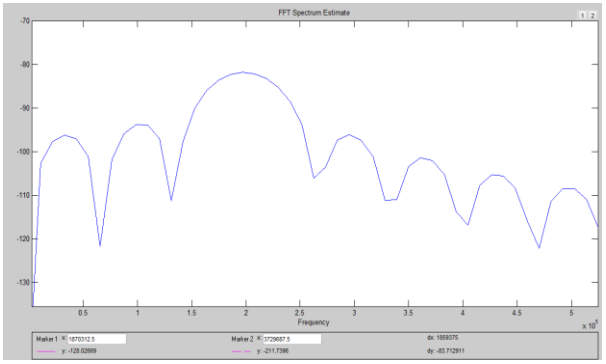

Fig. 9. Highest peak of the spectrum: Zoomed in

V. RESULTS

The above mentioned architectures are implemented on a Spartan 3E FPGA. The power and area comparisons of the same have been mentioned in the table below.

TABLE I. COMPARISON OF DIFFERENT APPROACHES

Architecture		Area	Power
Existing DDC	LUT based NCO	28%	52mW
	Unfolded FIR architecture	180%	80mW
Proposed DDC	CORDIC based NCO	23%	54mW
	Folded FIR architecture	31%	56mW

VI. CONCLUSION

As shown in the previous section, the combination of the CORDIC based NCO and the folded FIR architecture yields better results when compared to the combination of the LUT based NCO and the unfolded architecture. As mentioned in section 2, papers have explained that CIC filter implementation can also be looked into. But, the CIC filter requires and compensation filter. If the number of coefficients of the CIC filter is less, then the accuracy might not be good. Thus, to maintain the accuracy, the folded FIR architecture has to be used.

ACKNOWLEDGEMENT

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