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An Offset Cancelling Tri-State Sensing Latch with High Precision and Low Power Consumption for NAND Flash Memory Using SAPON Method

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- ***Abstract*—As NAND flash memory density increases, there is a significant need for high-precision and low-power sensing latches. The offset canceling sensing latch (OCSL) is a promising solution to enhance read precision by sampling and compensating for the trip voltage offset, thereby reducing the effective trip voltage variation. However, the OCSL encounters three main issues due to short-circuiting between VDD and GND: 1) increased energy consumption during the sense phase, 2) additional energy consumption during the sample phase, and 3) the potential for data corruption in the sample phase. This brief introduces the offset canceling tri-state sensing latch (OCTSL), designed to achieve high precision and low-power read operations with minimal die area overhead through three key innovations: 1) a sense phase without short-circuiting between VDD and GND by utilizing a tri-state sensing latch, 2) a sample phase without short-circuiting between VDD and GND through the addition of a sensing node pre charge, and 3) a couple-down phase that enables the use of the tri-state sensing latch via a sensing node coupling capacitor. Compared to the OCSL, the OCTSL reduces the effective trip voltage variation, lowers energy consumption during both the sample and sense phases, and eliminates the risk of data corruption in the sample phase, all with a slight increase in die area.**
- ***IndexTerms*—CMOS analog integrated circuits, flash memories, latches, low-noise sense amplifiers, offset cancelling, SAPON.**

I. INTRODUCTION

The "High-Precision and Low-Power Offset Canceling Tri-State Sensing Latch" in NAND flash memory is a design approach aimed at enhancing the accuracy and efficiency of reading data from NAND flash memory cells. This design aims to achieve precise reading of stored data by implementing an offset canceling mechanism, which compensates for any offset or error in the trip voltage, thereby reducing variations and improving the accuracy of the read operation.

Energy efficiency is prioritized by minimizing power consumption during the sensing and sampling phases of the read operation. This focus on low power consumption is crucial for improving the overall power efficiency of NAND flash memory, particularly as memory density increases. The use of a tri-state sensing latch in the design eliminates short circuits between the power supply (VDD) and ground (GND) during the sense phase, which contributes to reducing energy consumption and enhancing the precision of the read operation.

This approach is designed to achieve high precision in reading NAND flash memory while maintaining low power consumption. It employs an offset canceling technique and incorporates a tri-state sensing latch to address the challenges of accuracy and energy efficiency in NAND flash memory systems.

The page buffer is a critical circuit that powers the cell string and reads stored data by sensing a bit-line current (IBL) determined by the threshold voltage of the selected cell. In a conventional page buffer's read operation, there are four phases: bit-line precharge, sensing node precharge, develop, and sense. These phases involve actions such as connecting the bit-line, clamping with a bit-line clamp, and converting threshold voltage data. To prevent errors from coupling between bit-lines, the sensing node precharge phase charges the sensing node capacitor to VDD.

In the conventional page buffer, the sensing latch minimizes transistor count for efficient data storage but faces variations in intrinsic trip voltage (VTRIP). The conventional sensing latch, used in NAND flash memory, encounters challenges such as VTRIP variation, leading to imprecise sensing, especially with numerous page buffers. As word-line numbers increase and multi-level cell technology advances, the sensing latch size decreases, exacerbating VTH.CELL distribution issues.

The proposed Offset Canceling Tri-State Sensing Latch (OCTSL) addresses these concerns by introducing features such as a tri-state sensing latch in the sense phase to minimize VTRIP variation, a sample phase with sensing node precharge to reduce energy consumption and prevent data corruption, and a couple-down phase using a sensing node coupling capacitor to facilitate tri-state sensing latch adoption. These features ensure high precision and low power consumption. Moreover, by minimizing transistor count and addressing scalability concerns, the OCTSL design represents a significant advancement in achieving precise data reading and low power consumption in NAND flash memory systems.

II. LITERATURE REVIEW

NAND flash memory technology has undergone significant developments over the years to meet the evolving demands of various applications. Key advancements and challenges in this domain have been addressed through rigorous research and innovation.

Researchers in 1997 (1) introduced a 64-Mb NAND flash memory with improved read and program performances,

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achieving a 40 MB/s read throughput and a 5 MB/s program throughput, thus demonstrating enhanced data retrieval and storage capabilities. This advancement marked a significant milestone in the evolution of NAND flash memory technology.

A recent study (2) addressed the challenge of improving read latency in NAND flash memory by proposing a high-speed BL pre-charge scheme with an off-cell-like BL locking (OCBLL) to reduce BL coupling capacitance, alongside a sense-out-node amplification (SOA) scheme to enhance read accuracy. These innovative schemes represent crucial steps toward overcoming performance limitations in NAND flash memory.

In 2009 (3), researchers presented a 16 Gb 4-state MLC NAND flash memory with a sustained program throughput of 34 MB/s, achieved through the utilization of all available cells along a selected word line and additional performance enhancement modes, emphasizing the significance of optimizing memory architectures for improved efficiency. This study highlighted the importance of maximizing the utilization of memory cells to enhance overall performance.

A study in 2014 (4) introduced a true 3D 128Gb vertical-NAND (V-NAND) Flash, offering superior device scalability and achieving 50MB/s write throughput with extended endurance, thus showcasing the potential of 3D NAND technology for various applications. This research showcased the promising future of 3D NAND technology in addressing scalability and performance challenges in flash memory systems.

Overall, these studies underscore the continuous efforts to enhance NAND flash memory technology, focusing on improving performance, scalability, and cost-effectiveness to meet the growing demands of diverse applications.

III. DESIGN METHODOLOGY

The Offset Canceling Tri-State Sensing Latch (OCTSL) improves upon the Offset Canceling Sensing Latch (OCSL) by introducing three key features. Firstly, it incorporates a tristate sensing latch during the sense phase, eliminating short-circuits between VDD and GND and reducing variation in the threshold voltage (VTRIP). The shielding of floating nodes

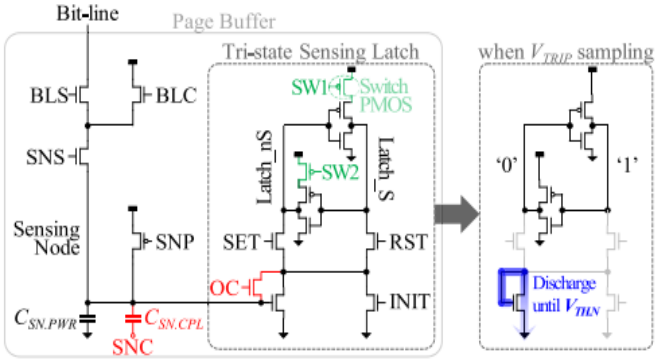

Fig 1. Page buffer and read operation of OCTSL.

The page buffer and read operation of the Offset Canceling Tri-State Sensing Latch (OCTSL) involve key steps in data handling. The page buffer temporarily stores the latch data during read operations. In the read operation, the sensing node is precharged and then connected to the discharge NMOS, allowing the latch to be read. The use of a sensing node coupling capacitor enables a tristate latch adoption, lowering enhances noise insensitivity. Secondly, in the sample phase, OCTSL includes sensing node precharge, reducing energy consumption and eliminating the risk of corrupting latch data. During the read operation, VTRIP is sampled by connecting a precharged sensing node to the discharge NMOS, minimizing energy use. Lastly, OCTSL includes a couple-down phase with a sensing node coupling capacitor, enabling tristate latch adoption and lowering the sensing node voltage for precise readings. A new DC regulator is introduced with minimal die area overhead to control the sensing node discharge level during the couple-down phase. Overall, OCTSL addresses short-circuit issues, VTRIP variation, and energy consumption, providing a more robust and efficient sensing latch design.

The Offset Canceling Tri-State Sensing Latch (OCTSL) is an improved version addressing issues in the Offset Canceling Sensing Latch (OCSL). It introduces three key features to enhance performance:

Tri-State Sensing Latch: In the sense phase, OCTSL incorporates a tri-state sensing latch, which helps eliminate short-circuits between power (VDD) and ground (GND). This reduces variation in the threshold voltage (VTRIP) and enhances overall stability. Additionally, the floating nodes (Latch_S and Latch_nS) are shielded to improve noise immunity.

Sensing Node Precharge in Sample Phase: During the sample phase, OCTSL includes sensing node precharge, which not only reduces energy consumption but also eliminates the risk of corrupting latch data. The read operation involves sampling VTRIP by connecting a precharged sensing node to the discharge NMOS, minimizing energy usage.

Couple-Down Phase with Sensing Node Coupling Capacitor: OCTSL incorporates a couple-down phase with a sensing node coupling capacitor. This enables the adoption of a tri-state latch, lowering the sensing node voltage for more precise readings. A new DC regulator is introduced with minimal die area overhead to control the discharge level of the sensing node during the couple-down phase, ensuring accurate and efficient operation.

the sensing node voltage for precise readings. The page buffer efficiently manages the temporary storage of latch data, while the read operation ensures accurate retrieval of information from the latch, facilitated by the tristate sensing mechanism and sensing node precharge in the Offset Canceling Tri-State Sensing Latch design.

SAPON:

Nowadays, low power VLSI is an emerging discipline where high power consumption has become a key metric in VLSI design. High power dissipation is not regarded as good when it comes to battery lifespan in the case of battery-operated applications. It alters reliability, cooling costs, and also contributes to the reduction of battery life. Switching and short circuit leakage power play a significant role in the high-frequency dynamic transition of inputs. Several standard reduction techniques exist to reduce the power consumption of circuits. In this paper, we have scrutinized the source of power consumption in static and dynamic leakage power and introduced a new technique called the SAPON (Stackly Arranged low Power ON transistor) technique to mitigate the

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power reduction of circuits. We have utilized various CMOS logic circuits such as INVERTER, NAND, NOR, and MUX to implement these techniques and compared their total power consumption with the standard reduction techniques.

IV. VERIFICATION METHODOLOGY

The tool used for simulation purpose for the entire research work is Tanner EDA tool version 13.0. The features and functionality of this tool has been described below:
In the process of developing electronic circuits, the design cycle includes a crucial phase known as pre-fabrication verification. This step is vital due to the expenses and time constraints associated with fabrication, making accurate verification essential for efficient design. Electronic Design Automation (EDA) tools are instrumental in this process, aiding in the design and verification of circuit operation by solving the circuit's differential equations numerically. Through simulation, these tools enable circuit designers to validate and refine their designs before sending them for fabrication. EDA tools offer various simulation techniques, including transient analysis, AC analysis, DC analysis, and frequency domain analysis, allowing designers to comprehensively evaluate circuit behavior under different conditions. Overall, EDA tools play a pivotal role in the pre-fabrication verification phase, helping streamline the design process, minimize errors, and ensure the production of high-quality electronic circuits efficiently.

Schematic Editor: Schematic Editor (S-Edit) serves as a user-friendly PC-based platform designed for schematic capture, offering robust capabilities for handling complex full custom IC designs. Integrated closely with Tanner EDA's suite, including T-Spice simulation, L-Edit layout, and HiPer verification tools, S-Edit empowers designers to navigate the fast-paced market efficiently, enhancing productivity and accelerating the realization of concepts into silicon. Its seamless integration with third-party tools streamlines the design capture process, enabling exploration of design choices and providing insights into their ramifications. By expediting the design cycle, S-Edit allows for greater flexibility in pursuing optimal solutions, thereby freeing up time and resources for process corner validation. This approach minimizes downstream risks, increases yield, and shortens time to market.

T spice: In order to translate concepts into tangible designs effectively, it's crucial to have a simulation tool capable of handling large circuits swiftly and accurately. This requires a tool that offers fast run times, seamless integration with other design software, and adherence to industry standards. Tanner T-Spice Circuit Simulator addresses these requirements by providing a user-friendly interface and a design environment that is both faster and more intuitive. Its notable features include support for multi-threading, device state plotting, real-time waveform viewing and analysis, and a command wizard for simplifying SPICE syntax creation. By streamlining the simulation phase, T-Spice helps save time and money during the design process.
Furthermore, T-Spice ensures more precise simulations by supporting the latest transistor models such as BSIM4 and the Penn State Philips (PSP) model. Its compatibility with various design solutions and ability to run on both Windows and Linux platforms make it easy and cost-effective to integrate into existing workflows.Additionally, T-Spice offers numerous innovations and improvements not found in other SPICE and SPICE-compatible simulators.

Waveform Editor: The Waveform Editor, known as W-Edit, is a software tool designed to showcase T-Spice simulation output waveforms in real-time during simulation runs. Visualizing the complex numerical data generated from VLSI circuit simulations is crucial for testing, understanding, and enhancing these circuits. W-Edit provides a user-friendly interface for viewing waveforms, offering ease of use, powerful features, and quick performance within a flexible environment designed for graphical data presentation.

Layout Editor (L-Edit): Within the suite of Tanner EDA tools, L-Edit serves as the layout editing software. It incorporates several essential features, including Interactive DRC for instantaneous design rule checking during the editing process. It also includes Standard DRC for hierarchical DRC, Standard Extract for netlist extraction, Standard LVS for layout versus schematic comparisons, Node Highlighting to highlight all geometry related to a specific node, and SPR for standard cell place and route functionalities.

V. RESULTS AND DISCUSSION

The Figure 2 shown below shows Schematic of OCTSL using SAPON and Figure 3 shows the Waveform of OCTSL using SAPON

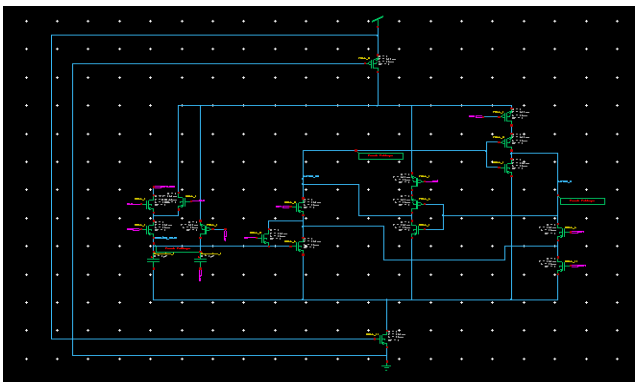

Fig.2 Schematic of OCTSL using SAPON

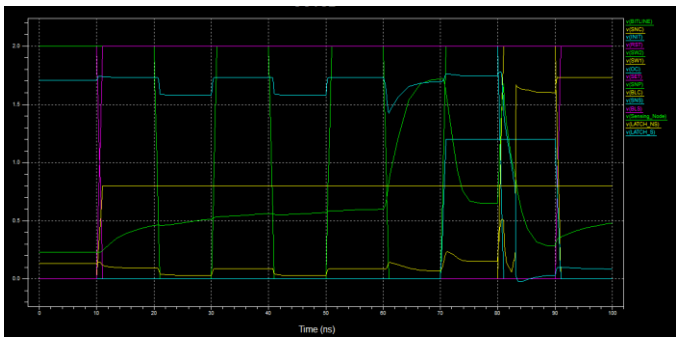

Fig 3 Waveform of OCTSL using SAPON

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Below mentioned is the area of OCTSL using SAPON

```
*  Device and node counts:
*              MOSFETs - 17
*                 BJTs - 0
*              MESFETs - 0
```

Here are the power results of OCTSL using SAPON

```
Power Results
vl from time 0 to 1e-007
Average power consumed -> 8.980757e-004 watts
Max power 1.511798e-003 at time 6.1e-008
Min power 4.354233e-004 at time 8.06823e-008
```

Delay of OCTSL will be as follows:

```
delay = 7.3101e-008
   Trigger = 1.0050e-008
   Target  = 8.3151e-008
```

VI. CONCLUSION

By integrating the tristate sensing latch with the Offset Canceling Sensing Latch (OCSL), significant alterations occur in the sense phase, making it independent from the inverter PMOS. This modification effectively eliminates the inherent voltage variation in the trip point caused by the inverter PMOS. Moreover, incorporating the tristate sensing latch eradicates short-circuit currents during read operations, resulting in a notable reduction in energy consumption during both sample and sense phases. Additionally, the absence of short-circuit currents in read operations mitigates the risk of data corruption in the sensing latch during the sample phase. Overall, this enhancement in the sensing latch mechanism not only enhances stability but also reduces energy consumption and improves data integrity during the sample phase, thereby contributing to a decrease in power consumption through the SAPON approach.

REFERENCES

[1] [1] J.-K. Kim et al., “A 120-mm264-Mb NAND flash memory achieving 180 ns/byte effective program speed,” IEEE J. Solid-State Circuits, vol. 32, no. 5, pp. 670–680, May 1997.
[2] [2] J. Sim and B. Lee, “Non-volatile memory device and read method thereof,” U.S. Patent 9 042 175, Aug. 1, 2015.
[3] [3] R. Micheloni, L. Crippa, and A. Marelli, Inside NAND Flash Memories, New York, NY, USA: Springer, 2010, pp. 197–233, doi: 10.1007/978-90-481-9431-5.
[4] [4] J. H. An, J. Y. Chun, H. K. Park, and S.-O. Jung, “All-bitline read scheme with locking bit-line and amplifying sense node in NAND flash,” IEEE Access, vol. 9, pp. 28001–28011, 2021, doi: 10.1109/ACCESS.2021.3058391.
[5] [5] S.-H. Joo et al., “Method of reading memory cells with different threshold voltages without variation of word line voltage and nonvolatile memory device using the same,” U.S. Patent 83 607, Apr. 4, 2013.
[6] [6] C. Missiroli et al., “Nand flash memory comprising current sensing page buffer,” U.S. Patent 140 823, May 18, 2017.
[7] [7] M. L. Mui et al., “BIT Line current trip point modulation for reading nonvolatile storage elements,” U.S. Patent 269 083, May 29, 2014.
[8] [8] R.-A. Cernea et al., “A 34 MB/s MLC write throughput 16 Gb NAND with all bit line architecture on 56 nm technology,” IEEE J. Solid-State Circuits, vol. 44, no. 1, pp. 186–194, Jan. 2009.
[9] K.-T. Park et al., “Three-dimensional 128 Gb MLC vertical NAND flash memory with 24-WL stacked layers and 50 MB/s high-speed programming,” IEEE J. Solid-State Circuits, vol. 50, no. 1, pp. 204–213, Jan. 2015, doi: 10.1109/JSSC.2014.2352293.
[10] Y. Li et al., “A 16Gb 3b/ cell NAND flash memory in 56nm with 8MB/s write rate,” in IEEE ISSCC Dig. Tech. Papers, San Francisco, CA, USA, Feb. 2008, pp. 506–632.