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An Optimized Fully Dynamic Latched Comparator for High Speedflash and Pipeline Data Conversion Applications

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***Abstract*—A Novel High Speed CMOS Comparator with low power dissipation, low offset and high speed is proposed. Inputs are reconfigured from typical differential pair comparator such that near equal current distribution in the input transistors can be achieved for a meta-stable point of the comparator. Restricted signal swing clock for the tail current is also used to ensure constant currents in the differential pairs. Nearly 14.6 mV offset voltage is easily achieved with the proposed structure making it favorable for flash and pipeline data conversion applications. The proposed topology is based on hysteresis using positive feedback and pre-amplifier stage, has a small power dissipation, less area, and it is shown to be very robust against transistor mismatch. Comparator structures are designed in Tanner S-edit and simulations are carried out in H-Spice to determine offset voltage, power - dissipation and speed. These are compared and the superior features of the proposed comparator are established.**

Keywords*—*Meta-stable, Differential pair, Offset-Voltage, Hysteresis, Pre-amplifier

I. INTRODUCTION

Over the years, development of digital integrated circuit has closely followed Moore's Law. As a result, transistor size has greatly shrunk and the speed of digital circuit has been exponentially increased. There exists very high speed digital circuit with its ever growing processing power and efficiency. In real world every signal is analog in nature. So there is a need to convert the analog signal into digital signal. In order to interact analog world with digital world some sort of interface is needed for proper communication. So data conversion circuits with high speed are needed for better transmission of information. This trend puts high pressure on analog circuit designers to develop very high speed interface circuits, namely, analog to digital [6] and digital to analog converters. In high-speed analog-to-digital converters, comparator design [12] has a crucial influence on the overall performance that can be achieved.

In this paper, we present a new dynamic latched comparator which shows lower input-referred latch offset voltage [11] and higher load drivability than the conventional dynamic latched comparators [2]. Even though numbers of transistors in the proposed comparator are more but overall area is small when compared to conventional dynamic latched comparators. This paper is organized as follows. Section-II provides architecture and design aspects of high speed comparators and section-III describe the conventional comparators. Section-IV describes the proposed dynamic latched comparator. Schematics and simulation results from HSPICE using 90nm PTM technology with V_{DD}=1V and their comparisons are presented in Section-V and conclusion is drawn in Section-VI.

II. DESIGN ASPECTS OF HIGH SPEED COMPARATOR

The following Figure 1 illustrates the various blocks involved in the high speed comparator.

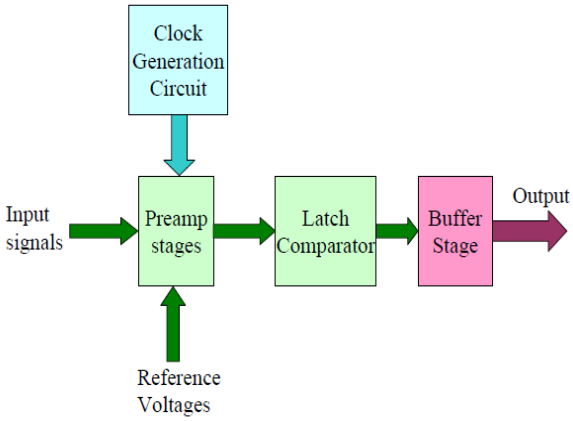

Fig.1. High Speed Comparator architecture

The pre-amplifier [10] is a circuit which is used to amplify the signal so that it can easily drive the load. In most latch comparator designs pre-amplifiers are also used to avoid the kickback effect [7] from the latch and input referred offset. This circuit is a differential amplifier with pull-up can be a resistor load or an active load. The design of the preamplifier must be done in such a manner that the desired latch input voltage is achieved in minimum time. The decision circuit is the heart of the comparator and should be capable of discriminating mV level signals. It is also called latch. The simplest form of a latch consists of two cross-coupled NMOS transistors.

The final component in comparator design is the output buffer. The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal (i.e., 0 or V_{DD}). The output buffer should accept a differential input signal. For a simple design for the output buffer, we can use the self-biased differential-amplifier.

III. CONVENTIONAL COMPARATORS

Different Conventional comparators are Open loop and Pre-amplifier Based Latched Comparators.

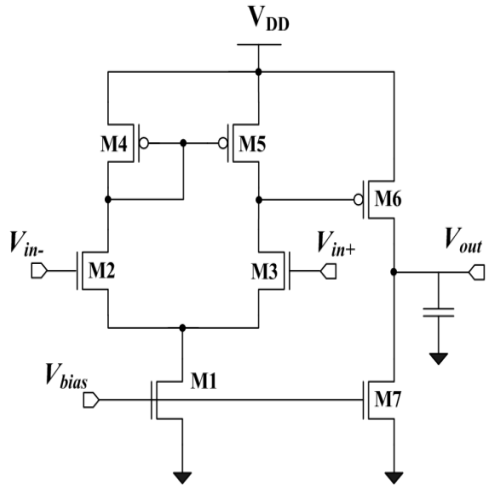

Fig.2. Open Loop Comparator

Open-loop comparators [3], shown in Figure 2, are an operational amplifier without frequency compensation to obtain the largest possible bandwidth, hence improving its time response. Since the precise gain and linearity are of no interest in comparator design, no-compensation does not pose a problem. However, due to its limited gain-bandwidth product, open-loop comparators are too slow for many applications.

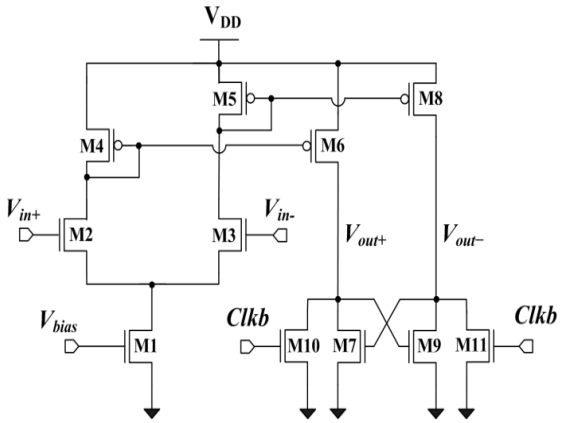

Fig.3. Pre-amplifier based latched comparator

An amplifier is employed before the latched comparator shown in figure 3, which decreases the offset voltages caused by the device mismatch as show in figure. The main advantages of the pre-amplifier based latched comparators are their high speed and low input referred latch offset voltage. In addition, by using pre-amplification stage, kickback noise can be considerably reduced and meta-stability problem also can be relaxed. Pre-amplifier based latch offer high speed and low offset while they still consume static power.

There are other types of comparators called fully dynamic latched comparators [2], which are Lewis-Gray Comparator, Differential pair comparator, Double-tail latch-type voltage SA [4], Two Stage Dynamic Comparator. Each comparator will have its own advantage and disadvantages. The various performance parameters of the comparators are compared in terms of power, size, offset voltage and delay and the superior features of the proposed comparator are established.

IV. PROPOSED COMPARATOR

The proposed comparator provides better input offset characteristic and faster operation in addition to the advantages of those comparators such as less kickback noise, reduced clock load and removal of the timing requirement between clock signals over a wide common-mode and supply voltage range. The overall area is small even though number of transistors is more. It is because of widths of transistors are optimized without compromising the speed and performance of the comparator.

For its operation, during the pre-charge (or reset) phase (Clk=0V), both PMOS transistor M4 and M5 are turned on and they charge Di nodes' capacitance to V_{DD}, which turn both NMOS transistor M16 and M17 of the inverter pair on and Di' nodes discharge to ground. Sequentially, PMOS transistor M10, M11, M14 and M15 are turned on and they make Out nodes and SW nodes to be charged to V_{DD} while both NMOS transistors M12 and M13 are being off. During the evaluation (decision-making) phase (Clk=V_{DD}), each Di node capacitance is discharged from V_{DD} to ground in a different time rate proportionally to the magnitude of each input voltage.

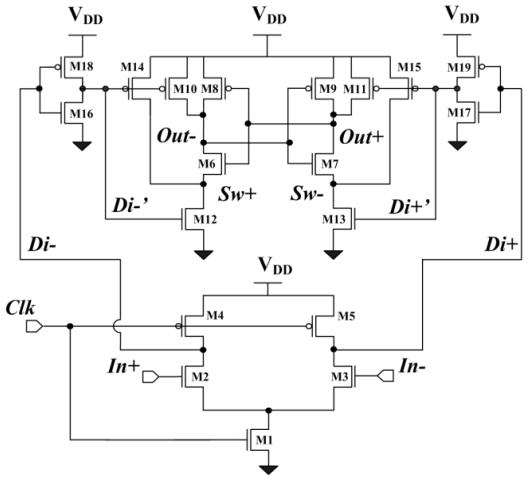

Fig.4. Proposed Comparator

As a result, an input dependent differential voltage is formed between Di+ and Di- node. Once either Di+ or Di- node voltage drops down below around $V_{DD}-|V_{tp}|$, the additional inverter pairs M18/M16 and M19/M17 invert each Di node signal into the regenerated Di' node signal. Then the regenerated and different phased Di' node voltages are amplified again and relayed to the output-latch stage by transistor M10−M13. As the regenerated each Di' node voltage is rising from 0V to V_{DD} with a different time interval, transistor M12 and M13 turn on one after another and the final amplification is made between SW nodes before the regeneration process. Once either of SW node voltages falls below around $V_{DD}-V_{tn}$, the output latch stage starts to regenerate the small voltage difference at Out nodes into a full-scale digital level.

A. Monte Carlo analysis

Monte Carlo analysis is usually utilized to model random mismatch [5] between different components due to process variation. Process variations may change the parameters of MOSFETs, BJTs and resistors. For accurate statistical simulation, a certain model for each of these components in a particular processing technology should be formed by the manufacturing company. These models include the distribution of different important technological parameters of each component, e.g., for a MOSFET these parameters are ΔV_{th} (threshold voltage variation), ΔW (width variation), ΔL (length variation), Δt_{ox} (oxide thickness variation), etc. Since each of these variations is originated from many other independent stochastic variables, these parameters would ideally have a Gaussian distribution. Every Gaussian distribution is characterized by its mean value and the standard deviation (σ) from that mean.

V. SCHEMATICS AND SIMULATION RESULTS

A. Schematics

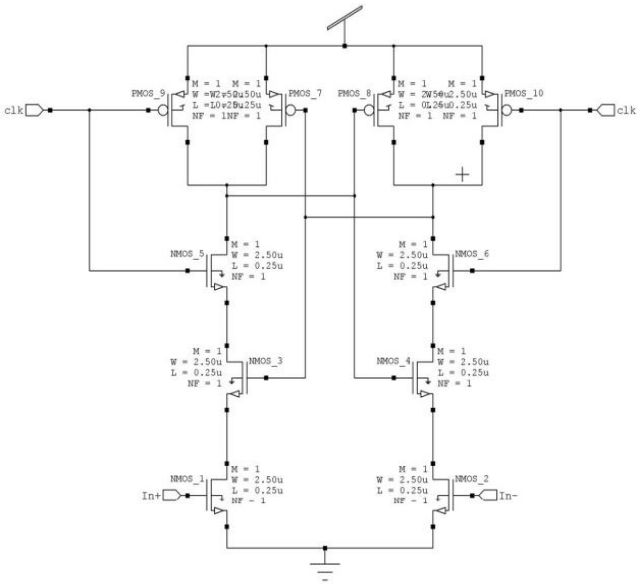

Fig.5. Lewis Gray Comparator (Comparator1)

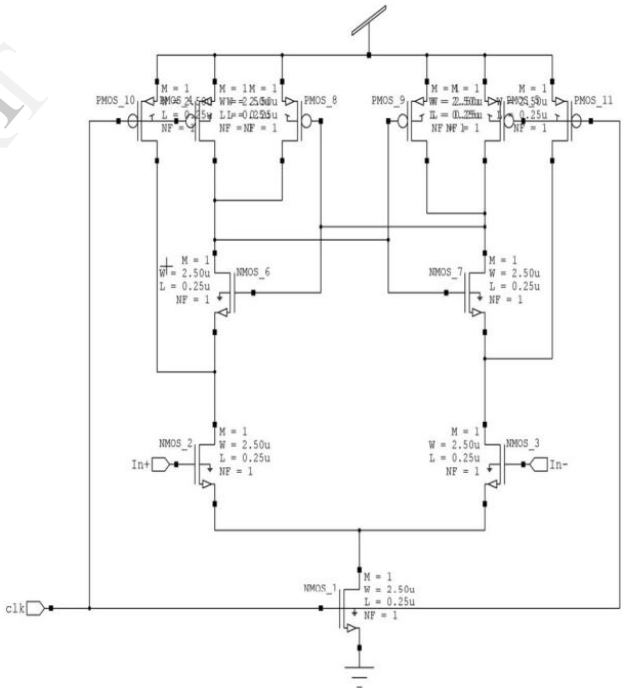

Fig. 6. Latch Type Voltage SA Comparator (Comparator2)

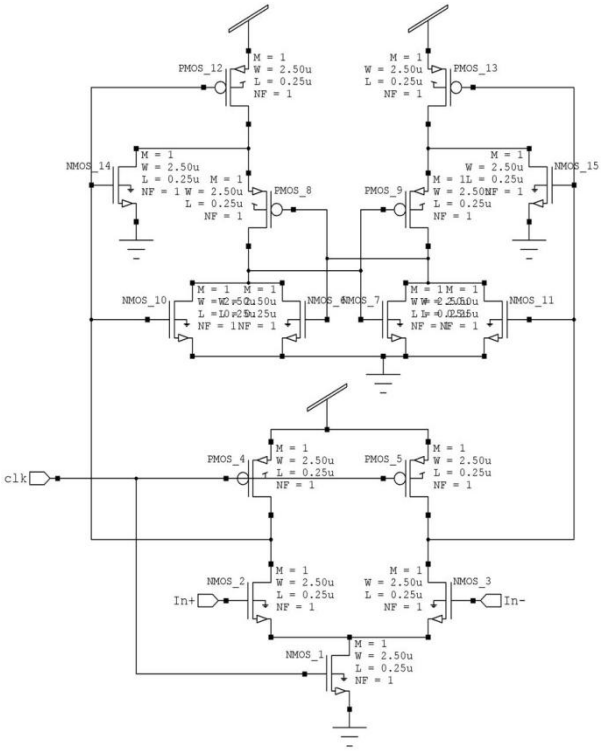

Fig. 7. Dual-Tail Latch-Type Voltage SA Comparator (Comparator3)

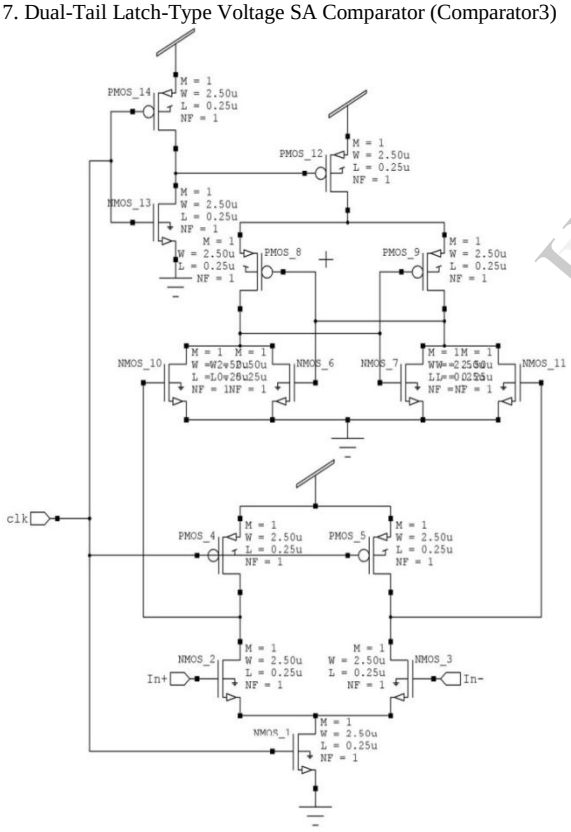

Fig. 8. Two Stage Dynamic Comparator (Comparator4)

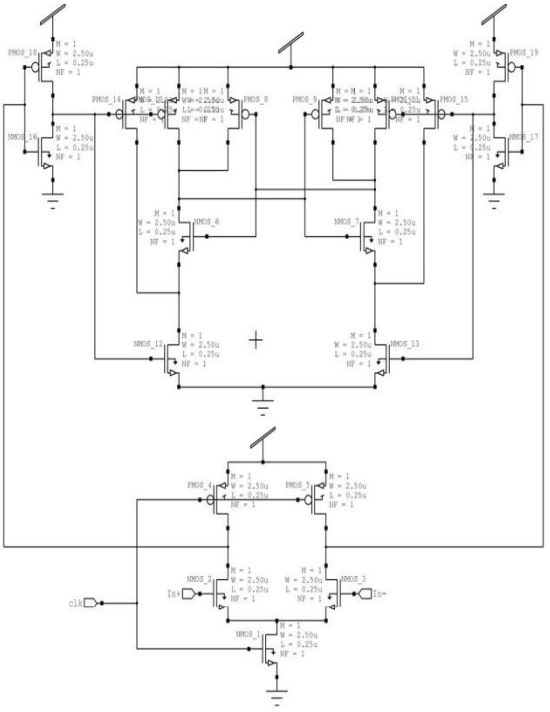

Fig. 9. Proposed Dynamic Comparator (Comparator5)

B. Simulated Waveforms

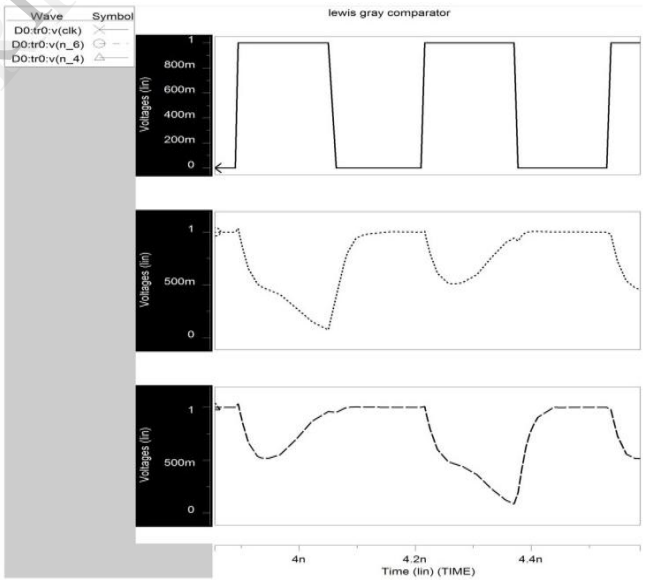

Fig. 10. Simulated Waveforms for Comparator1

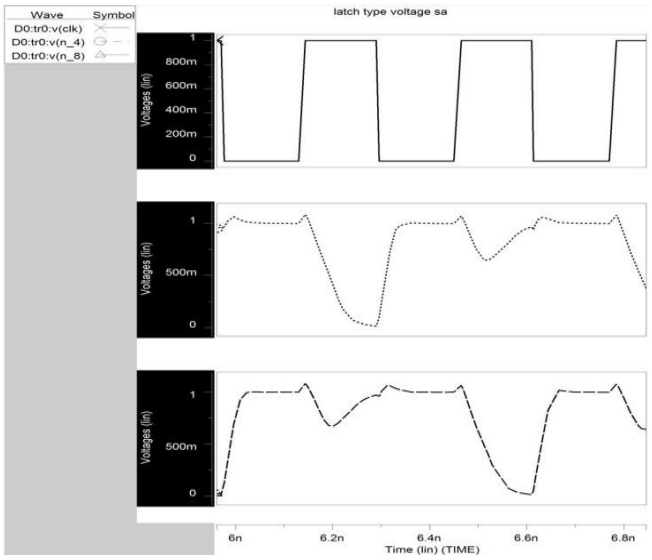

Fig. 11. Simulated Waveforms for Comparator2

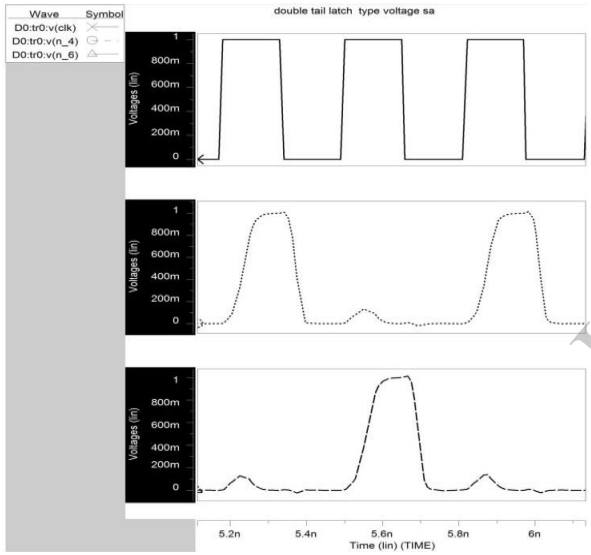

Fig. 12. Simulated Waveforms for Comparator3

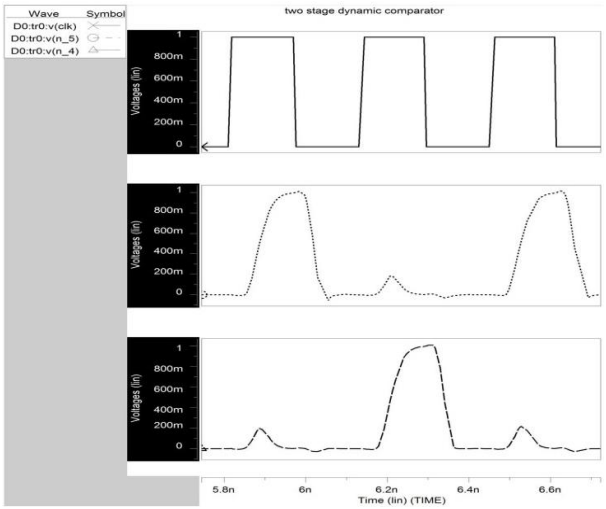

Fig. 13. Simulated Waveforms for Comparator4

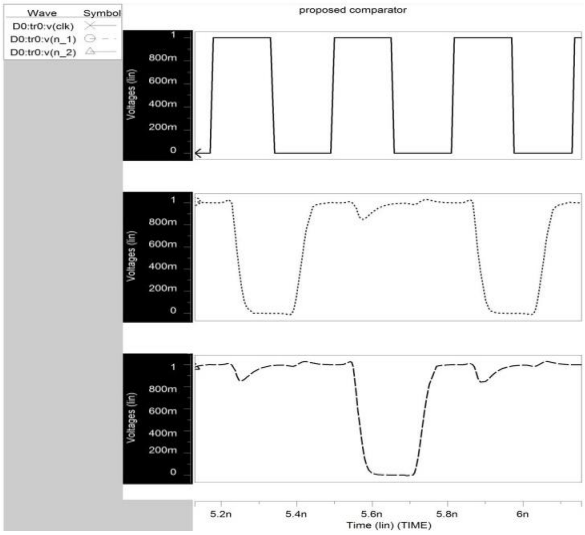

Fig. 14. Simulated Waveforms for Comparator5

C. Offset Simulation

Monte Carlo analysis is used to find the offset of comparators. For our simulation, all variations are assumed to be normally distributed about nominal values and the random mismatch in threshold voltage V_{th} was modeled as follows.

$$\sigma_{V_{th}} = \frac{A_{V_{th}}}{\sqrt{WL}} \quad Where\ W, L\ are\ in\ \mu m$$

A_{Vth} is process dependent parameter and assumed to be 3mV in our mismatch analysis.

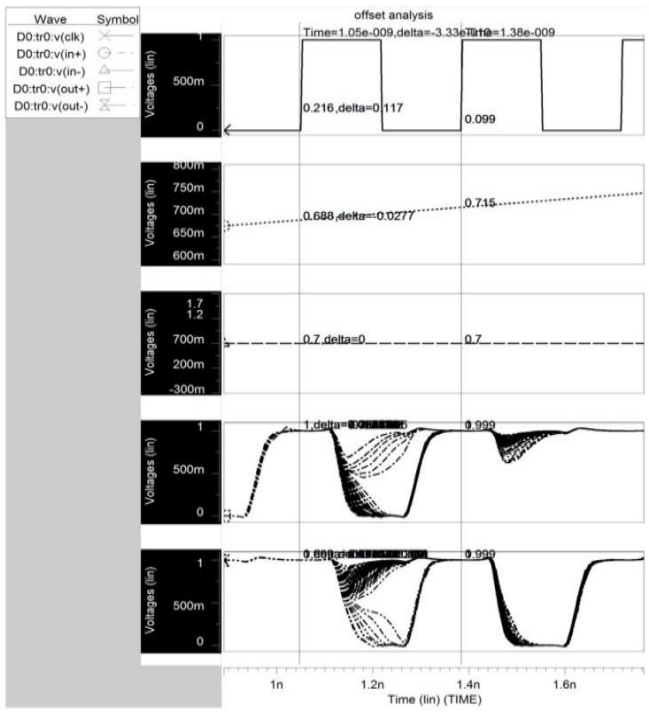

Fig.15. Monte Carlo Simulated waveform for offset calculation (Comparator5)

D. Performance Comparison

To compare the performances of the proposed comparator with conventional comparators, each circuit was designed using 90nm technology with $V_{DD} = 1V$, f_{CLK}=3GHz, C_{LOAD}=7fF, Temp=25^{0}C, and common mode voltage $V_{com} = 0.7V$ and simulated with HSPICE.

The power, delay and offset comparisons of five comparators are shown in Figures 16, 17 and 18 respectively in 90nm Technology.

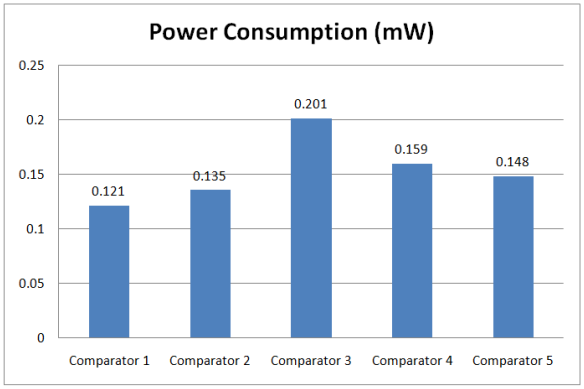

Fig. 16. Power comparison

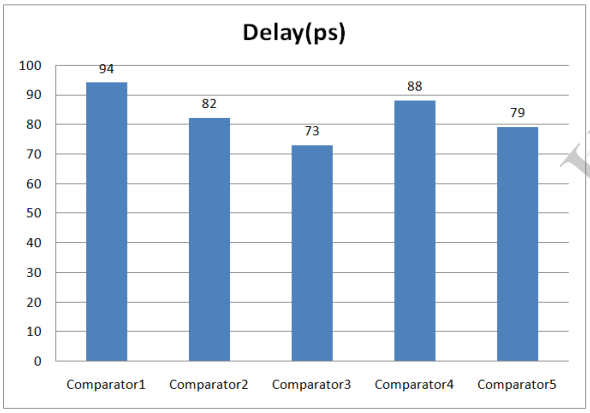

Fig. 17. Delay comparison

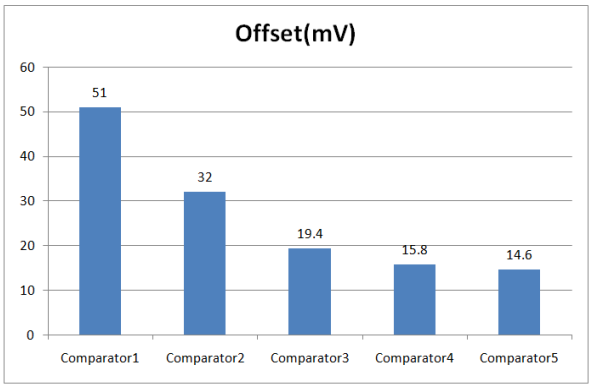

Fig. 18. Offset comparison

VI. CONCLUSION

A novel high-speed, low power and low-offset dynamic latch type comparator method is presented in this work. The proposed design uses isolated differential stage and latch stage which leads to low kickback noise and also it uses the preamplifier stage before the latch stage, which reduces the offset voltage by its gain. The Monte- Carlo simulation results clearly reveal that the dynamic latch comparator is able to switch properly with different input stepping sizes. The comparison study shows that the novel design is able to operate at a higher clock frequency of 3GHz with less offset voltage, low power and propagation delay in 1V supply voltage, which is better than other dynamic latched comparators.

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BIOGRAPHIES

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