

An RTOS-Based Architecture for Industrial Monitoring using ZIGBEE Wireless Network Stacks with Multi-Processor Support

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Abstract— RTOS (Real Time Operating System) is a Process which done between hardware and application. Packets have to send at particular time. During the packets transmission some collision may occur. To overcome this collision we are going to do this project. This project is implemented in two sections as prototype. First one runs with RTOS and LPC2148 as master node and another as normal data acquisition node to which sensors are connected. Second section may contain any controller as per need. Communications between two nodes are accomplished through wireless HART. The basic view of this technique is to reduce the possibility of collision (and thus increase the communication reliability), and to meet the critical requirement of timing determinism of industrial applications. This is essential to reduce the possibility of collision (and thus increase the communication reliability), and to meet the critical requirement of timing determinism of industrial applications. To do this, all the nodes must be synchronized precisely. Also, the stack designer must guarantee that the node can finish everything within the time slot. It offers advantages in terms of platform freedom, product life cycle, safety and security, system integration complexity, and performance quant ability. Associate in Nursing enforced Wireless HART stack has well-tried the feasibility of the planned design in sensible product style. And future challenges further as suggestions to Straightforward improvement area unit mentioned.

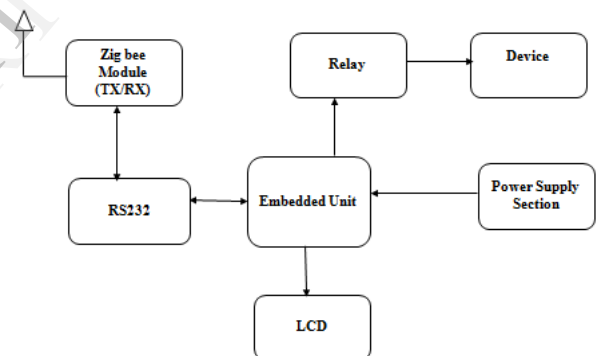
Index Terms: LPC2148, RS232, Monitoring Sensor Module, Actuator Unit

I. INTRODUCTION

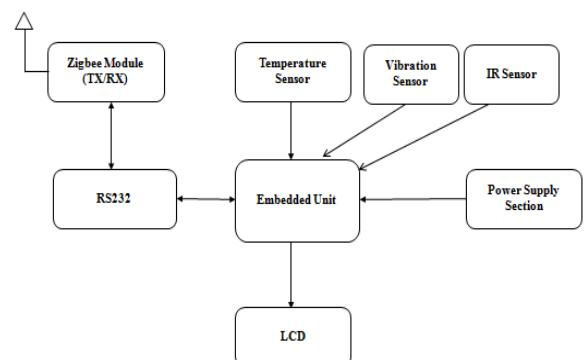
An enforced Wireless HART stack has well-tried the Feasibility of the projected design is for sensible product style. And future challenges yet as suggestions to plain improvement area unit mentioned. This is essential to reduce the possibility of collision (and thus increase the communication reliability), and to meet the critical requirement of timing determinism of industrial applications. To do this, all the nodes must be synchronized precisely, i.e. the jitter of synchronization should be much smaller than the length of time slot. Also, the stack designer must guarantee that the node can finish everything within the time slot. Such timing critical requirement has become one of the primary challenges to design the protocol stacks. Firstly, it is challenging to finish the complicated tasks

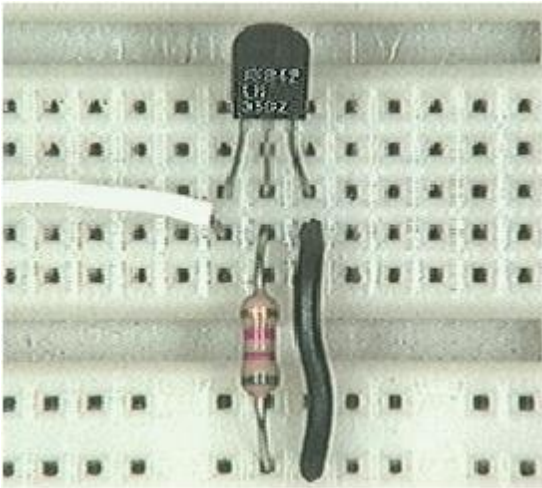
(packet parsing, encryption, decryption, authentication, etc.) within such a short timeslot by the processor with limited resource (clock frequency, memory, energy supply, etc.). Secondly, the IWSN stacks are often only a part of the timing critical tasks that the At the same time, the rapidly increasing complexity and other specific requirements of industrial systems have made it necessary to adopt the real time operation system (RTOS) in the IWSN stacks. However, the adoption of RTOS and support of multiprocessor have made it more challenging to guarantee the timing integrity. An optimized architecture is needed, but existing study on this topic is insufficient.

A. Master Node:



B. Data Acquisition Node:





Fig; LM35 Sensor

D. RS232

Computers transfer knowledge in 2 ways: parallel and serial. In parallel knowledge transfers, typically eight or additional lines (wire conductors) square measure went to transfer knowledge to a tool that's solely a number of feet away. samples of parallel transfers square measure printers and exhausting disks; every uses cables with several wire strips. though in such cases plenty of knowledge are often transferred in an exceedingly short quantity of your time by exploitation several wires in parallel, the gap cannot be nice.

To transfer to a tool set several meters away, the serial methodology is employed. In serial communication, the information is shipped one bit at a time, in distinction to parallel communication, within which the information is shipped a computer memory unit or additional at a time. The ARM has serial communication capability engineered into it, thereby creating doable quick knowledge transfer exploitation solely a number of wires.

When a chip communicates with the skin world, it provides the information in byte-sized chunks. In some cases, like printers, {the information the knowledge the knowledge} is solely grabbed from the 8-bit. since long cables diminish and even distort signals. What is more, AN 8-bit knowledge path is pricey. For these reasons, serial communication is employed for transferring knowledge between 2 systems set at distances of many feet to lots of miles apart. The Figures shows serial versus parallel knowledge transfers tedious and long. For this reason, there square measure special IC chips created by several makers for serial knowledge communications. Knowledge transfer rate: the speed of knowledge transfer in serial digital communication is expressed in bits per second (bits per second). Another wide used word for bits per second is baud. However, the information measure and bits per second rates don't seem to be essentially equal. this is often thanks to the

very fact that baud is that the electronic equipment word and is outlined because the range of signal changes per second. In modems, there square measure occasions once one modification of signal.

The very fact that in serial communication one knowledge line is employed rather than the 8-bit knowledge line of parallel communication makes it not solely less expensive however conjointly makes it doable {for 2|for 2} computers set in two completely different cities to speak over the phone. For serial digital communication to figure, the computer memory unit {of knowledge of information should be born-again to serial bits employing a parallel-in serial-out shift register; then it are often transmitted over one data line. This conjointly implies that at the receiving finish there should be a serial-in- parallel-out register to receive the serial knowledge and pack them into a computer memory unit. Of course, if Knowledge is to be transferred on the phone; it should be born-again from 0s and 1s to audio tones, that square measure sinusoidal-shaped signal. This conversion is performed by a electronic equipment referred to as electronic equipment, that stands for "modulator/ rectifier."

When the gap is brief, the digital signals are often transferred because it is on an easy wire and needs no modulation. This is often however IBM laptop keyboards transfer knowledge to the motherboard. However, for long-distance knowledge transfers exploitation communication lines like a phone, serial digital communication needs a electronic equipment to modulate (convert from 0s and 1s to audio tones) and draw out (converting from audio tones to 0s and 1s).

Serial digital communication uses 2 ways, asynchronous and synchronous. The synchronous methodology transfers a block of knowledge (characters) at a time whereas the asynchronous transfers one computer memory unit at a time. it's doable to write down code to use either of those ways, however the programs are often tedious and long. For this reason, there square measure special IC chips created by several makers for serial knowledge communications and knowledge transfer rate: the speed of knowledge transfer in serial digital communication is expressed in bits per second (bits per second). Another wide used word for bits per second is baud. However, the information measure and bits per second rates don't seem to be essentially equal. this is often thanks to the very fact that baud is that the electronic equipment word and is outlined because the range of signal changes per second. In modems, there square measure occasions once one modification of signal transfers many bits of knowledge. As way because the conductor wire is bothered, the baud and bits per second square measure identical.

The data transfer rate of a given automatic data processing system depends on communication ports incorporated into that system. as an example, the first IBM PC/XT might transfer knowledge at the speed of one hundred to 9600 bits per second. but in recent years, Pentium-based PCs transfer

knowledge at rates as high as 56K bits per second. It should be noted that in asynchronous serial digital communication, the baud is usually restricted to one hundred 000 bps.

E. RS232 STANDARDS

To allow compatibility among digital communication instrumentation created by varied makers, AN interfacing customary referred to as RS232 was set by the physics Industries Association (EIA) in 1960. In 1963 it had been changed and referred to as RS232A,B,C in 1965 and 1969, severally. Today, RS232 is that the most generally used serial I/O interfacing customary. This customary is employed in PCs and diverse varieties of instrumentation. However, since the quality was set long before the arrival of the TTL logic family, its input and output voltage levels don't seem to be TTL compatible. In RS232, a one is delineated by -3 to -25V, whereas a zero bit is +3 to +25V, creating -3 to +3 undefined. For this reason, to attach any RS232 to a microcontroller system we have a tendency to should use voltage converters like MAX232 to convert the TTL logic levels to the RS232 voltage level, and the other way around. MAX232 IC chips square measure ordinarily said as line drivers.

F. MAX3232 DESCRIPTION

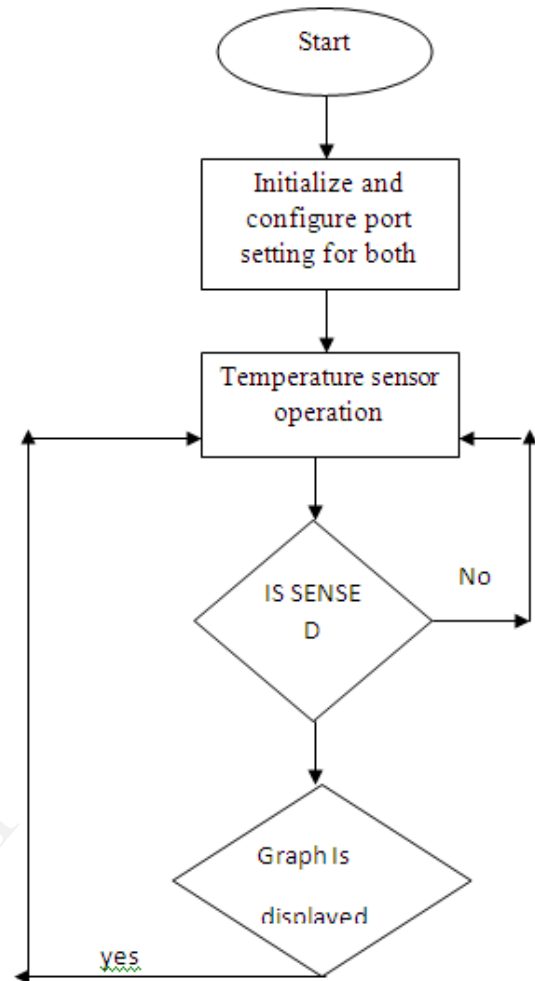
MAX3232 is compatible with RS-232 customary, have twin transceiver. every receiver converts TIA/EIA-232-E levels into TTL/CMOS levels. every driver converts TTL/CMOS levels into TIA/EIA-232-E levels. The MAX3232 is characterized for operation from -40°C to +85°C for all packages.

MAX3232 is purposed for application in superior informatics systems and management Baud rate: The ARM transfers and receives knowledge serially at several information measure rates. The baud within the ARM is programmable. This can be through with the assistance of timer one. The relationship between the crystal frequency and therefore the baud is mentioned here.

The ARM divides the crystal frequency by twelve to induce the machine cycle frequency. Within the case of XTAL = eleven.0592 MHz, the machine cycle frequency is 921.6 kHz (11.0592 rate / twelve = 921.6 kHz). The ARM's serial electronic equipment divides the frequency of 921.6 kHz by thirty two all over again before timer one to line the baud uses it. Therefore, 921.6 kHz divided by thirty two offers twenty eight, 800 Hz.

This is the amount that's used throughout here to seek out the timer one price to line the baud. once timer one is employed to line the baud it should be programmed in mode two, that's 8-bit, auto-reload.

G. Flow chart



To induce the information measure rates compatible with the laptop, we have a tendency to should load. The values shown during this table are the information measure rates supported by 486/Pentium IBM laptop

IV. CONCLUSION

In Future RTOS architecture support the wireless sensor network architecture. In this advantage of Wireless HART stack implemented on a lowest cost two processor platform. In the current Situation, we have analysed, a huge amount of messages are transmitted between layers. reduce the possibility of collision (and thus increase the communication reliability), and to meet the critical requirement of timing determinism of industrial applications. This is essential to reduce the possibility of collision (and thus increase the communication reliability), and to meet the critical requirement of timing determinism of industrial applications.

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