International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 1 Issue 6, August - 2012

Analysis and Comparison of Leakage Reduction Techniques for 6T-SRAM and 5T-SRAM in 90nm Technology

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Abstract: **As the feature size of the transistor is scaled down, the leakage power substantially increases. According to Moore's law, number of transistors doubles in every eighteen months. This shows that in upcoming years, power dissipation would be one of the major factors. One of the major fields where leakage power is prominent is in memory. Memory used as bridging between processor and the main memory is known as cache memory as these are faster and keep a pace with the processor in retrieving the data because main memory is slow.**

While designing cache memory, 6T-SRAM is the standard form all over. There is always a trade-off between speed, area and power in SRAM. Consequently, as the channel length reduces, the standby leakage in cache memory increases.

To minimize the leakage power dissipation in cache memory, various leakage reduction techniques were applied to 6T-SRAM and 5T-SRAM. The techniques implemented on 6T-SRAM and 5T-SRAM includes MT-CMOS, dynamic voltage scaling and gated V_{DD}. The technology used for these memories is GPDK 90nm using Cadence Virtuoso.

Keywords **— Leakage Power, 6T-SRAM (Static Random Access Memory), 5T-SRAM, MT-CMOS (Multi-Threshold Complementary Metal Oxide Semiconductor), Gated V_{DD}, Dynamic Voltage Scaling.**

I. INTRODUCTION

Memory is a basic element used for storing and retrieving data. Magnetic disks, optical disks are the examples of memory. The data is stored in memory in terms of logic 0 or logic 1, one bit at a time. Cluster of eight bits is called a byte and further grouping makes the hierarchy of mega and gigabytes.

Memory is a sequential circuit which employs a latch for storing a bit. The array of memory makes hierarchy for storing several bytes of data. Memory is broadly categorized in two ways – volatile and non-volatile. Volatile memory stores the data as long as power is present. RAM is the widest used example in volatile memory. Non-volatile memory is a kind of memory that stores the data even in the absence of power. ROM supports non-volatile memory.

Read Only Memory (ROM)

ROM is a read memory that retains the data when the power is turned OFF. Its key function in PC is to boot the system at the startup.

Random Access Memory (RAM)

RAM is the read write memory that retains the data as long as the power is supplied. RAM is used as the main memory for reading from the memory or writing into the memory through the address lines. RAM is of two types- SRAM and DRAM.

Static RAM (SRAM)

The static RAM uses latch as sequential circuits for storing the data. Unlike DRAM, it doesn't require any periodic refresh since latches retains the data. It is mostly used in cache as it has faster access time. It has low density for storing the data as it requires more number of transistors for storing single bit.

Dynamic RAM (DRAM)

Dynamic RAM comprises of a capacitor and a transistor for storing a bit. Since it employs a capacitor which is a major reason for not able to retain the data, it requires constant refreshing. In view of the fact that its storing density is more and has relatively more access time as compared to SRAM, it is mostly employed in main memory.

Cache Memory

Cache memory is placed between the main memory and the processor. As the main memory is slow and cannot keep a pace with the speed of the processor. In order to fetch the instructions readily from main memory caches are best at this place. SRAMs are used as cache memory as these are faster in accessing the data compared to DRAM since latter requires periodic refresh. This frequent refresh requires more access time which makes it slower than SRAM. Additionally, SRAMs are costlier than DRAMs.

II. NECESSITY OF LOW POWER

In the past, power dissipation was never the major issue as the transistor density and the operating frequency was less that could lead to this factor. Gradual growth rate in transistor density resulted in adverse effect of power dissipation. Chip area and speed are the major trade-off considerations but a low power design decision affects the aspects such as reliability, design cycle time, reusability, testability, and design complexity [4].

First factor is the increasing in number of transistors predicted by Moore's law that number of transistors will increase in every 18 months [3]. The need of low power arises from such evolution forces of integration circuit. The need for low power chips is the increased market demand for portable electronic devices that require batteries.

Sources of power dissipation

There are three sources of the power dissipation that can be classified as dynamic power dissipation and static power dissipation in digital CMOS circuit [2]. Short circuit and switching are the types of dynamic power dissipation whereas static power consumption occurs due to sub-threshold leakage current, reverse bias diffusion leakage.

In dynamic power dissipation the parasitic capacitances are charged and discharged during logic transition. The current flowing through the path offering resistance results in electrical energy converting to power dissipated as heat. The power dissipated is proportional to the square of the supply voltage, node voltage swing and the average switched capacitance per cycle.

$$P_{switching} = \alpha (V_{DD})^2 C_{Load} f \text{ [1]} \qquad \text{Eq.(1)}$$

The second source of power dissipation is when there is a short circuit current flowing from supply to ground while n-sub network and p-sub network are conducting simultaneously. During the interval when both logics are changing in response to the change in output. The duration during which both the networks are simultaneously on, depends on their rising and fall time and thus depends the duration of short circuit current.

$$P_{shortckt}=V_{DD}*I \text{ [1]} \qquad \text{Eq.(2)}$$

The static power dissipation consists of leakage current flowing through the transistor when input and outputs are not changing. This current is known as sub-threshold leakage current since it occurs when the gate voltage is less than the threshold voltage. In other words, sub-threshold leakage is a drain-source current of transistor when gate-source voltage is less than threshold voltage of the transistor [4].

$$I_{subth}=A*e^{q/nkT(V_{GS}-V_{th})}(1-e^{qV_{DS}/kT}) \text{ [5]} \qquad \text{Eq.(3)}$$

$$P=I_{stat}*V_{DD}$$

III. LEAKAGE IN CELL

Leakage current comprises of sub-threshold leakage current, gate leakage current and gate induced drain leakage. In SRAM when WL is asserted 0 (Fig.1), and BL and $\overline{BL}$ are pre-charged to V_{DD}, with node Q and $\bar{Q}$ storing 0 and 1 respectively [16-17], their exist leakage current. With the above said condition, both the access transistors are OFF. In OFF state, sub-threshold current flows through transistors M1, M4 and M5 since these are OFF. Transistors M2, M3 and M6 contribute to gate leakage current. Gate induced drain leakage current flows through transistors M2, M3, M5 and M6. To minimize all these leakage current, following techniques are applied to the memory cell.

(i). Gated V_{DD}

The power that dominates in transistor is sub-threshold leakage and gate-leakage power. As the size of the transistor is scaled down in deep sub-micron, it has become the major component that cannot be neglected any more as it majorly contributes to the leakage power. To minimize the leakage power, a high Vth gated V_{DD} transistor is placed between the circuit and ground [7]. Alternately, PMOS can be employed as gated V_{DD}. PMOS reduces the overhead area because it does not require any necessary sizing as NMOS gated V_{DD} does. But it is not mostly preferred if used in terms of saving the power since it cannot isolate the bit-line with the ground.

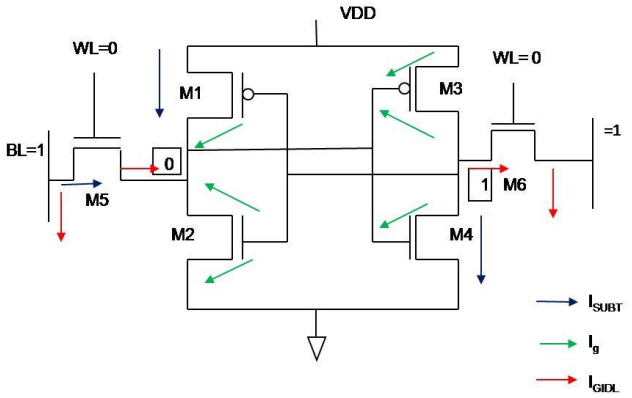

Fig.1. Schematic visualizing leakage in 6T-SRAM in standby mode [4]

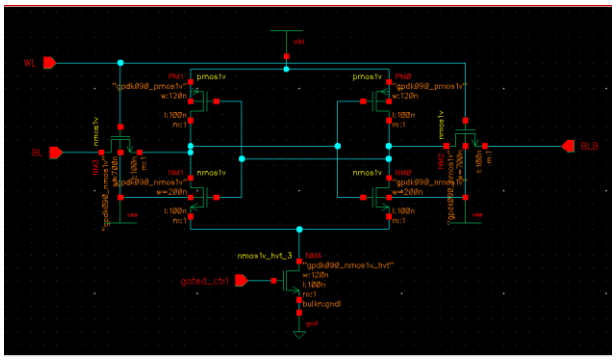

Fig.2. Schematic of Gated V_{DD} with 6T-SRAM

A high threshold NMOS transistor is used to turn OFF the power from the memory cell when it is not in use (Fig.2). Since leakage depends exponentially on the threshold voltage, it is possible to reduce leakage power to a large extend by employing a high threshold device [14]. When the memory cell is in use this signal is ON, providing the path to ground. When the WL (word line) is held low, no functioning takes place in the cell, at the same time gated signal is turned low to reduce the leakage of the circuit.

NMOS gated V_{DD} should be sized such that it saves energy. If the size is varied more, it becomes less efficient for power. Sizing of the NMOS gated V_{DD} can be decided depending on the size of the NMOS transistor since any one of them only would be ON during read operation. Gated V_{DD} is more favorable during the read operation.

(ii) .Dynamic voltage scaling

Another method to reduce leakage power is dynamic voltage scaling. This circuit employs two PMOS high threshold transistors that have their individual signal to supply V_{DD} during the active mode of the circuit and low voltage to be activated when the circuit is in sleep mode [14].

In the architecture, two PMOS transistors are placed between the V_{DD} and memory cell. M7 transistor supplies V_{DD} to the circuit when the input signal LV (low voltage) is low during

the active mode of the cell. On the contrary, M8 transistor is turned ON by applying the signal $\overline{LV}$ to the memory cell when the circuit is in sleep mode. To improve the leakage current of the circuit, the pass transistors can also be employed with high threshold voltage.

The circuit is more susceptible to noise and the threshold voltage varies across the process corners.

(iii).MT-CMOS(Multi-Threshold Complementary Metal Oxide Semiconductor)

The architecture of MT-CMOS consists of high threshold transistors, placed near the supply or GN and the circuit [15]. In SRAM, PMOS high V_{TH} is placed between V_{DD} and the memory while NMOS high V_{TH} transistor is positioned between cell and GND. The memory cell comprises of low V_{TH} transistors for high speed. These are connected to virtual V_{DD} and virtual GND instead of direct supply. In active mode, transistors M7 and M8 are ON while memory carries it functional read and write operation when WL is high. At this point of time, transistor M7 and M8 connects the circuit from virtual V_{DD} to V_{DD} and virtual GND to GND respectively. Conversely, when WL is inactive, the circuit moves in sleep mode. In this OFF state, the transistors M7 and M8 disconnects the circuit from the V_{DD} and GND. The circuit remains in the floating state during sleep mode. This leads to the reduction in the leakage current. The only drawback of this architecture is that as soon as the power is OFF, it loses its data.

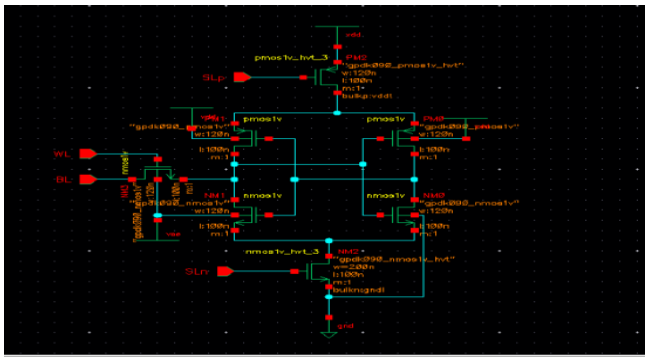

Fig.3. Schematic of MT-CMOS in 5T-SRAM

To avoid such state, diodes can be connected in parallel to the high V_{TH} transistors. During active mode, the high V_{TH} transistors are ON while diodes are OFF. On the contrary, the diodes conduct during sleep mode resulting in retaining the data with reduced leakage current.

IV. RESULT

The architecture of the SRAM and the leakage reduction techniques were implemented using 90nm technology file in Cadence Virtuoso. These blocks were simulated using Spectre and techniques to reduce leakage power were implemented.

The leakage current flowing through the transistors that were in off state, the graphs were plotted. The average of these current of each off-state transistor was calculated and the obtained current of each transistor was summed up and power dissipation in standby was achieved by the product of sum of leakage current and V_{DD}.

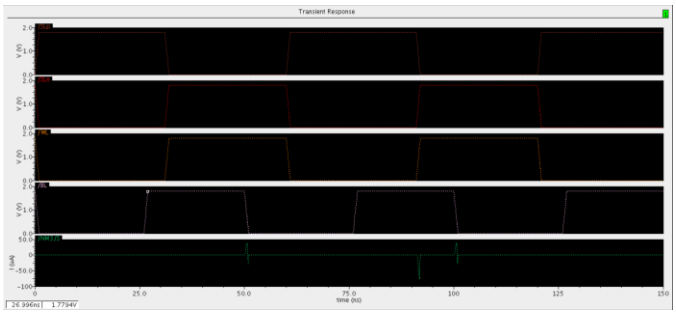

Fig.4. Current waveform of MT-CMOS 5T-SRAM

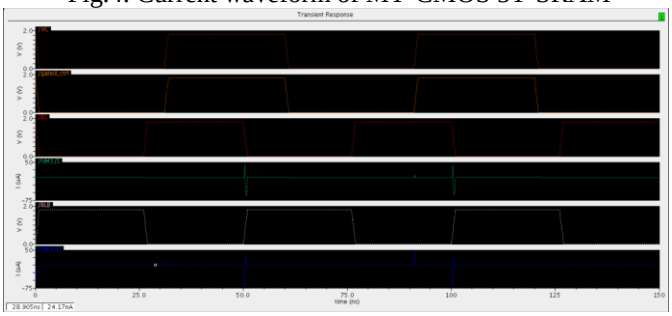

Fig.5. Current waveform gated V_{DD} 6T-SRAM

The leakage reduction techniques were implemented and leakage power was measured for all those transistors that were in off state.

Low power technique	6T-SRAM in µW	5T-SRAM in µW
Conventional	9.5	4.14
MT-CMOS	5.24	**2.33**
Dynamic voltage scaling	7.3	3.4
Gated-V_{DD}	**5.1**	3.4

Table.1. Comparison of low power techniques applied on 6T-SRAM and 5T-SRAM

V. CONCLUSION

Proper read and write operation of 5T-SRAM and 6T-SRAM were performed and leakage power was calculated. Subsequently, leakage reduction techniques were implemented on these SRAMs and it was found that MT-CMOS has reduced leakage power in 5T-SRAM to a large extent. Gated V_{DD} was effective on 6T-SRAM as it reduced the leakage by 46%. The percentage by which the leakage power was reduced by MT-CMOS technique on 5T-SRAM was found to be 43.71%.

REFERENCES

[1] Jan M.Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits:A Design Perspective" Prentice Hall series in electronics and VLSI, Prentice Hall, second edition, 2009

[2] Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" John Wiley & Sons, pp.253-269, 2000

[3] Gary Yeap, "Practical Low Power Digital VLSI Design" Springer, pp.159-163, 2009

[4] Behnam Amelifard, Farzan Fallah, Massoud Pedram,“ Leakage Minimization of SRAM Cells in a Dual-Vt and Dual-Tox Technology”, *IEEE* TVLSI-00009-2007

[5] Ashish Siwach, Rahul Rishi, “Asymmetric SRAM-Power Dissipation and Delay”, IJCEM International Journal of Computational Engineering & Management, Vol. 11, January 2011.

[6] Rohit Sachdeva “Analysis and design of cache memory cell for leakage reduction”,Thapar University, July 2009.

[7] Michael Powell, Se-Hyun Yang, Babak Falsafi, Kaushik Roy, and T. N. Vijaykumar “Gated-VDD: A Circuit Technique to Reduce Leakage in Deep-Submicron Cache Memories”,ISLPED 2000 Rapallo, Itlay

[8] Nicholas LiCausi, “A Survey Of SRAM Performance Enhancements” , Rensselaer Polytechnic Institute,Troy, July 2007

[9] Neeraj Kr. Shukla, Shilpi Birla, R.K. Singh and Manisha Pattanaik “Analysis of the Effects of the Operating Temperature at the Performance and Leakage Power Consumption in a Conventional CMOS 6T-SRAM Bit-Cell at 65nm, 45nm, and 32nmTechnologies”, IACSIT International Journal of Engineering and Technology, Vol.3, No.1, February 2011

[10] Shrivathsa Bhargav and Jaime Peretzman ,“Designing an SRAM array at the 90nm CMOS tech node”

[11] Irina Vazir, Prabhjot S.Balaggan, Sumandeep Kaur, Cailan Shen “SRAM IP for DSP/SOC projects”, San Jose State University

[12] Jeyran Hezavei, N.Vijaykrishnan, M.J.Irwin,“A Comparative Study of Power Efficient SRAM Designs”, Pond Laboratory, Department of Computer Science & Engineering, Pennsylvania State Univeristy

[13] Ingvar Carlson, Stefan Anderson, Sreedhar Natarajan, Atila Alvandpour “A High Density, Low Leakage, 5T SRAM for Embedded Caches”,2004

[14] Krisztián Flautner, Nam Sung Kim, Steve Martin, David Blaauw, Trevor Mudge,“Drowsy Caches: Simple Techniques for Reducing Leakage Power”, International Society for Computers and their applications, 2002

[15] Satoshi Shigematsu, , Shin’ichiro Mutoh, Yasuyuki Matsuya, Yasuyuki Tanabe and Junzo Yamada, “A 1-V High-Speed MTCMOS Circuit Scheme for Power-Down Application Circuits” IEEE Journal Of Solid-State Circuits, Vol. 32, No. 6, June 1997

[16] Navid Azizi, Farid N. Najm ,“An Asymmetric SRAM cell to lower Gate Leakage”, IEEE Computer Society, 2004

[17] Jiajing Wang, Amith Singhee, Rob A. Rutenbar, and Benton H. Calhoun, “Two Fast Methods for Estimating the Minimum Standby Supply Voltage for Large SRAMs,” IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 29, No. 12, December 2010.