Analysis Of A High Efficient Single-Stage Single-Switch Electronic Ballast For Compact Fluorescent Lamps

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***Abstract*—A single-stage dimmable electronic ballast with very high power factor and high efficiency is presented in this paper. A compact Fluorescent lamp power circuit is designed by integrating a SEPIC power factor corrector with a current-fed resonant inverter. This integration produces a single power-processing unit that minimizes the number of circuit components. The proposed resonant inverter reduces the circulating current in the resonant tank and allows simple gate drivers to be used so that isolation devices can be eliminated. With the SEPIC power factor corrector stage operating in the discontinuous conduction mode (DCM), a close-to-unity power factor is achieved for different lamp-power conditions. A small-signal analysis is presented, and a simple variable frequency controller is provided for dimming operations. Simulation waveforms are provided to highlight the merits of the proposed circuit for a 40-W compact fluorescent lamp.**

***Index Terms*—Electronic ballast, Compact fluorescent lamps, power factor correction.**

I. INTRODUCTION

Due to higher lamp efficacy and longer lifetime, compact fluorescent lamps (CFLs) are becoming more widely used than incandescent lamps. Table I compares the lumen performance between a CFL and incandescent lamp [1]. It shows that for the same amount of light output, a CFL consumes only one-third of the power of an incandescent lamp. Hence, CFL presents a very attractive approach to reduce energy cost in lighting applications. In fluorescent lamps, it is well known that ballast is required to provide sufficient high voltage for proper lamp ignition and stabilize the lamp current once the lamp arc is established. The conventional line-frequency magnetic ballast is heavy and bulky, which makes the device itself too large to be installed inside the CFL. The low operating frequency also causes light flickering, and it is impossible to implement dimming operations with a magnetic ballast. As a result, electronic ballast becomes the most suitable candidate to be used in CFL applications. A typical electronic ballast configuration consisting of a power factor correction (PFC) stage and a resonant inverter is shown in Fig. 1(a). This two-stage circuit [2] results in a high-cost and large-size circuit. Single-stage inverters (SSIs) are then proposed [3]–[9] by combining the PFC switch and one of the switches in the half-bridge resonant inverter together, as shown in Fig. 1(b), using the synchronous switch concept [10]. This design presents significant improvements in size and cost reduction over the conventional two-stage circuit. The main drawback with the SSI is the need of a complicated control circuit to function as dc-link voltage regulation and output-lamp current regulation. In this paper, a single-stage dimming electronic ballast with variable frequency control using an integrated buck-boost PFC current-fed resonant inverter is proposed.

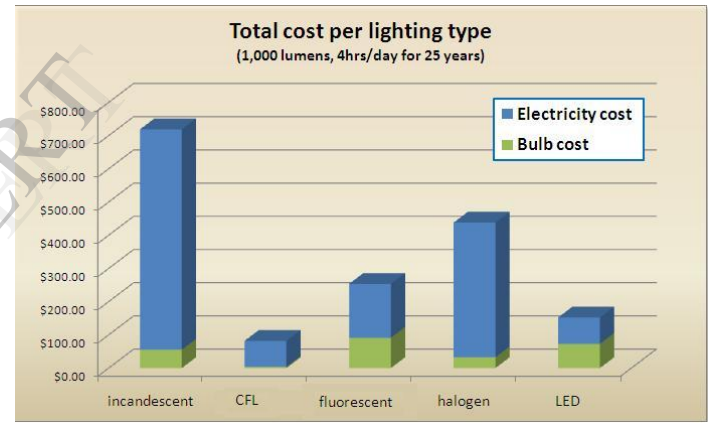


Fig 1: Total cost per Lighting types

TABLE I
COMPARISONS BETWEEN A CFL AND AN INCANDESCENT LAMP

luminous flux (light output)	Incandescent	Compact fluorescent
450 lm	40 W	7-11 W
600-700 lm	60 W	11–15 W
950 lm	75 W	18–20 W
1200 lm	100 W	20-28 W
1600 lm	125 W	28-32 W
1900 lm	150 W	35-42 W

Although the efficiency of the SSI tends to be lower than the conventional design approach, the proposed SSI circuit saves one MOSFET and a PFC controller compared to the two-stage high-power-factor ballast circuit. It also allows a simple-switch driver circuit to be used without any isolation devices. The controller circuit utilizes the use of a simple lamp dimmer to achieve dimming operation by varying the switching frequency of the resonant circuit. By closed-loop feeding the lamp current to the proposed controller, the lamp is always driven by a current source, and stability can be guaranteed.

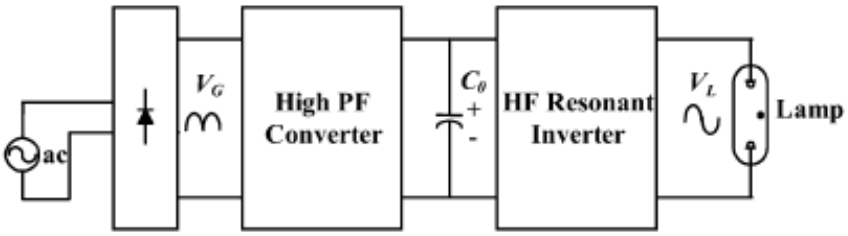


Fig.2 : Typical Block diagram of Electronic Ballast in Commercial CFL.

Detailed operating principles of the proposed circuit will be discussed in this paper. To further reduce the number of MOSFETs required in the ballast power circuit, single-switch electronic ballasts were reported in [12]–[17] by using the class-E resonant inverter. These electronic ballasts use only one switch to simultaneously achieve PFC while providing the lamp current stabilization at lower than the conventional two-stage electronic ballast with boost PFC. This paper proposes new high-power-factor single-switch electronic ballast for CFL applications. The proposed circuit has both lower peak current and voltage stress across the switch than that of the class-E resonant inverter. Detailed operating principles and characteristics of the proposed circuit are provided in this paper. The merits and performance of the circuit are justified through experimental results. This paper is organized as follows. Section II provides a detailed description of the operating principles of the proposed single-switch ballast
circuit. The mathematical analysis of the proposed ballast circuit, including current and voltage stress analysis on all the semiconductor devices is discussed. Section III gives a design example and provides experimental waveforms to highlight the performance of the circuit. Section IV summarizes the merits of the proposed work.

This paper is organized as follows. Section II provides detailed description of the operating principles of the proposed single-stage ballast circuit. Section III gives a detailed discussion on the mathematical design of the proposed ballast circuit and provides a design example, including small-signal analysis and the controller design. Section IV provides all the simulation and experimental waveforms to highlight the performance of the circuit on a 40-W CFL. Section VI gives a conclusion to summarize the merits of the proposed research.

II. Descriptions and Characteristics of Proposed Circuit

A. *Derivation of Proposed Single-Stage Ballast Circuit*

To design a low-cost and small-size high-power-factor electronic ballast circuit for CFLs, the design objective is to reduce the number of active components (i.e., diode and MOSFET) in the power circuit. Since it is not possible to further reduce the switch count from the active PFC stage perspective,

switch count reduction is performed on the inverter stage. A single switch current-fed resonant inverter is proposed by

connecting the switch (M_1) in series with a diode (D_1), as shown in Fig. 3(b). The other circuit elements that make up the single switch inverter include: an input inductor (L_{in}) and a
resonant circuit consists of L_r and C_r , and a starting inductor (L_p) An advantage of the proposed inverter circuit compared to the class E resonant inverter is that when the switch is ON, only the input current (i_{in}) will flow through the switch, as illustrated in Fig. 3.This means that the conduction loss of the MOSFET is significantly reduced in the proposed design compared to the class-E resonant inverter. Another advantage of the proposed single switch resonant inverter is that the MOSFET voltage stress is much lower than that of the class-E resonant inverter. The MOSFET peak voltage of a class-E resonant inverter is approximately 3–5 times the peak of the input voltage. However, in the proposed circuit, the voltage across the MOSFET is a function of

both L_{in} and C_r . Hence, by properly designing L_{in} and C_r , the voltage across the MOSFET can be minimized. In active PFC, a front-end converter is required to Provide very high power factor at the line input. DC–DC converters such as the boost, buck–boost, flyback, Cuk, and SEPIC are all possible options for active PFC. In the proposed design, the SEPIC converter is chosen for PFC for the following reasons: 1) it does not require a large-size high-voltage dc-link
capacitor, as in the boost PFC case; 2) unlike the Discontinuous conduction- mode (DCM) operating boost converter, the dc-link capacitor of the SEPIC converter does not suffer from high voltage stress in order to achieve high power factor [19]; and 3) the output dc-link voltage polarity is not inverted, as in the

$$V_s(t) = V_p \sin(2\pi f_L t) \tag{1}$$

$$I_{s,\text{avg}}(t) = \frac{V_p D^2 T_s}{2L_b} \sin(2\pi f_L t) \tag{2}$$

$$P_{\text{in}} = \frac{1}{2\pi}\int_0^{2\pi} V_p \sin(2\pi f_L t) I_{s,\text{avg}}(t) d(\omega_L t) = \frac{V_p^2 d^2 T_s}{4L_b} \tag{3}$$

$$\frac{V_{\text{dc}}}{V_{\text{rect}}} = -\frac{D}{\Delta_1} = -\frac{D}{\sqrt{2L_b/RT_s}}. \tag{4}$$

buck–boost converter case, which allows simpler circuit configuration and input electromagnetic interference (EMI) filter designs [20].When the SEPIC converter operates in DCM with a fixed switching frequency, the peak of the DCM inductor
current will follow the rectified sinusoidal envelope and a loseto- unity power factor is achieved at the input. This feature

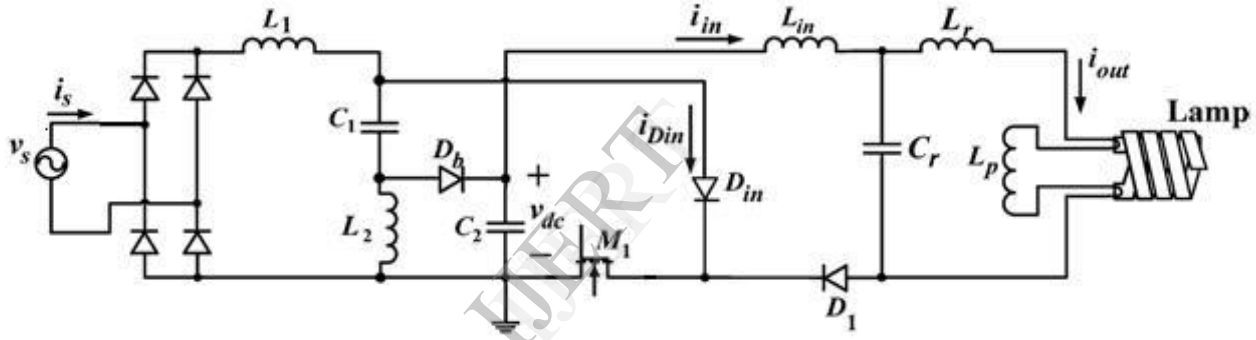


Fig. 3. Proposed single-stage single-switch electronic ballast.

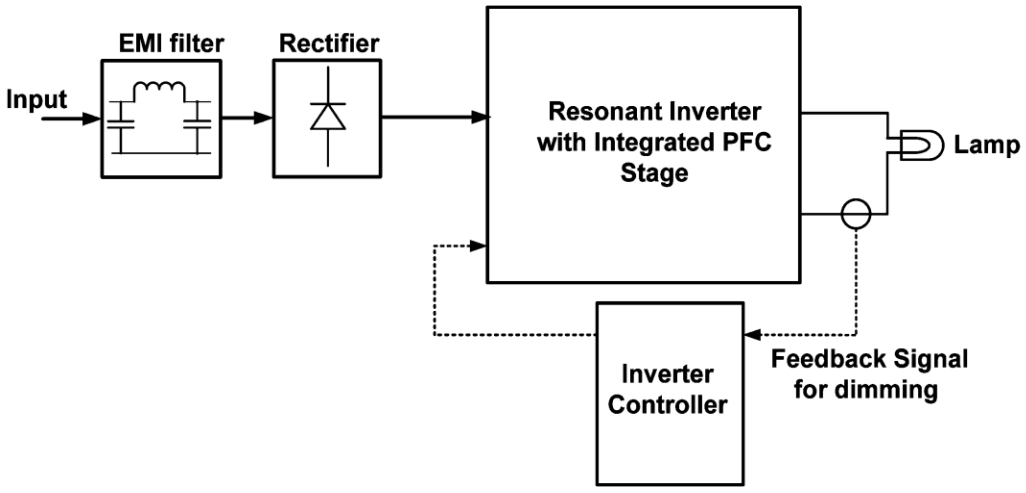


Fig. 4: Proposed Typical Electronic Ballast with Feedback signal for Dimming

can be analyzed by first examining the input line voltage. The input line voltage is given by: $v_s(t) = V_p \sin(2\pi f_L t)$, where V_p is the peak line voltage and f_L is the line frequency. Second, the average current ($i_{s,avg}(t)$) drawn from the line is given in (1), here $L_{eq} = (L_1 L_2)/(L_1 + L_2)$, T_s is the switching period, and d is the duty ratio. From (1), it can be observed that $i_{s,avg}(t)$ is purely sinusoidal and is in phase with $v_s(t)$. Therefore, a very high power factor is achieved at the input. The input average power equation is derived from (1) and is expressed as (2). Another advantage of the SEPIC converter is that the input line current ripple can be reduced by properly designing the two inductors (L_1 and L_2) and capacitor C_1 [20]. By doing so, an input LC filter can be saved in the SEPIC PFC configuration. As a result, it can be concluded that SEPIC converter is capable of achieving all the advantages of the other dc–dc converters for PFC application. Fig. 4 illustrates the finalized single-stage single-switch electronic ballast circuit that is essentially an integration of a SEPIC converter and a single-switch inverter to form a high-power-factor electronic ballast.

C. Analysis of Resonant Inverter with nth Harmonics circuit

The resonant inverter stage employs a single input inductor (L_{in}) current-source resonant inverter that consists of a resonant inductor (L_r) and a parallel capacitor (C_r) to form the corner frequency, as given in (5). The parallel inductor (L_p) is the starting inductor that provides sufficient high voltage to ignite the lamp. It also helps to reduce the circulating current in the resonant tank by providing more current to flow to the lamp at the desired switching frequency [15]. Fig. 4 shows the equivalent circuit of the resonant inverter with R_{lamp} representing the steady-state lamp resistance and r_f representing the resistance of the filament. Equation (6) gives the equation for the Q-factor of the proposed resonant circuit. By selecting high-enough Qvalue in the resonant circuit, close-to-sinusoidal waveforms are achieved at the output, and fundamental approximation can be applied [16]. The characteristics impedance (Z_o) of the resonant circuit is also defined, as in (7), to relate the quality factor and the lamp resistance

Before the lamp is ignited, the lamp resistance is infinite and the output of the resonant circuit can be modeled as an open circuit.

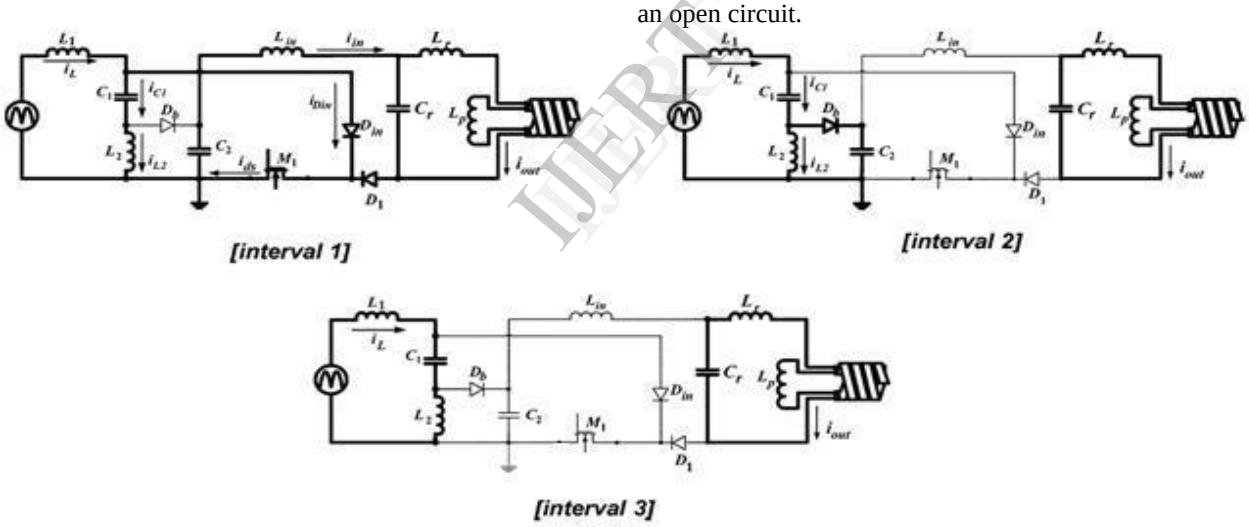


Fig. 5. Operating principles of proposed circuit.

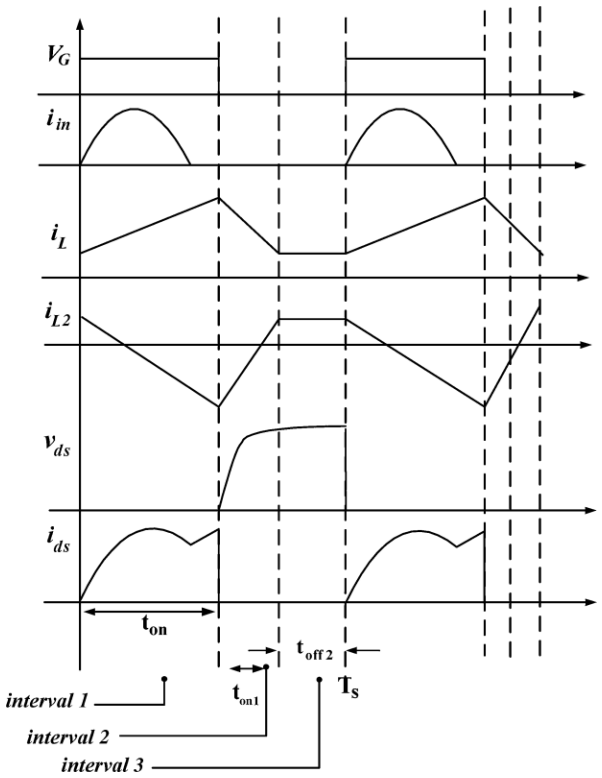


Fig. 6. Key waveforms of proposed circuit.

D. Proposed Circuit Operation

The operating stages and key waveforms of the proposed circuit are presented in this section. The circuit operating principles can be explained by examining the proposed circuit in four different intervals within a switching period, as shown in Fig. 5. The key waveforms of proposed circuit within a switching period are illustrated in Fig. 6.

Interval 1: When *M*1 is ON, *iL* rises linearly, *i*in increases slowly due to the presence of *L*in , so that close to zero-current switching is provided at the turn ON of the MOSFET. The total current flowing through the switch is *ids*, which is the sum of *i*in and *iD*in .

Interval 2: When *M*1 is OFF, *iL* decreases linearly through diode *Db* . It continues to decrease linearly until it is equal to *iL*2 , this stage ends when diode *Db* stops conducting.

Interval 3: All three diodes are OFF with the resonant circuit continuing to deliver the required energy to the output. Now, *iL* flows through both *L*1 and *L*2 . After this stage, the next switching cycle starts again.

E. Characteristics of Resonant Circuit

The basic characteristics that define the resonant circuit are provided in this section. The corner frequency (*fo*) and the quality factor (*Q*) are defined as (26) and (27), respectively

$$f_o = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{5}$$

$$Q = \frac{\omega_o L_r}{R_{\text{lamp}}} \tag{6}$$

$$Z_o = \sqrt{\frac{L_r}{C_r}} = Q R_{\text{lamp}}. \tag{7}$$

During the lamp preheat stage, the lamp resistance is infinite and the resonant circuit becomes a parallel *L*–*C* network. The preheat frequency during this phase is given by (28), where *i*pre is the preheat current. The preheat voltage is given by (29)

$$i_{\text{sn},1}(t) = I_{\text{sn}} \sin(2\pi f_{\text{ph}} t). \tag{8}$$

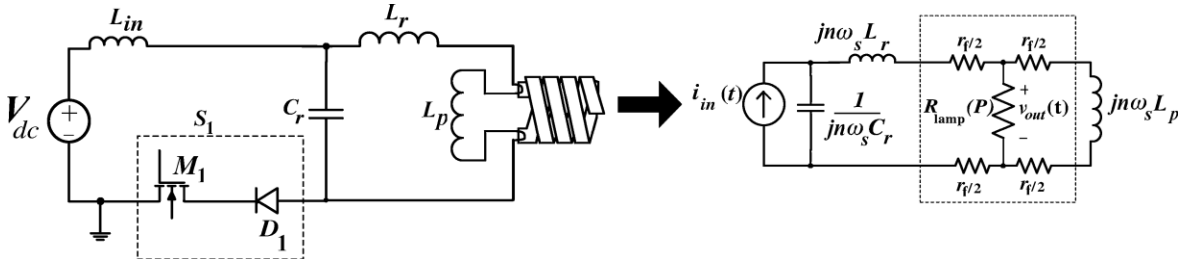


Fig. 7. Equivalent ballast circuit for fundamental analysis.

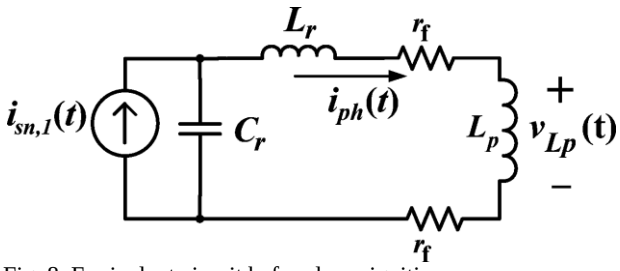


Fig. 8. Equivalent circuit before lamp ignition.

During lamp ignition, the load can still be treated as an open circuit at the output of the resonant circuit. The lamp ignition frequency (f_{ign}) is then derived using (29) and the final expression is given by (30), where V_{ign} is the amplitude of the lamp ignition voltage and I_{in} is the average current of i_{in}. The magnitude of the ignition voltage (V_{ign}), which is the voltage across the parallel inductor (L_p), is given by (31) in terms of the fundamental component of i_{in} . After the lamp is ignited, the lamp resistance becomes a finite value. By applying undamental approximation to the resonant circuit and assuming that the losses in the passive circuit components are negligible, the output-to-input voltage gain equation can be obtained and is plotted in Fig. 12 as a function of the relative operating switching frequency, $f_r = f_s/f_o$, where f_s is the switching frequency. Providing that L_p is designed to be much larger than L_r , it can be observed that high output voltage can be achieved and guaranteed during the lamp start-up condition.

III. CONTROLLER DESIGN

The control block diagram of the proposed ballast circuit is shown in Fig. 9. An envelope peak detector is used in the feedback circuit to first convert the output sinusoidal signal to a dc signal. A simple proportional-integral (PI) compensator is then designed to regulate the error signal between the feedback lamp current and the reference signal. The variable frequency dimmer uses the modified 555 circuit [17] as the voltage-controlled oscillator (VCO) to vary the switching frequency of the resonant inverter to adjust the output lamp power. TheVCO circuit is then built in the laboratory using discrete electronic components. Fig. 10 shows the schematic of the VCO with the components that were used in the experimental prototype. By controlling the input signal (V_{con}), the output switching frequency (f_s) is adjusted; an expression that describes the relationship between V_{con} and f_s is given by (15), where R_T and C_T are the timing resistor and capacitor, respectively. According to Fig. 10, R_a and R_T define the duty ratio of the pulses generated by the modified 555 circuit as given in (16). As mentioned earlier, the switching frequency decreases during dimming as Q lowers. Hence, the current-source-type resonant inverter provides different dimming characteristics as opposed to the one in the conventional voltage-source resonant inverter. This characteristic will be further verified with the experimental results provided in a later section.

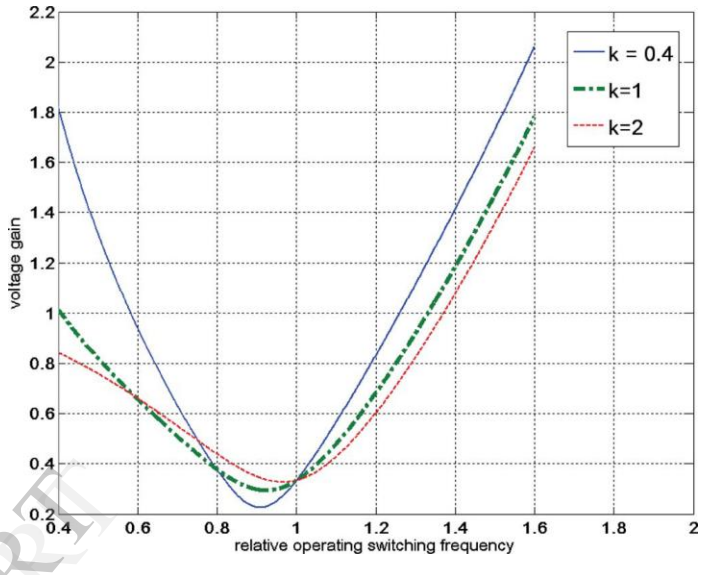


Fig. 9. Voltage gain plot for different k-values.

IV. DESIGN EXAMPLE, DIMMING, AND STABILITY ANALYSIS

A. Design Example

A 40-W CFL with a rated current of 0.4A_{rms} is chosen as the testing prototype. The design specifications are given as follows:

- corner frequency (f_o) 70 kHz;
- line voltage 110 V_{rms} 60 Hz;
- quality factor (Q) 2.0–3.0.

B. Design Procedure

1) The full-power steady-state lamp resistance is first

$$R_{\text{lamp}} = \frac{P_{\text{lamp}}}{I^2_{\text{la,rms}}} = \frac{40\ \text{W}}{(0.4\ \text{A})^2} = 250\ \Omega$$

$$L_r = \frac{R_{\text{lamp}} Q}{\omega_o} = \frac{250\ \Omega\,(2.2)}{2\pi \times 70\ \text{kHz}} = 1.2\ \text{mH}$$

$$C_r = \frac{1}{(2\pi \times 70\ \text{kHz})^2\,(1.2\ \text{mH})} = 3.9\ \text{nF}.$$

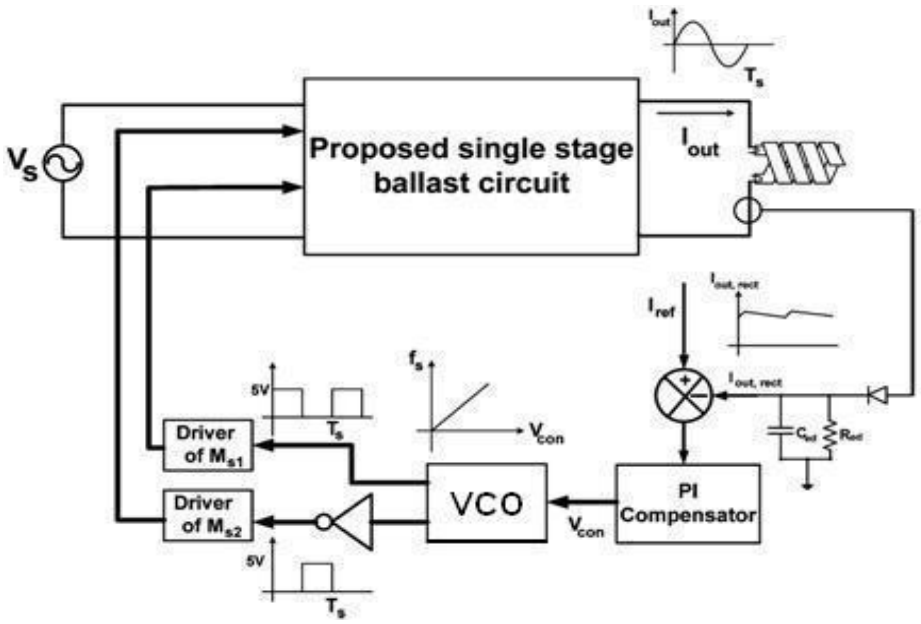


Fig. 10. Proposed closed-looped ballast system.

calculated as given by (17), where $I_{la,rms}$ is the lamp rms current. The resonant circuit components L_r and C_r are then calculated from (5) and (6), respectively, by selecting Q to be 2.2.

2) L_p is chosen according to the k -value decided from Fig. 8.

In this design, $k = 2$; hence

$$L_p = L_r k = 2.2 \text{ mH}.$$

3) The value of L_b can be calculated from (2) by substituting

$D = 0.5$, $T_s = 1/70$ kHz, and $P_{in} = 40$ W, assuming that the PFC stage efficiency (η) is 90%

$$L_b = \frac{V_p^2 D^2 T_s}{4 P_{\text{in}} \eta} = \frac{(156)^2\, 0.5^2\, (1/70\text{ kHz})}{4\,(40\text{ W})\,(0.9)} = 603.6\ \mu\text{H}.$$

4) *Lamp ignition process:* To properly start up the CFL, the switching frequency of the resonant circuit is initially set to around 45 kHz during the lamp preheat process by setting the variable resistance R_T in Fig. 10 to a lower value. Then the value of R_T is adjusted to provide an ignition frequency close to 55 kHz. The electrodes heat up at this switching frequency, and after the lamp is successfully ignited, the switching frequency continues to increase until the lamp current increases to its rated value. The maximum voltage stress ($V_{ds,max}$) across the switch during the lamp ignition phase can be calculated by noting that the peak voltage across the switch is equal to the voltage across the resonant capacitor (C_r). The relationship is given in (21), where $V_{ign} = 410$ V.

$$V_{\text{ds,max}} = V_{\text{ign}} \left(\frac{L_r}{L_p} + 1 \right) = 610 \text{ V}.$$

5) As fast recovery diodes are required in D_{s1} and D_{s2} to minimize the turn-off losses in the diodes, the model MUR1560 is used in the experimental prototype.

c. *Dimming Analysis*

The theoretical analysis during dimming is performed according to the ballast equivalent circuit shown in Fig. 4. The output voltage across the lamp from (10) is obtained again as a function of $R_{lamp}(I_{la,rms})$ and $i_{sn,1}$ as given in (28), where $R_{lamp}(I_{la,rms})$ is the lamp resistance model proposed in [21]. The switching frequency for different lamp-power conditions is then obtained by solving (28) in MATLAB and is given by (29), where A, a, b, and c are given by (30)–(33), respectively, as shown in (28), at the bottom of this page.

$$f_s(P) = \frac{1}{2\pi} \left(\sqrt{\frac{\left(-2b\sqrt[3]{A} + \sqrt[3]{A^2} - 12ac + 4\sqrt{b}\right)}{6a\sqrt[3]{A}}} \right)$$

During dimming, the lamp current decreases significantly. The parallel inductor L_p is essential to maintain a stable lamp arc across the two electrodes so that the lamp does not go off at very low dimming levels. The phasor representation of $i_{Lp}(t)$, the current that flows through inductor L_p is derived, as shown in (34) at the bottom of this page. To realize the practical dimming analysis in computer simulation, the lamp model discussed in [21] can provide better understandings of the dynamic analysis of the proposed circuit during dimming operations. with a step change in

the reference signal to dim the lamp to 10% of its full power. It is observed that a stable lamp current transition is maintained with almost the same dc bus voltage maintained during the dimming transition. The voltage across the parallel inductor is depicted in Fig. 15. It is observed that the voltage varies from 90 to 115 V_{rms} when the lamp is dimmed. This voltage level is sufficient to maintain the lamp arc during the dimming process.

V. Performance of the Proposed Circuit

A. Simulation Results

Fig.12 & 13 shows that the simulated line current at the full amp- power condition with a power factor of 0.996 is obtained.

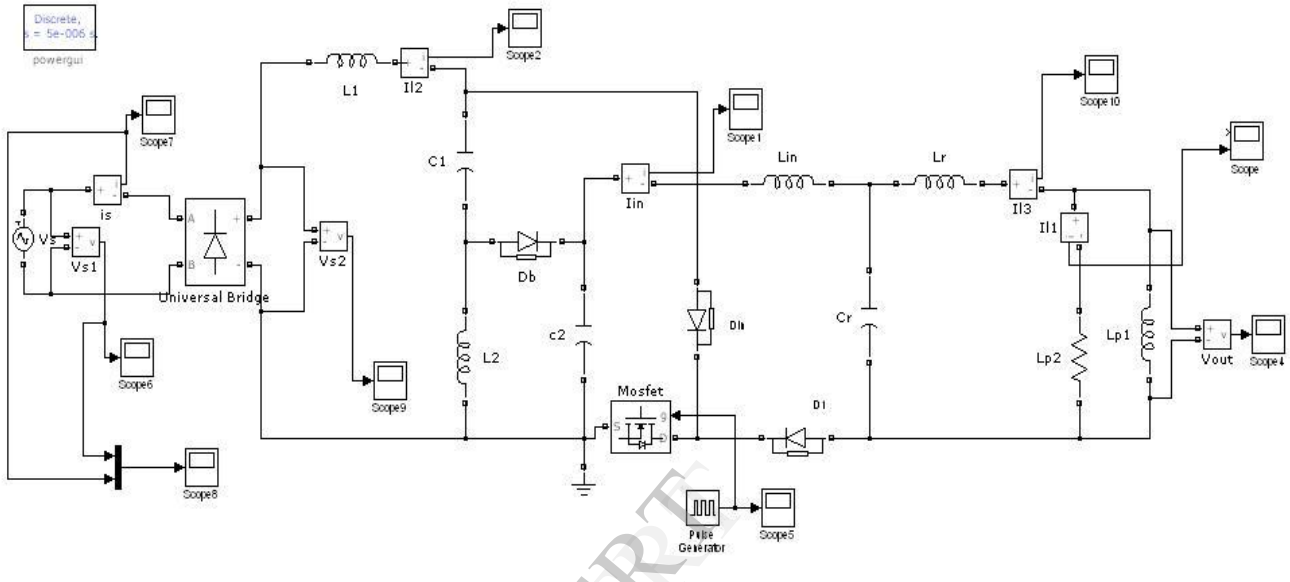
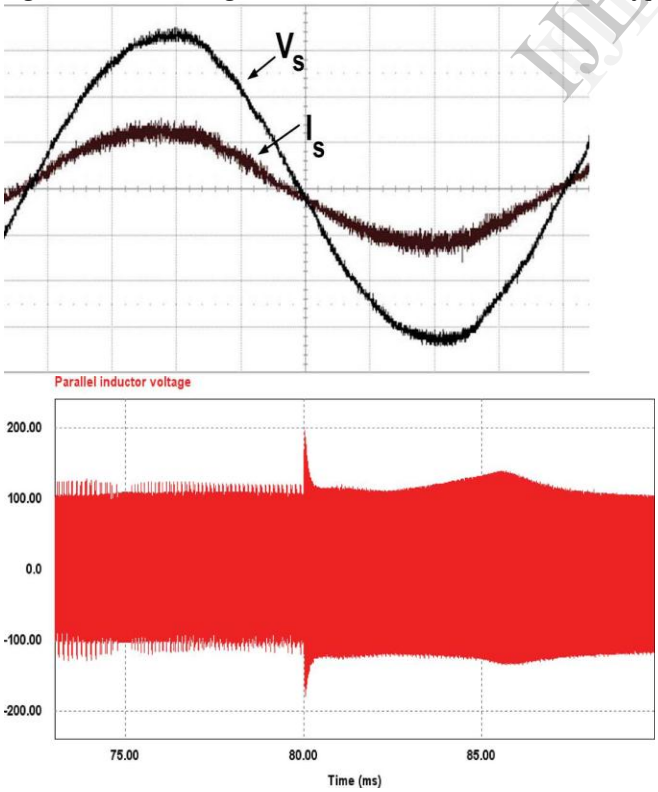
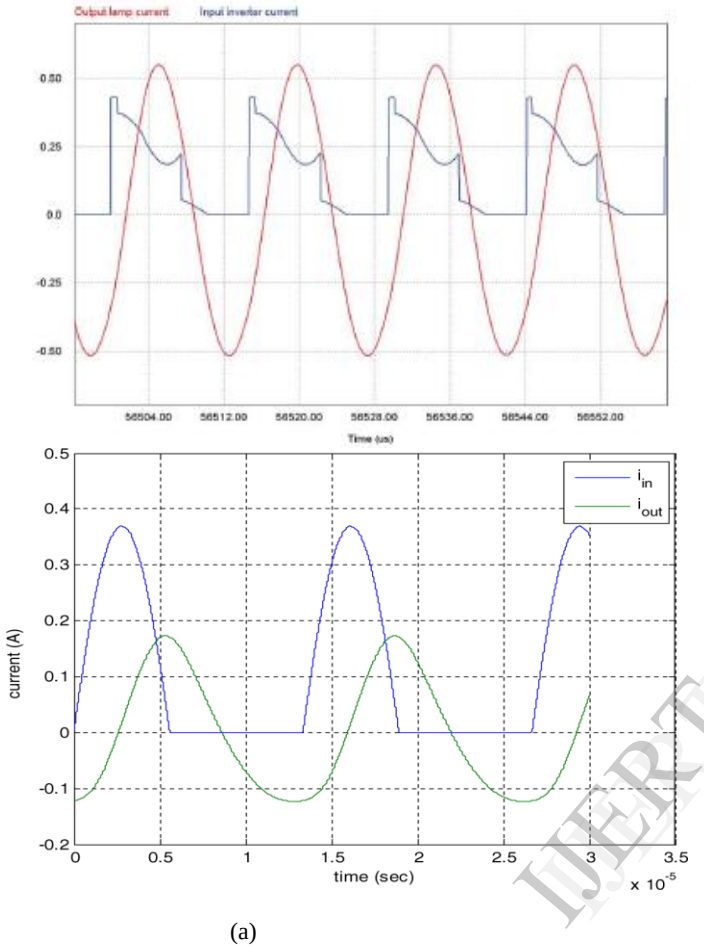


Fig.11. Electrical diagram of a MATLAB Simulated Prototype



(a) (b)

Fig. 12. (a) Measured lamp current and (b)Parallel inductor voltage waveform during dimming in Matlab



(a) (b)

Fig. 13. (a) Current waveforms at the resonant inverter stage plotted in MATLAB. (b) Simulated output current

Fig. 16(b) shows the output lamp current and the resonant inverter input-current waveforms. All these waveforms have good agreement with the predicted waveforms analyzed in Section II.

B. Experimental Results

Fig. 12 shows the measured line current and voltage from a commercial 40-W CFL. The power factor obtained is 0.62. Fig. 13(b) shows the input line current of the proposed circuit and a power factor of 0.992 is achieved. Fig. 14 illustrates the lamp voltage transition during the lamp ignition process. Fig. 15 shows the dc-link capacitor voltage and output lamp current. The crest factor of the lamp current is measured to be 1.59, which is below the limit, according to the ANSI standards [22]. Fig. 16 shows the steady state output lamp current.

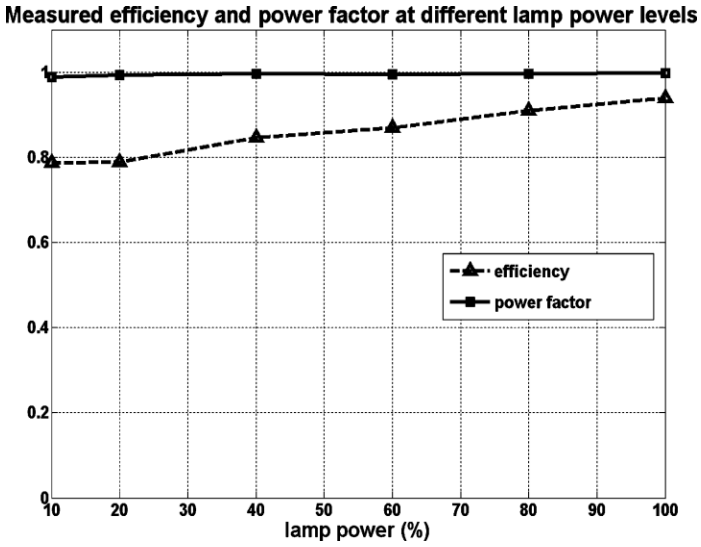


Fig. 14. Measured efficiency and power factor.

The current and voltage waveforms across the MOSFET are illustrated shows the MOSFET current and voltage waveforms within the two line frequency cycles. It is observed that the peak voltage across the MOSFET and the peak current flowing through the MOSFET is approximately 350 V and 0.85 A, respectively. The measured peak voltage and current values are close to the calculated values obtained in the previous section. Fig. 14 illustrates the power factor and efficiency performance for the proposed circuit under different line voltages. It is observed that a power factor of at least 0.98 is maintained under all operating conditions. The overall efficiency is measured to be approximately 90% at the rated voltage. The majority of the power loss is due to the turn- OFF switching loss of the MOSFET and the copper losses in the inductors.

IV. CONCLUSION

In this paper, Single-stage single-switch Dimmable electronic ballast with very high power factor (>0.995) and high efficiency (90.8%) has been introduced for CFL applications. Small-signal analysis has been presented and a simple-variable-frequency controller has been developed. Due to its single-switch characteristics, both the semiconductor complexity level and the MOSFET driver design are greatly simplified compared to the existing solutions. Detailed operating principles and the features of the proposed circuit have been provided in this paper. Simulation waveforms have been provided to highlight the merits of the proposed circuit for a 40-W compact fluorescent lamp.

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