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Analysis of Asymmetrical Cascaded 7 Level and 9 Level Multilevel Inverter Design for Asynchronous Motor

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***Abstract*- This paper proposes comparison between Asymmetrical Cascaded 7 level and 9 level Multilevel Inverter (MLI) using multicarrier based Level shift Pulse Width Modulation Technique (LSPWM) with induction motor load. This control scheme is applied to 7 level and 9 level Asymmetrical Cascaded Multilevel Inverter (CMLI). Different topologies of multilevel inverter have been reported in the literature, but this work mainly focuses on the asymmetrical cascaded multilevel inverter circuit with reduced number of input DC sources. Here PWM switching techniques for Asymmetrical cascaded multilevel inverters is Phase disposition (PD) . THD and motor output are analyzed in FFT window. The results are observed by MATLAB/SIMULINK software**.

***keywords*- Asymmetrical CMLI, LSPWM, THD, PD, IGBT and Asynchronous motor.**

1. INTRODUCTION

In recent era there is huge power requirement in industries and other areas. Multilevel inverter has become popular to fulfill power requirement[1] due to advantage of high power quality waveforms, low electromagnetic compatibility. Inverter is a device that converts electrical power from DC to AC form using electronic circuits. Generally simple inverter gives 2 or 3 level output voltage .Multilevel inverter gives 3 or more output voltage levels. It produces a stepped output voltage with reduced harmonic distortion when compared to a 2 level inverter. Multilevel inverter are basically 3 types[2]

- Diode clamped inverter
- Flying capacitor inverter
- Cascaded inverter

The most commonly efficient inverter is cascaded multilevel inverter. It provides higher output voltage and power levels. It is one of the methods used for drive application which meet the requirements such as high power rating with reduced THD and switching losses. The Asymmetric Multilevel Inverter increases the number of levels in the output and reduces the number of input DC sources required[3]. IGBT is used as semiconductor switch for designing the inverter circuit. It has the high power rating, less conduction loss and less switching loss.

DC sources are basically two types which are Asymmetrical DC source and symmetrical DC source. Asymmetric DC source has unequal magnitude of voltage whereas symmetric DC source has equal magnitude of voltage. Asymmetrical cascaded MLI has less number of DC source voltage and switches as compared to symmetrical cascaded MLI. The advantage of an asymmetric cascaded has an increased number of voltage levels for a given module counts. The comparison between asymmetrical cascaded 9 level MLI and 7 level MLI were done and based on the results obtained the most effective MLI is adopted that gives the reduced THD output and better performance for the single phase induction motor load.

2. ASYMMETRICAL CASCADED MLI

In Asymmetric Cascaded Multilevel Inverter, DC sources of unequal magnitude of voltage are used. Here 7 level and 9 level Asymmetric Cascaded MLI is analyzed[4]. In case of 7 level Asymmetric Cascaded MLI two unequal magnitude DC sources and 8 power switches are used. In case of 9 level Asymmetric Cascaded MLI three DC sources are used having 2 same and third different and 12

power switches are used. The basic modal circuit for 7 level and 9 level Asymmetric Cascaded MLI are shown in fig 1 and 2 respectively.

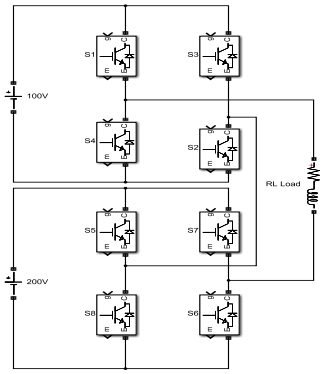

Fig 1 Asymmetrical seven level inverter

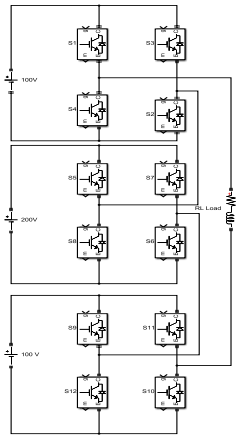

Fig 2 Asymmetrical nine level inverter

3. OPERATION OF CASCADED 9 LEVEL TOPOLOGY

The Asymmetrical cascaded 9 level multilevel inverter has three DC sources and twelve power switches magnitude of DC sources are 100V, 200V and 100V respectively. The sources are connected to three H-Bridge units which are cascaded in single phase. In an individual H-bridge the output voltage is $+V_{DC}$, 0 or $-V_{DC.}$ Hence the desired output voltage for 9 level Asymmetric CMLI are $+4V_{DC}$, $+3V_{DC,}$ $+2V_{DC,}$ $+V_{DC}$, 0, $-V_{DC,}$ $-2V_{DC}$, $-3V_{DC,}$ $-4V_{DC.}$

To get the desired output voltage the power switches are turned ON and OFF. By making the proper combination of switches we get the desired output voltage.To get maximum output voltage +4V; the switches S1, S10, S9, S6, S5 AND S2 are ON and remaining switches are OFF at this time. For +3V; the switches S1, S10, S12, S6, S5and S2 are ON and remaining are OFF. Similarly all voltage levels can be analyzed by see the table given below Table number 1.

Table no. 1 Switching pattern for asymmetrical cascaded nine level inverter

Output	4V	3V	2V	V	0	-V	-2V	-3V	-4V
S1	1	1	0	1	0	0	0	0	0
S2	1	1	1	1	0	0	1	0	0
S3	0	0	0	0	0	1	0	1	1
S4	0	0	1	0	0	1	1	1	1
S5	1	1	1	0	0	0	0	0	0
S6	1	1	1	1	0	1	0	0	0
S7	0	0	0	0	0	0	1	1	1
S8	0	0	0	1	0	1	1	1	1
S9	1	0	0	0	0	0	0	0	0
S10	1	1	1	1	0	1	1	1	0
S11	0	0	0	0	0	0	0	0	1
S12	0	1	1	1	0	1	1	1	1

4. MODULATION TECHNIQUE

Multilevel inverter has to synthesize a staircase waveform by using the modulation technique to have controlled output voltage. There are variety of modulation techniques available. Basically the control technique can be classified as the pulse width modulation which is considered as the most efficient method. In this inverter, level shifted pulse width modulation[5] used.

Here we are using phase disposition (PD) modulation technique. The reference signal has 50 HZ frequency and carrier waves have 2KHZ to 3KHZ frequency. Here we uses triangle generator for the purpose of carrier wave. The modulation index is 0.97. The formula used for MI is

$$\text{Modulation index} = V_{ref}/V_{car}$$

Where V_{ref} is reference voltage and V_{car} is carrier

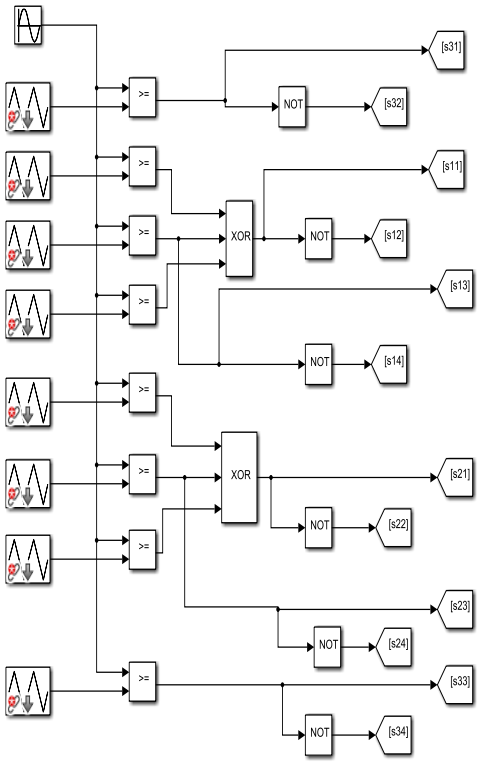

Fig 3: Simulation Control circuit of asymmetrical cascaded 9 level inverter

The complete gate pulses which are generated from above model is shown in fig 5 which is shown below.

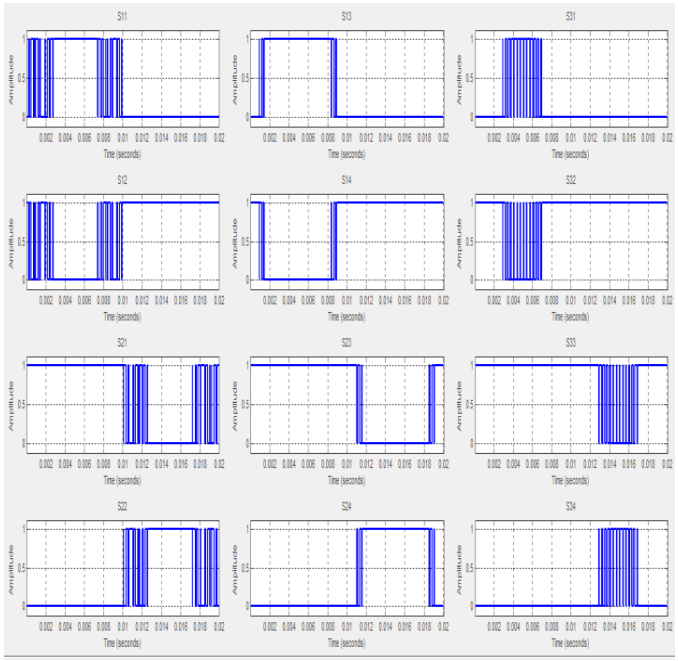

Fig 5: Complete gate signal for 9 level MLI using PD PWM Strategy

5. IMPLEMENTATION IN MATLAB

The complete result are observed in MATLAB/SIMULINK, the reference and carrier wave for PD CLPWM is shown in fig 4.

The complete simulation circuit for Asymmetric 7 and 9 level MLI with an induction motor are shown in fig 6 and fig 7.

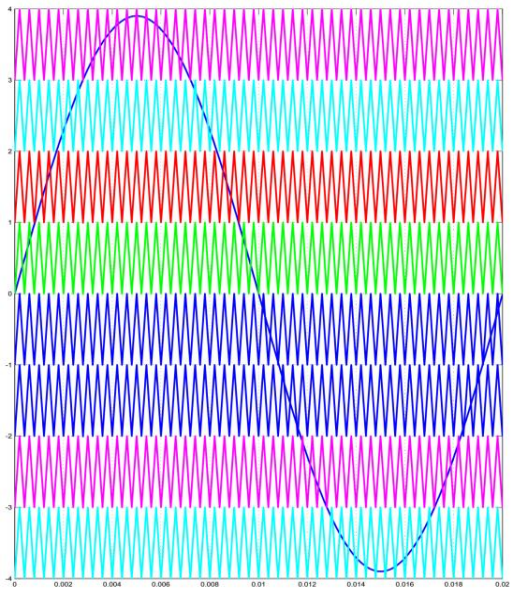

Fig 4: Reference and carrier waveform for PD 9 level MLI

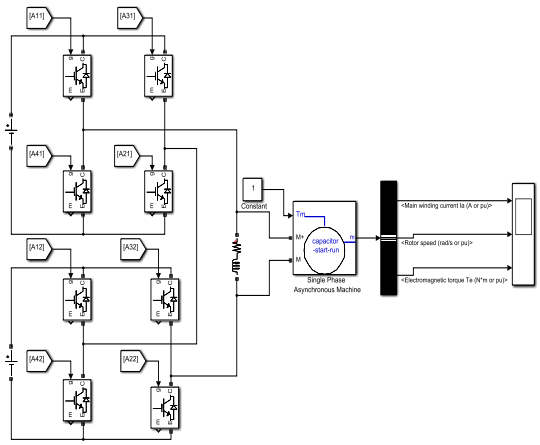

Fig 6. Simulation of asymmetrical seven level inverter circuit with induction motor load

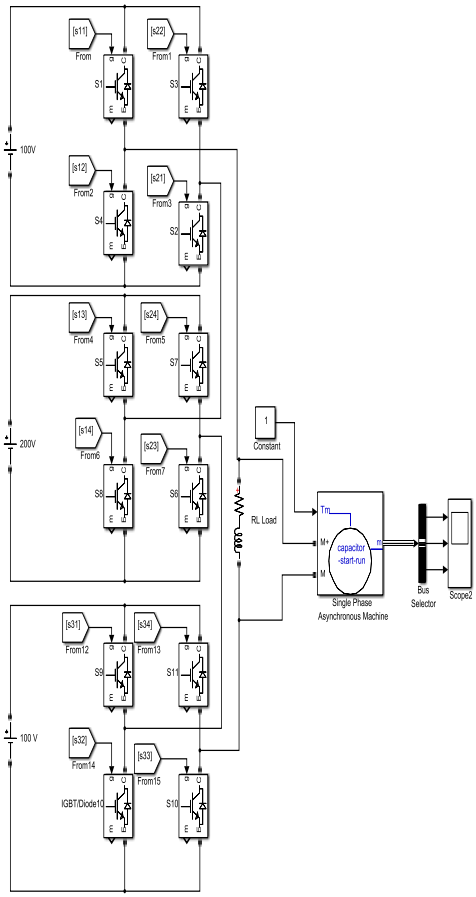

Fig 7: Simulation of Asymmetrical nine level inverter circuit with induction motor load

6. SIMULATION RESULTS

The performance analysis has been carried using a single phase induction motor and asymmetric inverter has been used for analysis. The parameters of the motor are specified in Table number 2.

Table no. 2 Switching pattern for asymmetrical cascaded nine level inverter

Parameter	Value
Voltage (V)	220
Frequency (Hz)	50
No. of pole pairs	2
Speed (rad/sec)	156

The output voltage waveform and phase current of seven level Asymmetric cascaded MLI with capacitor start-run induction motor load for 4 cycles is shown in fig.6. and its FFT analysis is shown in fig.8. The same waveform of nine level asymmetric cascaded MLI with capacitor start-run induction motor load for 4 cycles is shown in fig.7. and its FFT analysis is shown in fig.9.

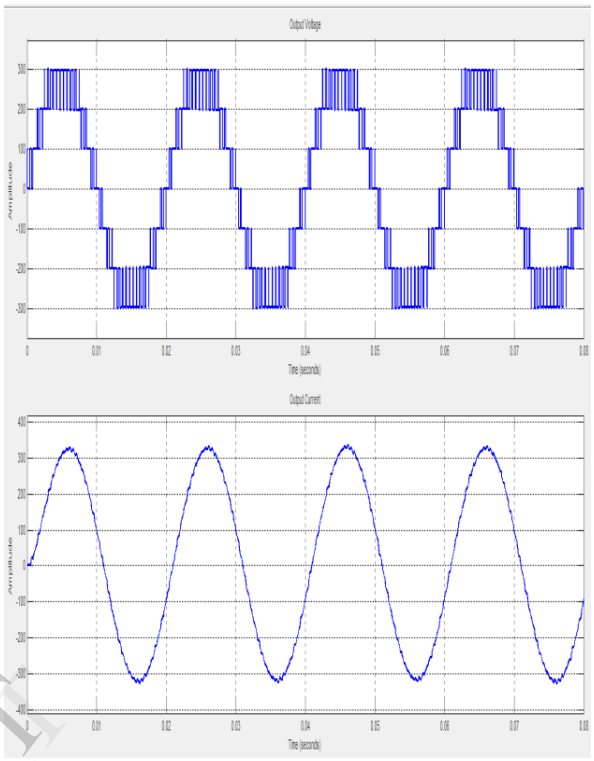

Fig 6. Output voltage and phase current of asymmetrical seven level multilevel inverter

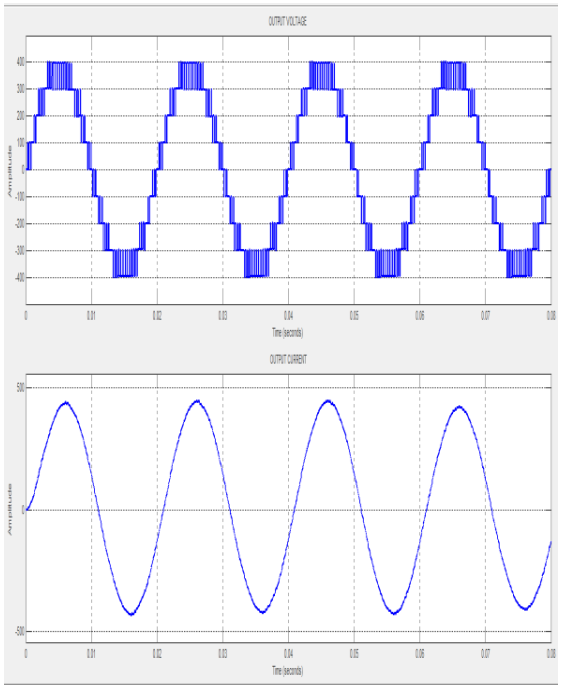

Fig 7. Output voltage and phase current of asymmetrical nine level multilevel inverter

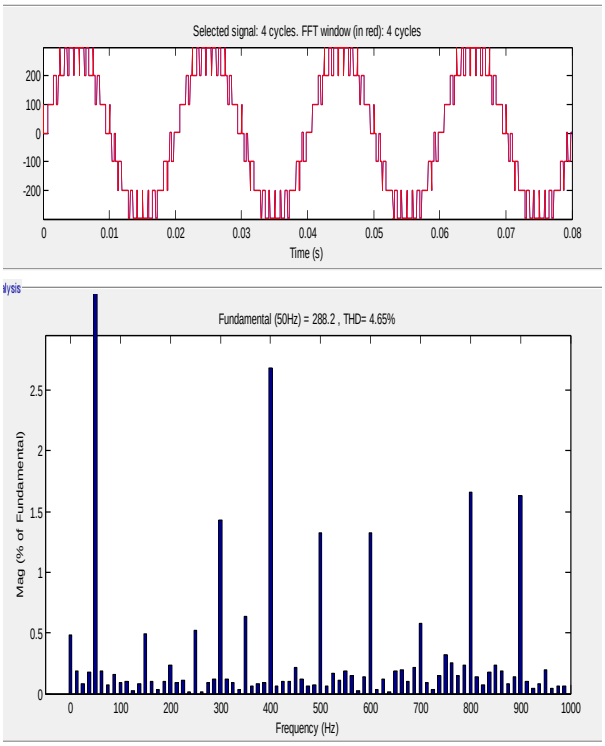

Fig 8: FFT analysis of voltage waveform of Asymmetric 7 level CMLI

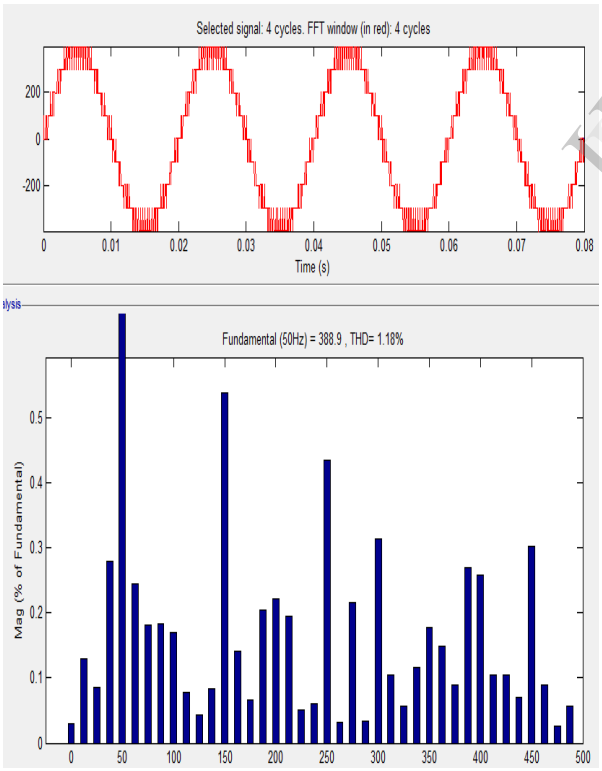

Fig 8: FFT analysis of voltage waveform of Asymmetric 9 level CMLI

Without LC filter the harmonics are eliminated to optimum level and therefore reduced the THD of the output voltage in case of 9 level asymmetrical cascade MLI.

The main winding current, speed and Torque of the induction motor at 0.3 sec for 7 level asymmetric cascaded MLI is shown in fig.9. The main winding current, speed and Torque of the induction motor at 0.3sec for 9 level asymmetric cascaded MLI is shown in fig.10.

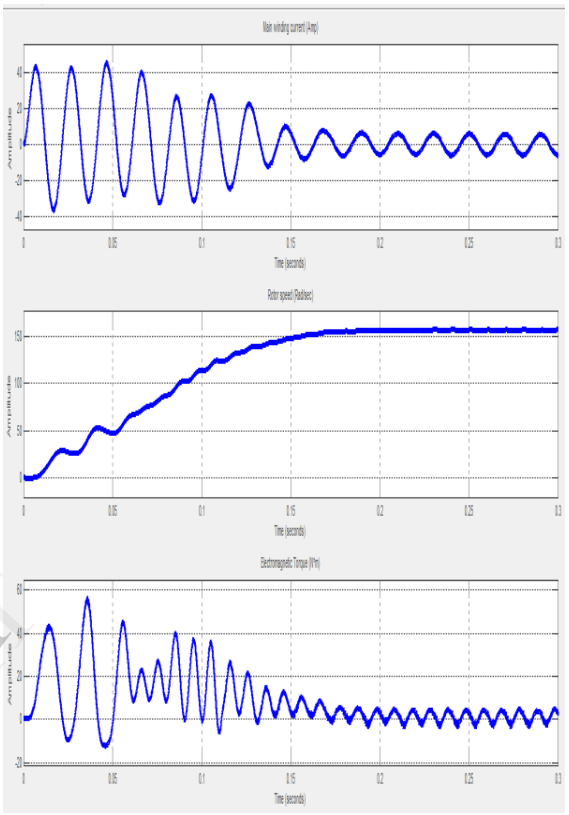

Fig 9: Motor output of Asymmetric cascaded 7 level MLI

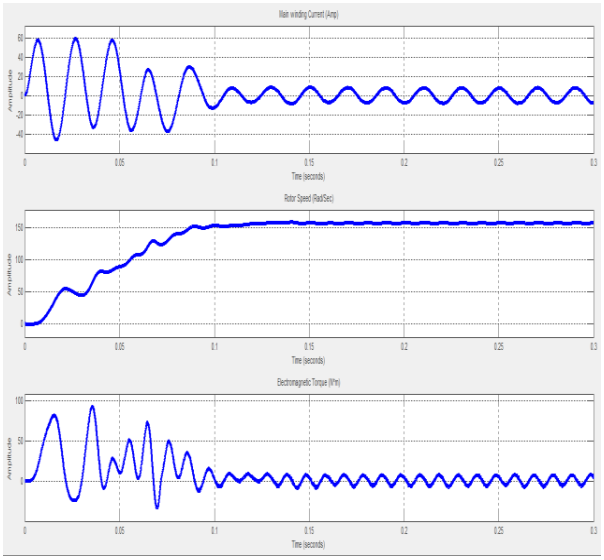

Fig 10: Motor output of Asymmetric cascaded 9 level MLI

The steady state value and THD of the output voltage of 7 level asymmetric cascaded MLI is compared with the same output waveform of 9 level asymmetric cascaded MLI is shown in Table no.3. The variation of motor parameter of 7 level asymmetric cascaded MLI is compared with the 9 level asymmetric cascaded MLI is shown in Table no.4.

Table no. 3: Steady state value for Induction Motor

MLI	Main winding current	Rotor Speed	Electromagnetic Torque	THD
7 Level	0.18 sec	0.2 sec	0.18sec	4.65 %
9 Level	0.13 sec	0.15 sec	0.13 sec	1.18%

Table no. 4: Variation of Induction Motor Parameters

MLI	Main winding current (Amp)	Rotor speed (rad /sec)	Electromagnetic Torque (Nm)
7 Level	+7 to -7	153	+5 to -3
9 Level	+8 to -8	158	+7 to -7

All simulation results are shown in above table no. 3 and table no. 4 respectively.

7. CONCLUSION

The paper deals with a comparison of cascaded 7 level and 9 level multilevel inverter for Asynchronous motor. Indeed, asymmetrical 7 level and 9 level multilevel inverter have been compared in order to find an optimum motor speed, torque and main winding current with lower switching losses, Total harmonic distortion and optimized output voltage quality. The steady state condition of motor output has reached earlier in case of asymmetrical cascaded 9 level inverter as compared to 7 level MLI. The simulation result shows that the asymmetrical 9 level multilevel inverter provides nearly sinusoidal output voltage with reduced Total harmonic distortion and optimized motor output. In addition asymmetrical 9 level multilevel inverter has less switching losses with improved output voltage quality.

8. REFERENCES

1. Rashid, M. H, 2004. "Power electronics: Circuits, devices and applications". Third Edition, Prentice Hall.
2. J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel Inverters: A survey of topologies, controls and applications," Industrial Electronics, IEEE Trans. Ind. Electronics, Volume 49, no. 4, pp. 724-738, 2002.
3. Ebrahim Babaei, 2008, "A Cascaded Multilevel Converter Topology with Reduced number of Switches" IEEE Transactions on power electronics, Vol. 23, No. 6.
4. Bharath. K, R. J. Satputaley, "Single phase Asymmetrical Cascaded Multilevel Inverter Design for Induction Motor," ASAR International Conference, ISBN: 978-81-927147-0-7.
5. K. Radha Sree, Sivapathi, Vardhaman. V, and Dr. R. Seyezhai, "Asymmetric Cascaded Multilevel Inverter for Electric Vehicles," IEEE-ICAESM-2012.
6. P. Satheesh Kumar, Dr S. P. Natrajan, Dr. Alamelu Nachiappan, Dr. B. Shanthi, "Performance Evaluation of Nine Level Modified CHB Multilevel Inverter for Various PWM Strategies," IJMER, Vol. 3. Issue. 5, Sept-Oct. 2013 pp-2758-2766.