Analysis of Dynamic Logic for SET

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***Abstract*— Dynamic logic circuits are appealing to use in circuit design because they are generally smaller and faster than static circuits .Compared with static logic, the dynamic logic requires fewer transistors to implement a given logic function and can offer considerable faster switching speeds and play important role in the design of many applications such as microprocessors, digital signal processors and dynamic memory High-speed integrated circuits frequently utilize dynamic logic circuitry to realize faster and smaller designs than corresponding static CMOS logic circuits. The use of these circuits in space is desirable, but not much work has been performed in assessing their vulnerability to ionizing particles present in the space environment. Single-event transients (SETs), or glitches that originate in logic circuits, are one of the most important categories of soft errors. The charge required to store (or potentially disturb) a digital logic signal decreases as feature sizes in advanced devices decrease. As a result, the soft- error rate has become a significant reliability issue for highly scaled technologies. Radiation-induced single event upsets (SEUs) pose a major challenge for the design of memories and logic circuits in high performance microprocessors. This paper presents study of effects of SET on dynamic logic circuits and the three SET hardened dynamic logic circuits proposed in [12].Simulation is carried out using one basic dynamic logic circuit and the results confirm that the proposed three schemes mitigate SET's efficiently.**

Keywords—Single-event transients (SETs), dynamic logic circuits, static CMOS logic circuits

I. INTRODUCTION

In integrated circuit design, dynamic logic (or clocked logic) is a design methodology in combinatorial logic circuits, particularly those implemented in MOS technology. It is distinguished from the so-called static logic by exploiting temporary storage of information in stray and gate capacitances. It was popular in the 1970s and has seen a recent resurgence in the design of high speed digital electronics, particularly computer CPUs. Dynamic logic circuits are usually faster than static counterparts, and require less surface area, but are more difficult to design, and have higher power dissipation. Dynamic logic is distinguished from so-called static logic in that dynamic logic uses a clock signal in its implementation of combinational logic circuits [1] .

Electronic circuits encode information in the form of a charge stored on a circuit node or as a current flowing between two circuit nodes. For example, one bit of static memory contains two nodes that store two complementary charges corresponding to logic ―1‖ and logic ―0.‖ The bit values ―1‖ and ―0‖ can be stored as node charges ―10‖ and ―01,‖ respectively. Technology scaling has achieved an increase of the operating velocity, extraordinary integration density, supply voltage reduction and parasitic node capacitances decrease with the advance of each generation. However, technology scaling worsens some adverse effects on present and future technologies, like the impact of single event transients (SETs) on the circuit behavior. An SET consists in the production of a voltage transient at a combinational circuit node caused by the strike of an ionizing particle that deposits an amount of charge at the node parasitic capacitance Such perturbation can propagate within the combinational block and eventually reach a memory element that might erroneously change its stored value because of the SET.

DSETs are momentary voltage or current disturbances that, although they don't cause an upset in the circuit actually struck by an energetic particle, may propagate through subsequent circuitry and eventually cause an SEU when they reach a latch or other memory element.[3]. Extensive research work is being carried out to mitigate the effects of SETs on dynamic logic circuits. Here we present a review of effects of SET considering one basic dynamic logic circuits and a study has been done on one of the scheme prososed to mitigate SET.

II. DYNAMIC LOGIC

Dynamic logic circuits are appealing to use in circuit design because they are generally smaller and faster than static circuits [14]. A dynamic logic gate replaces the PMOS block of static gates with a single PMOS transistor and an extra NMOS ―foot‖. Removing the PMOS block reduces the capacitance on the output node as well as reducing the loading of inputs. This allows the circuit to operate at higher clock frequencies.

TABLE 1. DYNAMIC LOGIC COMPARED TO STATIC LOGIC [14]

Area	Speed	Power	Noise
Smaller	Faster	Increased Usage	Increased Sensitivity

A. Maintaining the Integrity of the Specifications

Fig. 1 is a typical dynamic logic circuit including PMOS P1, NMOS N1 and a pull down network. The dynamic logic circuit operates in two states referred to as the precharge phase and the evaluation phase. The precharge phase occurs when the clock signal CLK is logic 0 and the evaluation phase occurs when CLK is logic 1. In the precharge phase, P1 is on and N1 is off.

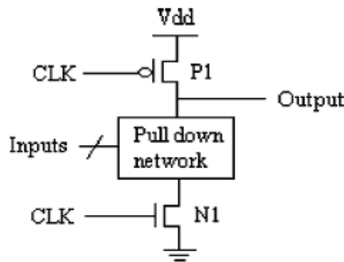


Fig. 1. Dynamic logic.[12]

The current flows from the source of P1 to the drain of P1 until the output is logic 1.In the evaluation phase, N1 is on and P1 is off. The output either remains at logic 1 or becomes logic 0 depending on the state of the pull down network. If the pull down network allows current flow towards ground, the output becomes logic 0.Otherwise the output remains at logic 1.Therefore,the pull down network consisting of two NMOS transistors in series implements a NAND function and the pull down network consisting of two NMOS transistors in parallel implements a NOR function.

A dynamic NAND gate is shown in Fig. 2(a).

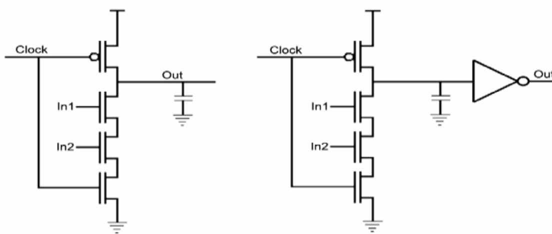


Fig. 2. Example of (a) dynamic NAND, (b) domino AND [15]

When the clock is logically LOW, the gate is in the precharge mode of operation and the capacitance associated with the output node is charged to Vdd. As the clock goes to a logic level HIGH, the gate transitions to the evaluate mode of operation where the output may then float HIGH or conditionally discharge. Floating nodes are more vulnerable to noise because they cannot easily recover once charge has been lost. Dynamic circuit inputs must satisfy the monotonicity constraint. An input cannot start HIGH and fall LOW during evaluate because charge may be lost on a floating node before the device turns off. A standard domino gate solves the monotonicty problem by adding an inverter to the output as in Fig. 2(b). Single Event Transient (SET)

As technologies scale down in size, the use of integrated circuits (ICs) in space environment presents a large number of challenges that arise from the increased susceptibility to soft errors . One of the major sources of soft errors is single event transients (SETs), which may be induced when an ion strikes the sensitive region of an IC [13]. The creation of soft errors due to the propagation of single event transients (SETs) is a significant reliability challenge in modern CMOS logic. The proper functioning of electronic equipment in radiation-rich environments may be limited by their vulnerability to single- event effects (SEEs). This can result in erroneous data, system shutdown, or even catastrophic failure.[18]

The first observation of single event transients (SETs) appeared in the 80's with the development and qualification of microprocessors and integrated circuits (ICs) for space applications At that time, SET issues were identified and sporadically addressed; however, they only became a commonplace problem at the end of the 90's with technology scaling to deep submicron dimensions , when the speed and complexity of new generation circuits reached the 100-MHz and the million-gate-per-circuit era. The occurrence of SETs and the propensity for propagation is enhanced as geometric dimension and capacitance scale down, while the probability of SET capture grows with increasing circuit operational frequency

B. SET basic Mechanism

Set Generation and Propagation--When a charged particle passes through a reverse-biased junction it results in a transient current and thus charge collection at the struck electric node. In a memory cell, if the collected charge is sufficient, it may result in a cell upset, i.e., a single event upset (SEU). This SET may propagate and induce an error in a memory element (typically a flip-flop) if the following four conditions are fulfilled 1) the SET is generated at a sensitive logic node, 2) it propagates down an open logic path and arrives at a latch or other memory element, 3) it arrives with sufficient amplitude and duration to change the memory state, and 4) it arrives during the cell ―window of vulnerability‖, i.e., when the clocking condition enables the transient capture [4].

C. Particle Generation

The terrestrial radiation environment consists of >92 percent neutrons, ~4 percent pions, ~2 percent protons, and sealevel muons generated by cosmic ray interactions in the Earth's atmosphere.[16]. Charged particles create a direct ionization in semiconductor devices, causing a current surge that is responsible for errors in the memory and processing elements of a computing system. Highly abundant neutrons do not have electrical charges; their effects occur through nuclear collisions that give rise to charged particles, which in turn cause ionization. The amount of ionization and the current surge in a given semiconductor device are directly proportional to the energy lost by radiation particles. In silicon, an average energy of 3.6 eV is required to create one electron-hole pair.

a) Alpha Particles : Alpha particles are emitted by various radioisotopes undergoing radioactive decay. Metals such as lead, which is a daughter product of the naturally radioactive decaychain of uranium-238, emit alpha particles with kinetic energy in the range of 3-6 MeV. Such low-energy alpha particles have a range of 15 to 30μm in silicon and are very effective in causing single even upsets in memory. Alpha particles are also generated by (n,α) nuclear reactions induced by slow neutrons (energy range of 0.0253 to 100s of eV) in various nuclei. Elements such as natural boron used in the doping of semiconductors contain the isotope boron-10 (~20 percent), which has a very high cross-section (~5,000 barns) for (n,α) reactions . Upon absorbing a slow neutron, boron-10 splits into an alpha particle with ~1.5 MeV energy and a lithium nucleus, both capable of causing ionization with high LET.[9][16][17]

b) Radiation in Space : There is an ever-increasing interest in using commercial off the shelf (COTS) electronics in space missions, both in the aerospace industry and NASA. It is worth mentioning that the radiation environments that would be encountered by electronics in space. Space near the Earth has cosmic rays in addition to the protons and electrons trapped in the magnetic field. These cosmic rays consist of >93 percent protons, ~6 percent alpha particles, and a remainder of heavy nuclei (up to uranium) with very high energies. [9][17]

D. Impact on circuits and systems

An SEU is a transient event that lasts about 100ps . If a charge disturbance on a circuit node is smaller than the noise margin, the circuit will continue to operate properly. Otherwise, the disturbed voltage may be interpreted as the opposite logic state and the circuit will malfunction. There is a difference in the response of dynamic circuits and static circuits with and without regenerative feedback. A dynamic node is affected by the total collected charge and the change in voltage is inversely proportional to node capacitance. A static node that has a glitch will eventually recover to its original state unless there is regenerative feedback that adds to the glitch and reverses the logic state of the node.In an actively clocked circuit, an SEU on any node has a finite probability of causing a glitch that may propagate to an input of a sequential cell, get latched as a wrong value, and affect the machine operation[9],[17].

III. PRECHARGE PHASE UPSET MECHANISM

During precharge, an ion hit on the drain of an NMOS device will give rise to a transient current that could discharge the node. Because the node is still connected to Vdd through the PMOS device, it will start charging back up. If the charging does not complete before the evaluation phase begins, then an upset may occur. The node will be unable to recover until the next precharge phase. (Fig. 3).

A simulated example shown in [15] can be seen in Fig. 3 using a 130 nm technology and a transient with total deposited charge of 21.1 fC. The latch output should remain LOW (the pulses are normal for dynamic operation). A hit occurred near the end of a precharge phase that caused an upset in the next clock cycle and can be seen with the rise in the latch output voltage.

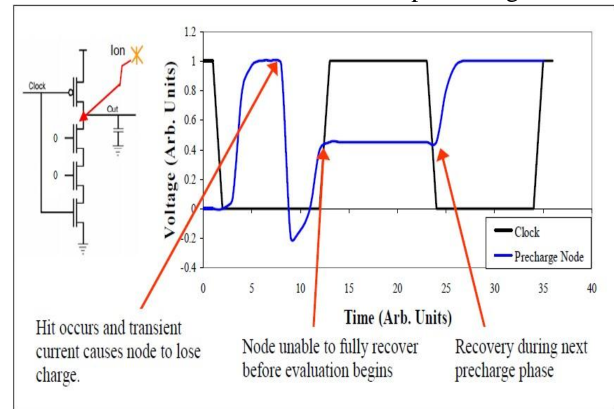


Fig. 3. Dynamic precharge transient [15]

The voltage overshoot is due to clock feedthrough. During the clock transition, the precharge device's gate-to- drain parasitic capacitance couples with the gates output allowing the voltage to rise above the rail. A window of vulnerability for the precharge upset mechanism therefore exists at the end of the precharge phase. This window ofvulnerability is the time required for the circuit to precharge up to a logic level ―1‖. Any hit occurring during this time will be unable to recover before evaluation. The window could also be considered as the minimum allowable time required for the circuit to precharge. This time will also change with inputs. For dynamic circuits, the worst-case precharge time is the time necessary to charge up the node with all other NMOS devices ―on‖ (expect the foot NMOS device). This is the time required for all internal nodes to be precharged HIGH.

IV. EVALUATION PHASE UPSET MECHANISM

Two mechanisms exist that could cause an upset in the evaluation phase of dynamic logic as a function of frequency. The first mechanism works by an N-hit causinga floating node to lose charge (Fig. 4)[15] .When the node loses charge, the voltage transient then begins propagating towards latching elements. If the transient is unable to reach a latch before the precharge phase, then an upset will not occur. Because a floating node has no active path back to Vdd, it cannot recover from charge loss until the next precharge phase. A window of invulnerability therefore exists at the end of the evaluation phase and is equal to the time needed for a transient to propagate to a latch.

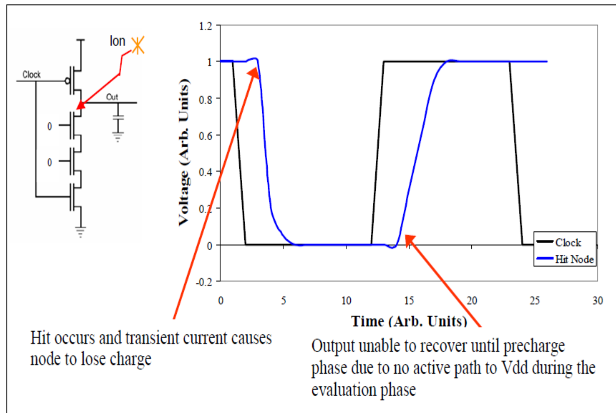


Fig. 4. Dynamic Evaluation Transient [15]

The second upset mechanism is caused by a P-hit adding charge to a node (Fig. 5) and thereby increasing the voltage on the node. Nodes that should conditionally discharge during evaluation are susceptible to this upset mechanism. A hit on the clocked PMOS device will keep a node charged for some time even if it should conditionally discharge. At higher frequencies, this delay in evaluation is long enough to cause an upset. A window of vulnerability here exists at the beginning of the evaluation phase. The window of vulnerability is equal to the time needed to discharge the hit node. Because using multiple dynamic gates requires that domino logic is used, once a node has discharged the dominos will ―begin to fall‖. After the dominos have started falling, it does not matter if the node gains charge. This is due to the fact that the gates have alreadycompleted their evaluation.

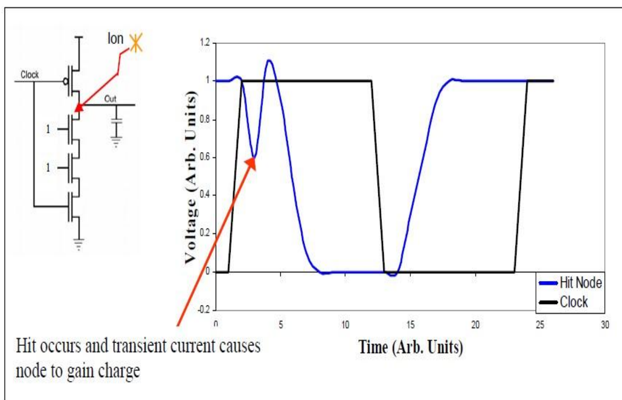


Fig. 5. Dynamic Charge Gain Transient

The circuit configuration will determine which evaluation upset mechanism will dominate. AND-like gates (gates with parallel NMOS devices) will be most vulnerable to the first evaluation upset mechanism while OR-like gates (gates with series NMOSdevices) will be most vulnerable to the second evaluation mechanism. This is becausewhen random inputs are used, an AND-like gate is less likely to discharge to ground than an OR-like gate.

V. SET TOLERANT DYNAMIC CIRCUITS

A. The first proposed SET hardened dynamic logic circuit is illustrated[12]

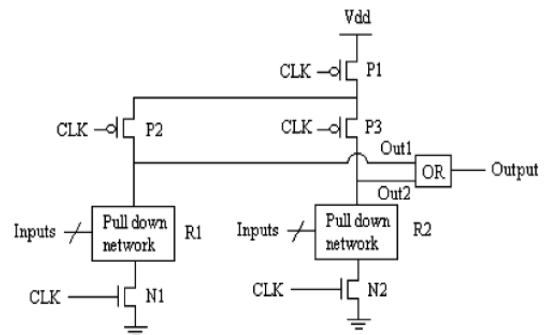


Fig. 6. First proposed SET hardened dynamic logic circuit [12]

Advantage- The hardened precharge circuit including PMOS transistors P1, P2 and P3 replaces the P1 transistor. If the output is logic 1 during the evaluation phase, an SET in R1 or R2 may cause an undesired pull-down current. So this SET may result in Out1 or Out2 being at an erroneous low voltage level But the OR gate can provide the correct output. Therefore, this dynamic logic circuit may mitigate some SETs.
Disadvantage-If two SETs occur in the pull down networks R1 and R2 sequentially during the evaluation phase, or if two SETs occur in N1 and N2 sequentially during the precharge phase, these SETs may result in Out1 and Out2 being both at an erroneous lowvoltage level. So theORgate may provide a faulty output. This problem can be solved by the second proposed SET hardened dynamic logic circuit

B. The second proposed SET hardened dynamic logic circuit[12]

Advantage - If Out1 and Out2 are both logic 1 under normal conditions during the precharge phase or the evaluation phase, PMOS T1 and T2 are turned on via inverters I1 and I2 respectively. Suppose that two SETs occur in R1 and R2 sequentially during the evaluation phase. When Out1 goes low temporarily due to a first SET, the turned on PMOS T1 supplies charge to return Out1 high. When Out2 goes low temporarily due to a second SET, the turned on PMOS T2 supplies charge to return Out2 high. Therefore, this dynamic logic circuit is hardened against SET, even in case of two sequential SETs. For the same reason, if one strike affects R1 and R2 sequentially during the evaluation phase.

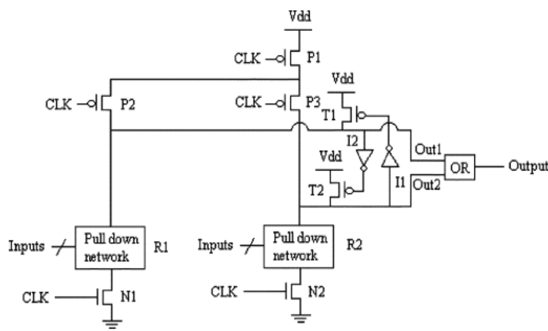


Fig. 7. second proposed SET hardened dynamic logic circuit [12]

Disadvantage- Inclusion of the inverter/PMOS circuit in Fig.results in increased power consumption when the output is transitioning from logic 1 to logic 0

C. The Third proposed SET hardened dynamic logic circuit[12]

Advantage- By connecting redundant pull down networks R1 and R2 in series, only one NMOS N1, one PMOS T1 and one inverter I1 are needed, so the third proposed scheme introduces less area overhead than the second proposed scheme.

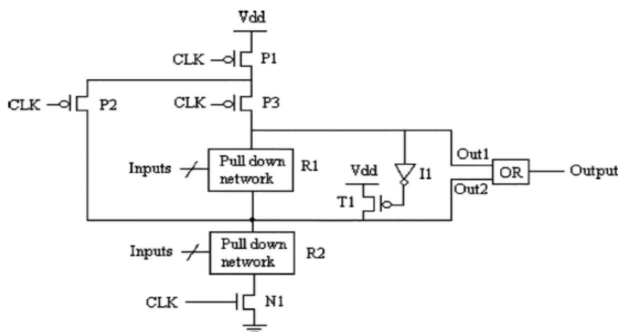


Fig. 8. Third proposed SET hardened dynamic logic circuit [12]

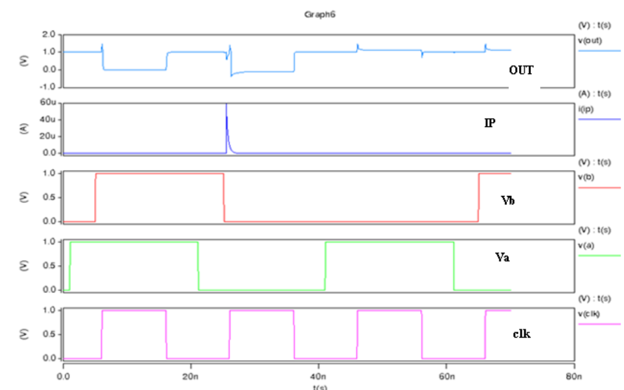
If the output is logic 0 during the evaluation phase, the transistors P1-P3 are off and an SET in P1, P2 or P3 will not induce an undesired pull-up current to impact the output of the dynamic logic circuit. Suppose that two SETs occur in R1 and R2 sequentially. The first SET in R1 will not result in Out1 being low because R2 is off. When Out2 goes low temporarily due to a second SET in R2, the turned on PMOS T1 supplies charge to return Out2 high.

Disadvantage- But due to the redundant pull down networks in series, the third proposed scheme may introduce a longer delay than the second proposed scheme.

VI. SIMULATION RESULTS

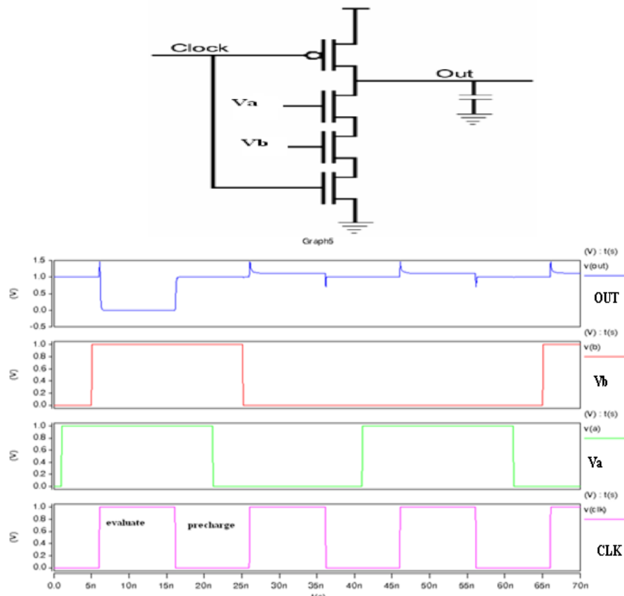
Simulations were carried out using a SPICE circuit simulator. The current induced by SET is modeled as an Exponential pulse with a specified initial value,final value , rise and fall delay time and rise and fall time constants specific for individual circuits. Following are the circuits simulated along with their ouputs and SET pulse specifications given.

A. DYNAMIC NAND WAVEFORMS WITH I/P & O/P WAVEFORMS



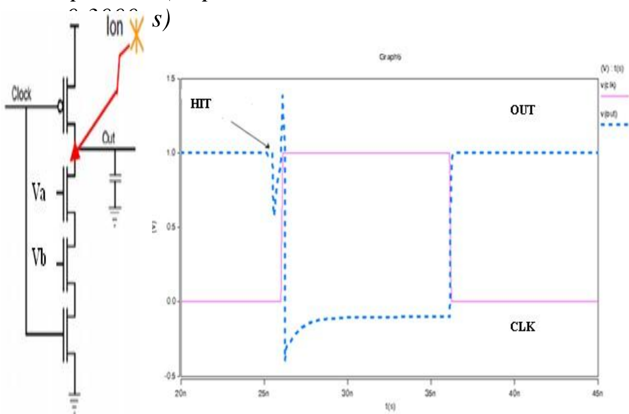
C. DYNAMIC NAND WITH SET PULSE APPLIED AT EVALUATE PHASE WITH I/P & O/P WAVEFORM

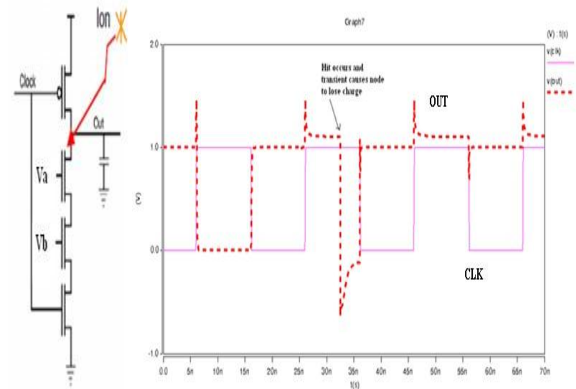
ip = EXP(0'sp' 32.505ns 0.3000ns 32.595ns 0.3000ns)

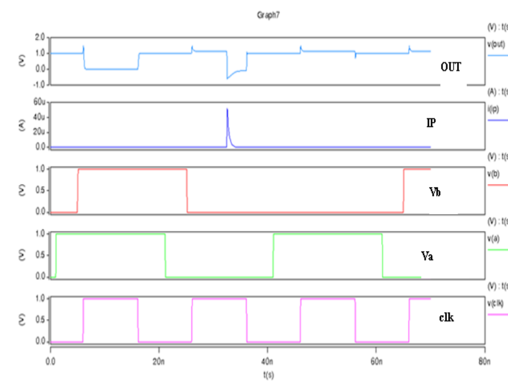


B. DYNAMIC NAND WITH SET PULSE APPLIED AT PRECHARGE PHASE WITH I/P & O/P WAVEFORMS

ip = EXP(0'sp' 25.5000ns 0.3000ns 25.5090ns 0.3000ns)

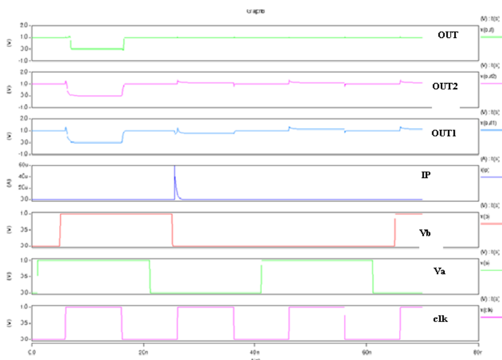




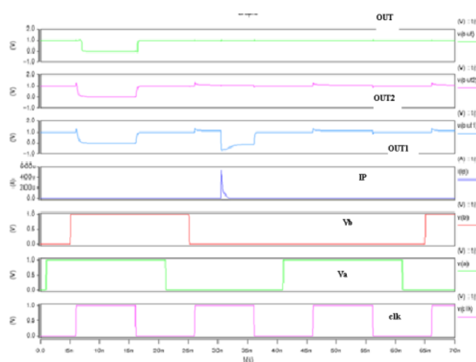


D. FIRST PROPOSED SET HARDENED DYNAMIC LOGIC CKT.[12]

a) 1 SET applied at precharge at R1 and R2 and set hardened output
ip = EXP(0'sp' 25.5000ns 0.3000ns 25.5090ns 0.3000ns)



b) 1 SET applied at evaluate and set hardened ip = EXP(0'sp' 30.505ns 0.3000ns 30.595ns 0.3000ns)

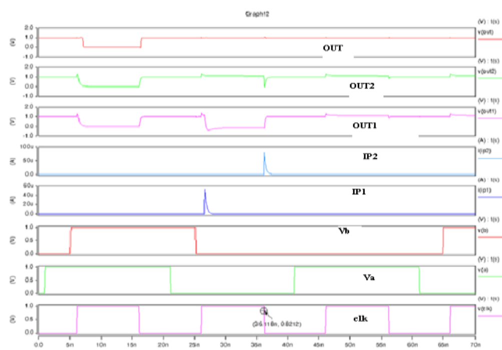


E. SECOND PROPOSED SET HARDENED DYNAMIC LOGIC CKT.[12]

2 SETs applied at evaluate in R1 and R2 and output waveforms with set hardening

ip1 OUT1 0 EXP(0'sp1' 26.505ns 0.3000ns 26.595ns 0.3000ns)

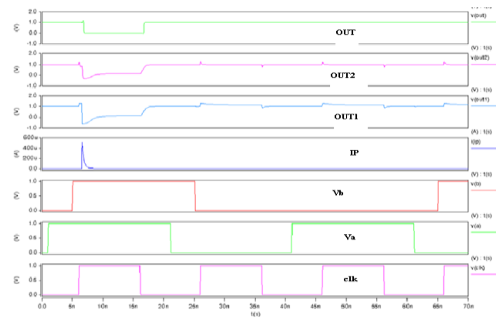
ip2 OUT2 0 EXP(0'sp2' 36.028ns 0.3000ns 36.118ns 0.3000ns)



F. THIRD PROPOSED SET HARDENED DYNAMIC LOGIC CKT.[12]

1SET applied at evaluate when o/p is logic 0 and output waveforms with set hardening

ip OUT1 0 EXP(0'sp' 6.505ns 0.3000ns 6.595ns 0.3000ns)



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