Analysis of Leakage Power Reduction using Leakage Control Logic with Power Gating

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***Abstract* - In the world of VLSI Circuits, the semiconductor device length is quickly lowering. Attributable to this the leakage power dissipation has become associate preponderating concern. In this paper power reduction techniques are accustomed scale back power for D-Latch and SR Latch. These techniques involves leakage control Logic, leakage Feedback, sleepy Stacking and Stacking. leakage power is truly consumed once a tool is each static and change, however typically the most concern with leakage power is once the device is in its inactive state , as all the power consumed during this state is taken into account "wasted" power. Power gating which is employed as a basis of this idea is additionally a power reduction technique during which a further "sleep" PMOS transistor is placed between Vdd and also the pull up network of a circuit and a further "sleep" NMOS transistor is placed between the pull down network and GND. These circuits are turned on once the circuit is active and turned off once the circuit is off. Numerous techniques are developed to cut back power leakage. In this paper, the technique which is best in power consumption is obtained which concludes that leakage control logic is able to reduce power more efficiently than other techniques. We have performed the simulation and implementation of all the four above stated techniques on D-Latch and SR-Latch with the help of Tanner Tools.**

Keywords* - *Leakage power, leakage control logic, sleep, PMOS transistor, NMOS transistor, power gating

I. INTRODUCTION

The most common style vogue in now a days VLSI design is that the Static CMOS logic style. Digital circuits are often operated inside fraction of your time. If there's any interconnection errors or contact happens between the block it will increase the facility dissipation within the circuit. In deep submicron technology, the power dissipation or discharge power are going to be reduced by victimization leakage power reduction techniques. Discharge power reduction is extremely necessary to think about low power style. The facility reduction should be achieved while not trading-off performance that makes it tougher to scale back leakage throughout traditional operation. On the opposite hand, there are many techniques for reducing power in sleep and standby mode that uses the concept of power gating wherever a sleep semiconductor is additional between actual ground rail AND circuit ground (called virtual ground). This device is turned-off within the sleep mode to chop off the discharge path. Power gating ends up in a discount in discharge as a result of once the sleep semiconductor is off the virtual ground rail charges upto a gradual state price near Vdd. Several alternative discharge power reduction techniques uses the construct of power gating for more reduction in discharge power.

II. PREVIOUS RESEARCH WORK DESCRIBING DIFFERENT LEAKAGE REDUCTION TECHNIQUES

A. Stacking Approach:

It is a technique used for leakage power reduction, which uses a stack effect by splitting an existing transistor into two half size transistors. Figure 2 shows its structure. When the two transistors are turned off at once, induced reversed bias between the two transistors results in sub threshold leakage current reduction. However these divided transistors increases a significant amount of delay and could limit the usefulness of the approach.

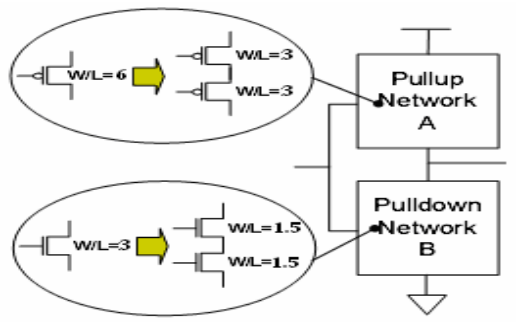

Fig. 1. Stacking

B. Sleepy Stacking Approach:

This technique involves the splitting of one transistor into three transistors, one of them is sleep transistor and rest are transistors having half the original transistor size. This type of configuration of transistors causes two-way leakage reduction, suppressing the leakage power using high-Vth transistors and involving the stack effect, thus resuults ultra-low leakage power during sleep mode and retaining original

logic state. There is a drawback in the sleepy stacking which is it increases area drastically and also having the disadvantage of sleep transistors.

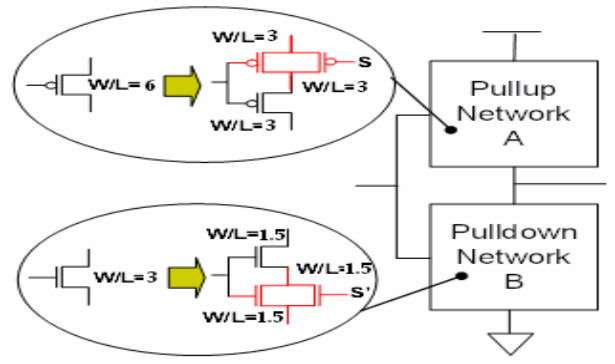

Fig. 2. Sleepy Stacking Approach

C. Leakage feedback Logic:

The leakage feedback logic approach relies on sleep approach. Figure 4 shows the structure of leakage feedback approach which uses two extra transistors to maintain logic state during the sleep mode, and the two transistors are operated by the output of an inverter which is operated by the output of a circuit implemented utilizing leakage feedback. A PMOS transistor is added in parallel to the sleep transistor and an NMOS transistor is added in parallel to the sleep transistor. The two transistors are operated by the output of an inverter which is operated by the output of the circuit. During this sleep mode, the sleep transistors are turned off and one of the transistors in parallel to the sleep transistors keep the connection with the appropriate power rail.

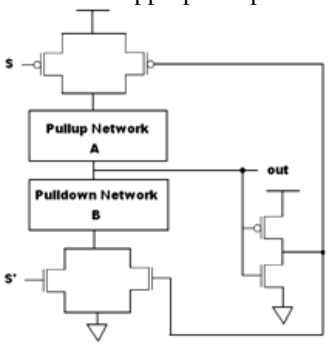

Fig. 3. Leakage feedback logic

III. PROPOSED LEAKAGE REDUCTION TECHNIQUE

Leakage Control Logic

In this technique we have tried to reduce power consumption by adding a set of two transistors in each NMOS and PMOS pair. The method and apparatus in order to reduce the leakage power is the effective stacking of transistors in the path from supply voltage to ground by applying self-biased leakage control transistors such that one of the added Leakage Control transistors is always near its cut-off region. It works based on the fact that a state with more than one transistor off in a path from supply voltage to ground is far less leaky than a state with only one transistor off in any supply to ground path.

This technique has been used for various circuits and in this paper it is used on D latch and SR latch.

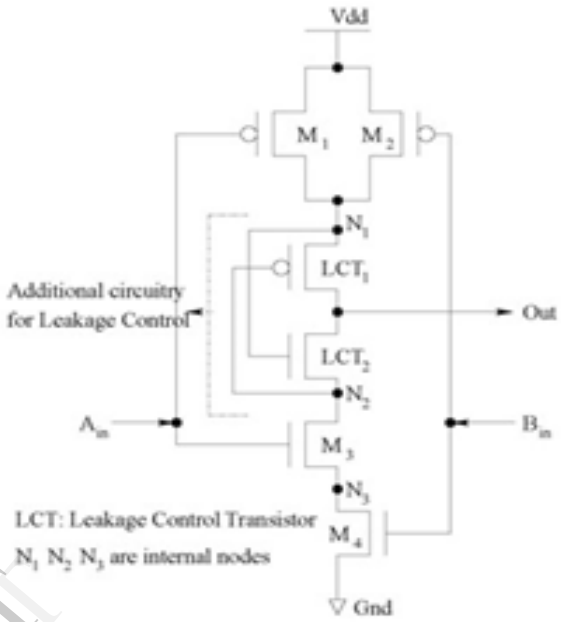

Fig. 4. Leakage Control Logic for NAND gate

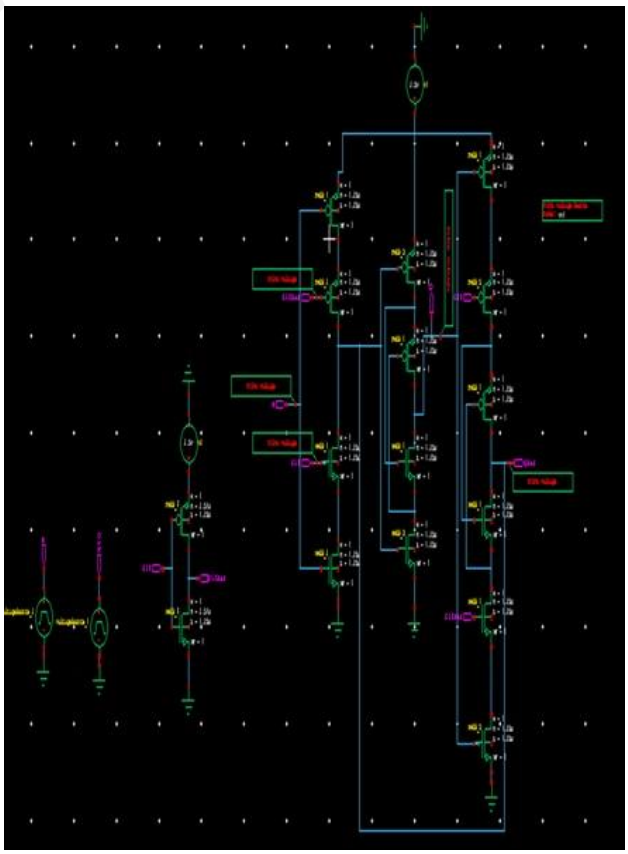

Fig. 5. D latch leakage control logic circuit

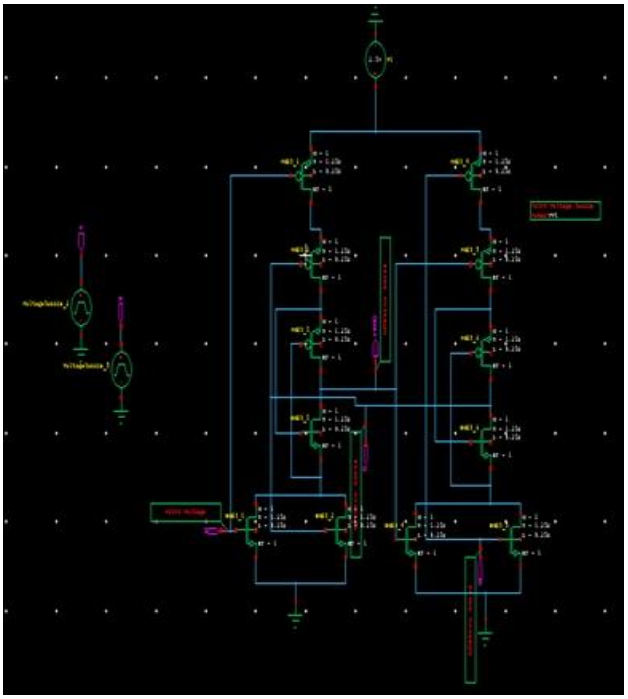

Fig. 6. SR latch leakage control logic circuit

IV. SIMULATION WAVEFOMS

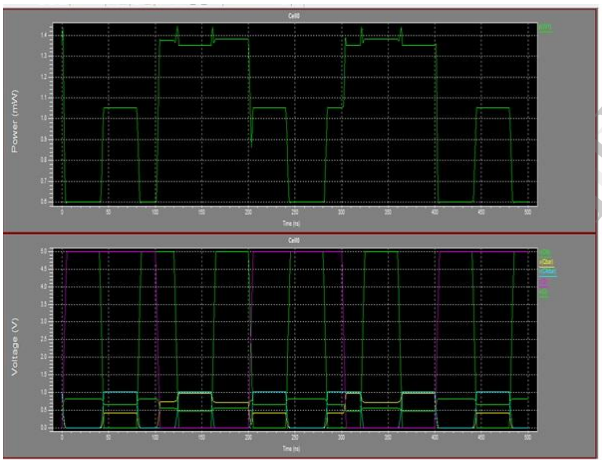

Fig. 7. Simple D latch

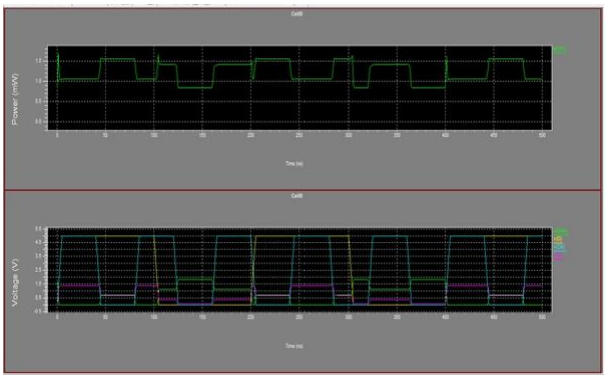

Fig. 8. D latch stacking

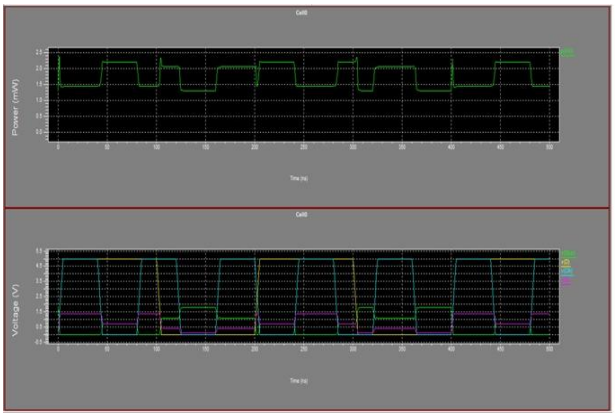

Fig. 9. D latch sleepy stacking

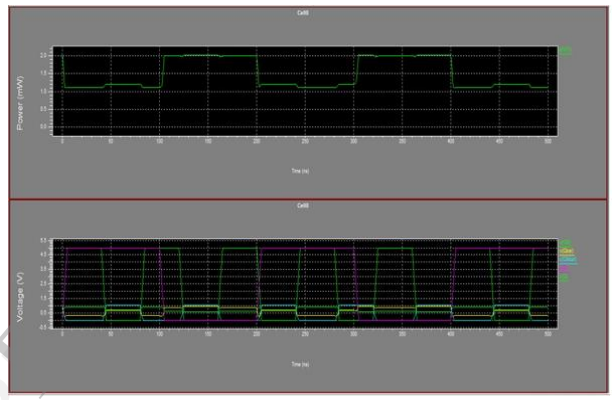

Fig. 10. D latch leakage feedback logic

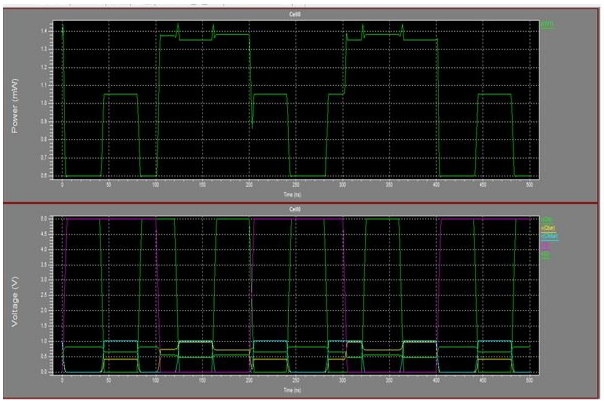

Fig. 11. D latch leakage control logic

Fig. 12. Simple SR latch

Fig. 13. SR latch stacking

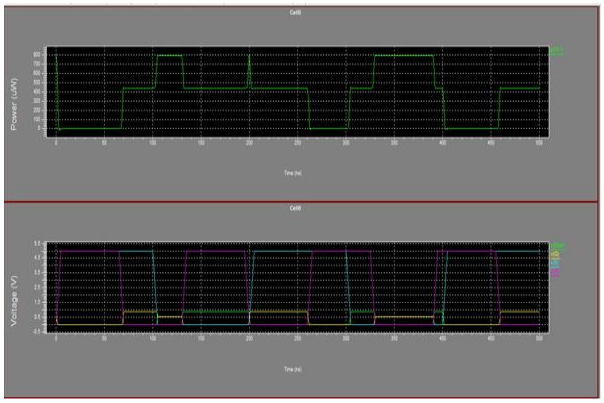

Fig. 14. SR latch sleepy stacking

Fig. 15. SR latch leakage feedback logic

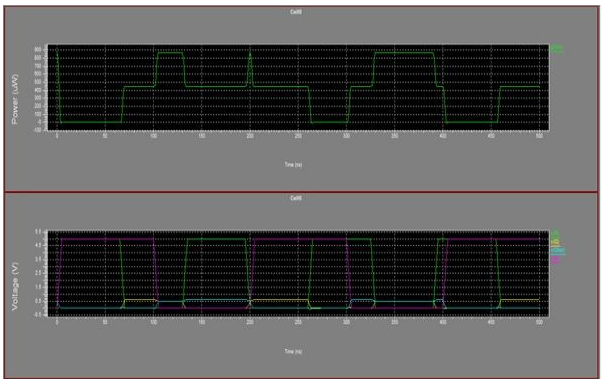

Fig. 16. SR latch leakage control logic

V. POWER COMPARISION

(a)For D Latch

TABLE I. Power consumption in various D latch circuit

Logic	Average power consumed
D latch	3.940513e-003 watts
D latch stacking	1.228086e-003 watts
D latch sleepy stacking	1.760429e-003 watts
D latch leakage feedback	1.490627e-003 watts
D latch leakage control	1.032401e-003 watts

The above represented table clearly shows that in case of D latch Leakage Control Logic, power is consumed to its minimum.

(b) For SR Latch

TABLE II. Power consumption in various SR latch circuit

Logic	Average power consumed
SR latch	1.410032e-003 watts
SR latch stacking	5.241096e-004 watts
SR latch sleepy stacking	3.595172e-004 watts
SR latch leakage feedback	7.180424e-004 watts
SR latch leakage control	3.854125e-004 watts

Also for SR Latch Leakage Control Logic is most efficient in comparison to other logics.

CONCLUSION

In the process of achieving higher performance and greater speed, the feature size and threshold voltage of CMOS technology is gradually scaling down which results in increase of leakage power dissipation. A novel approach namely “Leakage Control Logic” which is an efficient methodology to reduce leakage power is presented. This paper drives to a result that Leakage Control Logic is the most efficient logic to reduce power consumption in a CMOS circuit based on D latch and SR latch. Using this logic the number of transistor used in the circuit increases which leads to increase in area of circuit, but this paper is more concerned about power, so increase in area can be ignored.

REFERENCES

[1] Uma nirmal “A Low power high speed addressing using MTCMOS tech-niques” IJCEM International Journal of Computational Engineering & Man-agement, Vol. 13, July 2011.

[2] Kanak Agarwal, "Power Gating with Multiple Sleep Modes "IBM Research, Austin, TX, 78758.

[3]] Milind Gautam, "Reduction of Leakage Current and Power in Full Subtractor Using MTCMOS Technique" 2013 International Conference on Computer Communication and Informatics (ICCCI -2013), Jan. 04 – 06, 2013, Coimbatore, INDIA.

[4] Anbarasu.W “ Studying Impact of Various Leakage Current Reduction Techniques on Different D-Flip Flop Architectures” International Journal of Advancements in Research & Technology, Volume 2, Issue5, May-2013.

[5] Jun Cheol Park “Sleepy Stack Reduction of Leakage Power” PATMOS 2004, LNCS 3254, pp. 148–158, 2004.

[6] B. Srujana Sri “DESIGN OF LOW POWER 4-BIT FULL ADDER USING SLEEPY KEEPER APPROACH” IJRET, NOV 2012.

[7] T KRISHNA MOORTHY “Low Power Dissipation of 4 bit Parallel adder/ subtractor using Dual Sleep and ground bounce technique in 120nm and 90nm Technology” International Journal of VLSI and EmbeddedSystems-IJVES Vol 04, Article 10162;October 2013.