

Application Of Space Vector Modulation Technique For Three Level Neutral Point Clamped Inverters

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Abstract: --- Multilevel inverters are gaining importance in high power and high voltage applications due to their superior performance compared to two-level inverters. Among various modulation techniques for a multilevel inverter, the space vector pulsewidth modulation (SVPWM) is widely used. However, the implementation of the SVPWM for a multilevel inverter is complicated. The complexity is due to the difficulty in determining the location of the reference vector, the calculation of on-times, and the determination and selection of switching states. This paper presents the analysis of a three level three-phase inverter using sine pulse width modulation (SPWM) and space vector pulse width modulation (SVPWM). Neutral-point-clamped converters are increasingly applied in industrial drive systems as they allow the use of lower voltage devices in higher voltage applications, provide reduced output voltage total harmonic distortion (THD), and can develop low common mode voltage. Since the proposed multilevel SVPWM method uses two-level modulation to calculate the on-times, the computation of on-times for an n -level inverter becomes easier. Simulation is carried out using matlab/simulink and the simulation results are presented.

Keywords- three level inverter, sine pulse width modulation, space vector pulse width modulation.

I. INTRODUCTION

A multilevel inverter divides the dc rail directly or indirectly, so that the output of the leg can be more than two discrete levels. As both amplitude modulation and pulse width modulation are used in this, the quality of the output waveform gets improved with low distortion. The advantages of multilevel inverter are good power quality, low switching losses, reduced output dv/dt and high voltage capability. Increasing the number of voltage levels in the inverter increases the power rating. The three main topologies of multilevel inverters are the Diode clamped inverter, Flying capacitor inverter, and the Cascaded H-bridge inverter.

THREE-Level inverter topology has attracted attention in high power high performance voltage drive applications due to their superior performance compared to two-level inverters, such as lower common-mode voltage, lower dv/dt , lower harmonics in output voltage and current, and reduced voltage on the power switches [2]. Single-phase voltage source inverters cover low-range power applications and three-phase voltage source inverters cover the medium to high power applications [1]. The main purpose of these two level and three level inverter topologies is to provide a three phase voltage source, where

the amplitude, phase, and frequency of the voltages should always be controllable. Although most of the applications require sinusoidal voltage waveforms voltages are also required in some emerging applications. Three level diode clamped (Neutral point) inverter is most favorable among the various multi level configuration. The three level diode clamped inverter employs clamping diode and series DC capacitor to produce AC voltage waveform with three level(phase to ground).

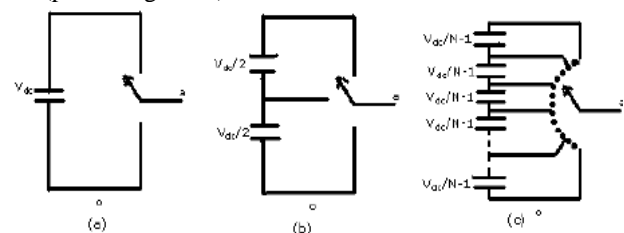


Figure Schematic Diagram of (a) Two level Inverter (b) Three Level Inverter (c) N Level Inverter

To control multilevel converters, the pulse width modulation (PWM) strategies are the most effective, like sine pulse width modulation, single pulse width modulation, space vector modulation etc. To control multilevel converters, the pulse width modulation (PWM) strategies are the most effective, especially the space vector pulse width modulation (SVPWM) one, which has equally divided zero voltage vectors describing a lower total harmonic distortion (THD). Although the complexity that presents the SVPWM strategy (many output vectors) compared with the carrier based PWM one, it remains the preferred seen that it reduces the power losses by minimizing the power electronic devices switching frequency (limiting the minimum pulse width).

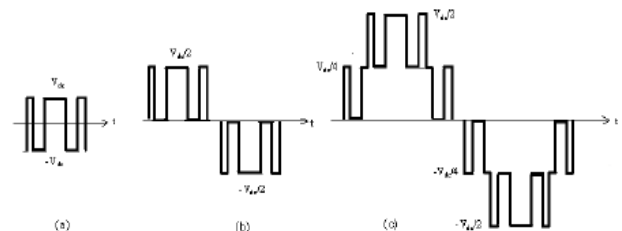


Figure Output Voltage of (a) Two Level Inverter (b) Three Level Inverter (c) Five Level Inverter

The three-level inverter topology is generally used in realizing the high performance, high voltage AC drive systems. In the conventional two-level inverter configurations, the reduction of the harmonic contents of the inverter output current is achieved mainly by raising the switching frequency. However in the field of high voltage,

high power application, the switching frequency of the power devices has to be restricted below 1kHz, due to the increased switching losses, So the harmonic reduction by raised switching frequency of the two-level inverter becomes more difficult in high power applications. In addition, in two-level configurations, the DC link voltage of the two-level inverter is limited by the voltage ratings of the switching devices, so the problematic series connection of the switching devices is required to raise the DC link voltage. By series connection, the maximum allowable switching frequency has to be more lowered, thus the harmonic reduction becomes more difficult. From the aspect of the harmonic reduction and the higher voltage level, three-level approach seems to be most promising alternative. The harmonic contents of the three-level inverter are less than that of two-level inverter at the same switching frequency and the blocking voltage of the switching device is half of the DC-link voltage. So the three-level inverter topology is generally used in realizing the high performance, high voltage AC drive systems.

II. THREELEVEL INVERTER

Fig. 1 shows a schematic diagram of a three level diode clamped inverter. The diode-clamped multilevel inverter consists of clamping diodes and cascaded dc capacitors to produce ac voltage waveforms with multiple levels. There are three arms of the inverter for a three phase inverter. Each arm is made up of four active switches $S1$ to $S4$ with four anti parallel diodes $D1$ to $D4$ respectively. On the dc side of the inverter, the dc bus capacitor is split into two, providing a neutral point N . The diodes connected to the neutral point, $Dn1$ and $Dn2$, are the clamping diodes. When switches $S2$ and $S3$ are turned on, the inverter output terminal A is connected to the neutral point through one of the clamping diodes. The voltage across each of the dc capacitors is $V_{dc}/2$, which is normally equal to half of the total input dc voltage V_{dc} .

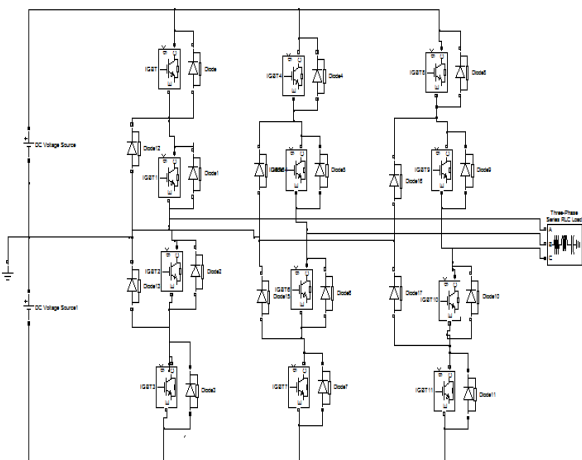


Fig.1: three level diode clamped inverter.

The circuit employs 12 power switching devices (e.g. **SI-S4**) and 6 clamping diodes. And the dc-bus voltage is split into three-level by two series-connected bulk capacitors, **C1** and **C2**. The middle point of the two capacitors can be defined as the neutral point N . As the result of the clamped diode, the switch voltage is limited to half the level of the dc-bus voltage V_{dc} . Thus, the voltage stress of switching device is greatly reduced. The output voltage V_o has three different states: $+V_{dc}$, 0 and $-V_{dc}$. taking phase **A** as an example, For voltage level $+V_{dc}$, **S1** and **S4** need to be turned on; for 0 level, **S1** and **S3** need to be turned on; and for $-V_{dc}$, **S2** and **S4** need to be turned on. We can define these states as 2, 1, and 0, respectively. Then, the switching variable S_o is shown in Table 1, the switching states of each leg of three-phase three level inverter is described by using switching variables S_o , S_1 , and S_2 . Whereas the difference is that, in three level inverter, each bridge leg has three different switching states.

III. SINE PULSE WIDTH MODULATION

In this method, the width of each pulse is varied in proportion to the amplitude of a sine wave evaluated at the centre of the same pulse. The distortion factor and lower order harmonics are reduced significantly. The gating signals are generated by comparing a sinusoidal reference signal with a triangular carrier wave of frequency F_c . The frequency of reference signal F_r , determines the inverter output frequency and its peak amplitude A_r , controls the modulation index M , and rms output voltage V_o . The number of pulses per half cycle depends on the carrier frequency.

Sinusoidal pulse width modulation is as shown in fig.2. In three phase sinusoidal pulse width modulation technique, there are three reference waves each shifted by 120° . A carrier signal is compared with the reference signal corresponding to a phase to generate the gating signal for that phase.

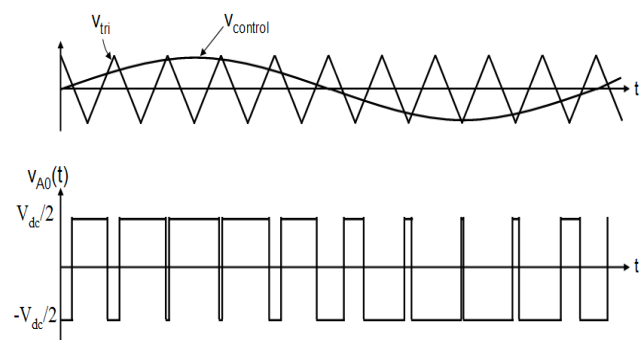


Figure 2: sinusoidal pulse width modulation.

PWM can be generated by analogue or digital control electronics. The advantages of digital controls over analogue are:

Stability (no drift, offsets or aging effects)

Precision (noise immunity)

Flexibility (can be customized by changing software)

Even if done digitally, significant computing time is required, as the PWM signals have to be calculated in real time. By using Space Vector Modulation this calculation process is simplified.

IV. SPACE VECTOR MODULATION

A three-level inverter is characterized by $3^3=27$ switching states as indicated in Fig.2 where the space vector diagram for the three-level inverter which is divided into the six sectors (I, II, III, IV, V, and VI) is also shown. There are 24 active states, and three zero states that lie at the center of the hexagon. Each sector has four regions (1,2,3,4) [3]. The switching states of the inverter are summarized in Table I. Switching state 'P' denotes that the upper two switches in leg A are on and the inverter terminal voltage v_{An} , which is the voltage at terminal A with respect to the neutral point n, is $+V_{dc}/2$, whereas 'N' indicates that the lower two switches conduct, leading to $v_{An} = -V_{dc}/2$. Switching state 'O' signifies that the inner two switches S_2 and S_3 are on and v_{An} is clamped to zero through the clamping diodes. Depending on the direction of load current [bin wo]. It can be observed from Table 1 that switches S_1 and S_3 operate in a complementary manner. With one switched on, the other must be off. Similarly, S_2 and S_4 are a complementary pair as well.

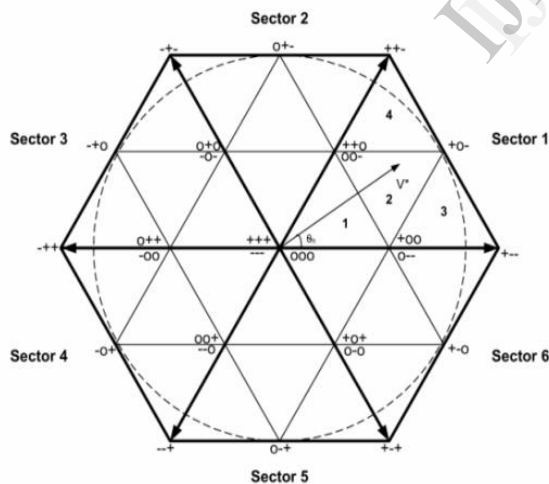


Fig.3: sectors of three level space vector diagram

The principle of SVPWM method is that the command voltage vector is approximately calculated by using three adjacent vectors. The duration of each voltage vectors obtained by vector calculations;

$$T_1V_1 + T_2V_2 + T_3 = T_{SV}^*$$

$$T_1 + T_2 + T_3 = T_S$$

where V_1 , V_2 , and V_3 are vectors that define the triangle region in which V^* is located. T_1 , T_2 and T_3 are

the corresponding vector durations and T_s is the sampling time.

In a three-level inverter similar to a two-level inverter, each space vector diagram is divided into 6 sectors. For simplicity here only the switching patterns for Sector A will be defined so that calculation technique for the other sectors will be similar. Sector A is divided into 4 regions as shown in Fig.3 where all the possible switching states for each region are given as well. SVPWM for three-level inverters can be implemented by using the steps of sector determination, determination of the region in the sector, calculating the switching times, T_a , T_b , T_c and finding the switching states.

The complexity is due to the difficulty in determining the location of the reference vector, the calculation of on-times, and the determination and selection of switching states.

The space vector diagram of any three-phase n-level inverter consists of six sectors. Each sector consists of $(n-1)^2$ triangles. The tip of the reference vector can be located within any triangle. Each vertex of any triangle represents a switching vector. A switching vector represents one or more switching states depending on its location. There are n^3 switching states in the space vector diagram of an n-level inverter. The SVPWM is performed by suitable selecting and executing the switching states of the triangle for the respective on-times. It is also known as "Nearest Three Vector" (NTV) approach. The performance of the inverter significantly depends on the selection of these switching states. Fig.6.3 shows the space vector diagram of a three-level inverter. There are six sectors (S1-S6), four triangles (Δ_0 - Δ_3) in a sector, and a total of 27 switching states in this space vector diagram.

A. Determining the sector

θ_n (Theta) is calculated Using the Equation no 1

$$\theta_n = 2 * \pi * frequency * time \quad 1$$

and then the sector, in which the command vector V_{ref} is located, is determined as;

If θ_n is between $0^\circ \leq \theta_n < 60^\circ$, then V_{ref} in Sector 1,

If θ_n is between $60^\circ \leq \theta_n < 120^\circ$, then V_{ref} in Sector 2,

If θ_n is between $120^\circ \leq \theta_n < 180^\circ$, then V_{ref} in Sector 3,

If θ_n is between $180^\circ \leq \theta_n < 240^\circ$, then V_{ref} Sector 4,

If θ_n is between $240^\circ \leq \theta_n < 300^\circ$, then V_{ref} Sector 5,

If θ_n is between $300^\circ \leq \theta_n < 360^\circ$, then V_{ref} Sector 6.

B. Determining the Region & Simplified Calculation of Duty Cycles

The theoretical maximum length of the normalized reference vector is the two-unity value. However, in steady state conditions, its length is limited to 3 due to the fact that

longer lengths of this vector will be outside of the vector diagram hexagon, and thus cannot be generated by modulation. In fig 6.4, the reference vector is decomposed into the axes located at zero and sixty degrees, obtaining projections m_1 and m_2 , respectively.

A. Finding the switching states

By considering the switching transition of only one device at any time, the switching orders given below are obtained for each region located in Sector 1 if all switching states in each region are used.

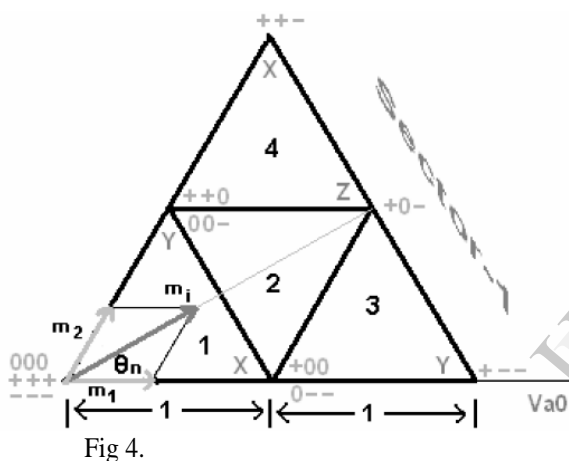
Therefore, switching signals for Sector 1 are,

Region 1: - 0--, 00-, 000, +00, ++0, +++

Region 2: - 0--, 00-, +0-, +00, ++0

Region 3: - 0--, ++-, +0-, +00

Region 4: - 00-, +0-, ++-, ++0



V.MATLAB/SIMULINK MODEL OF THREE LEVEL INVERTER WITH SINE AND SPACE VECTOR PULSE WIDTH MODULATION

The three phase inverter circuit is designed and implemented using matlab. The design procedure is as follows:

- The inverter consists of 3 IGBT arms which forms a three phase inverter.
- The input is a DC voltage source.
- The gate pulse is given by the space vector modulation block.
- The timing signals, timing generation and the timing calculations, the sequence of switching devices are designed and are given by the space vector modulation block.
- To get the required output, an LC filter is designed at the output of the inverter to get a pure sinusoidal output wave.
- The simulation is carried out using matlab.

This section details the step by step development of a Matlab simulation model for implementing SVPWM.

1. The input given is a constant DC link voltage.
2. The Switching time calculation: The switching time and corresponding switch state for each power switch is calculated and a space vector modulation block is created which gives the gating pulse for the switches used in the three phase inverter designed.
3. The three-phase inverter block: This block is built to simulate a voltage source inverter. The inputs to the inverter block are the switching signals and the outputs are the PWM phase-to-neutral voltages.
4. The filter block: To visualize the actual output of the inverter block, filtering of the PWM ripple is required. The PWM voltage signal is filtered here using a simple LC filter.
5. The input frequency is kept at 50 Hz and the switching frequency of the inverter is chosen as 2 kHz. The output is seen to be sinusoidal without any ripple except the switching harmonics.

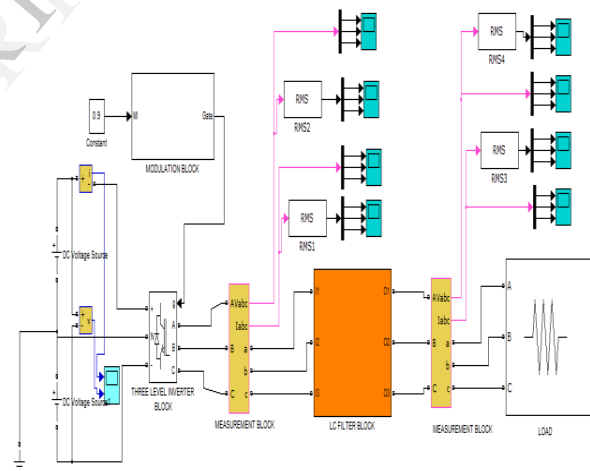


Fig. 5 three level simulink model.

PARAMETERS:

- V_{dc}= input voltage V_{dc} = V_{dc1}=275 V DC
- M.I= Modulation index = 0.9
- L= inductor in mH = 25.668mH
- C= capacitor in μF =36 μF
- Load= three phase resistive load
- Power = 5000 W
- Rated output voltage = 415 V
- Output frequency = 50 Hz.

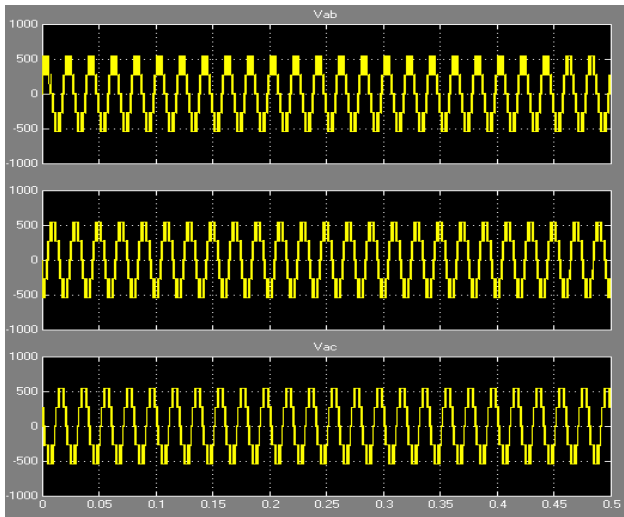


Fig.6 Output voltage waveform before the filter for three level inverter with SPWM

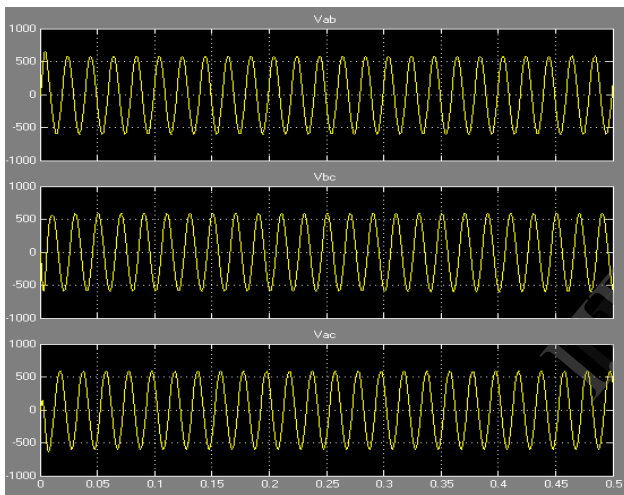


Fig.7 Output voltage waveform after the filter for three level inverter with SPWM

VI. COMPARISON OF SPWM AND SVPWM

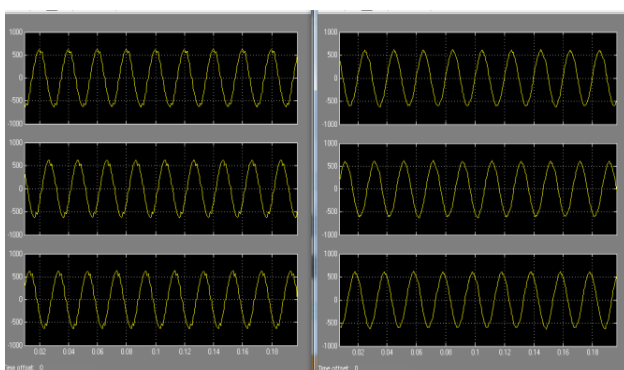


Figure 8 : comparison of sine PWM and SVPWM for a two level inverter.

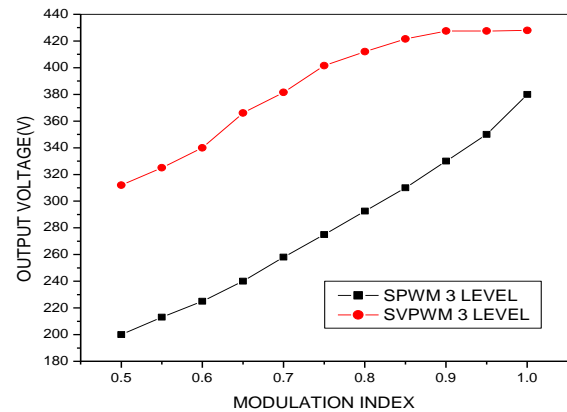


Fig. 9 SPWM vs. SVPWM for a three level inverter

VII. CONCLUSION

Space vector modulation requires only one reference space vector to generate three-phase sine waves and by controlling the reference space vector, the amplitude and frequency of load voltage can be varied. This algorithm is flexible and suitable for advanced vector control. Space Vector Modulation for a three phase UPS inverter makes it possible to adapt the switching behavior to different situations such as: half load, full load, linear load, non-linear load, static load, pulsating load, etc. Space Vector Modulation provides excellent output performance, optimized efficiency, and high reliability compared to similar inverters with conventional Pulse Width Modulation.

Model	Time taken to attain Steady State	Voltage overshoot, (pu)
spwm_3_lvl	4.00E-03	1.5
svpwm_3_lvl	2.20E-03	0.69

It is seen that the time taken by space vector modulation - SVPWM is 50% lesser than that for SPWM for the same levels. Also, the voltage overshoot is less in SVPWM as compared with SPWM and the dv/dt stress on the power semiconductor device reduces.

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