Built in Test Compression Capabilities in Programmable PRPG

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Abstract- **This paper presents a low power pseudo random pattern generator with desired preselected toggling activity. The proposed architecture has a linear feedback shift register or a ring generator (linear finite state machine) which drives phase shifter and it produces binary sequences with low switching rate. This will have the best test coverage achievable compared with the best-to-date conventional BIST-based PRPGs. In this proposed system we introduce with negligible impact on test application time and deterministically guide the test pattern generator towards test sequences which will improve the ratio of fault-coverage-to pattern-count. The above proposed hybrid system efficiently combines test compression with Logic BIST to deliver high quality tests. The system is implemented using HDL and the simulation and synthesis reports are shown.**

***Keywords*-LFSR, Optimization, Low Power, Test Patterns, pseudorandom test pattern generators (PRPGs), test data volume compression.**

I. INTRODUCTION

Different forms of embedded test are increased and they are essentially used to reduce the test time and cost of testing. Various forms of embedded test are increasingly viewed as essential to reduce test cost. Scan based testing has gained higher acceptance and reliable solution. However, in the scan based test, higher data switching activity is present. Due to high data activity the circuit under test will dissipate more power during test operations. Reductions in the operating power of the circuit in the test mode should be minimum and it is concern for the present scenario. A full-toggle scan pattern may draw several times the typical functional mode power, and this trend continues to rise, particularly over the mission mode's peak power. This power-induced over-test may result in thermal issues, voltage noise, power droop, or excessive peak power over multiple cycles which, in turn, cause a yield loss due to instant device damage, severe decrease in chip reliability, shorter product lifetime, or a device malfunction because of timing failures following a significant circuit delay.

Numerous schemes for power reduction during scan testing have been devised [1]. Among them there are solutions specifically proposed for built-in self-test (BIST) to keep the average and peak power below a given threshold. For example, the test power can be reduced by preventing transitions at memory elements from propagating to combinational logic during scan shift. This is achieved by inserting gating logic between scan cell outputs and logic they drive [2], [3].

During normal operations and capture, this logic remains transparent. Gated scan cells are also proposed in [4] and [5]. A synergistic test power reduction method of [6] uses available on-chip clock gating circuitry to selectively block scan chains while employing test scheduling and planning to further decrease BIST power in the Cell processor. A test vector inhibiting scheme of [7] masks test patterns generated by an LFSR as not all produced vectors, often very lengthy, detect faults. Elimination of such tests can reduce switching activity with no impact on fault coverage.

A device presented in [8] is comprised of an LFSR feeding scan chains through biasing logic and T-type flip-flop. Since this flip-flop holds the previous value until its input is asserted, the same value is repeatedly scanned into scan chains until the value at the output of biasing logic (e.g., a k-input AND gate) becomes 1. Depending on k, one can significantly reduce the number of transitions occurring at the scan chain inputs. A scheme that combines the low transition generator of [8] (handling easy-to detect faults) with a 3-weight PRPG (deployed to detect random pattern resistant faults) can also be used to reduce switching activity during BIST, as demonstrated in [9].

In this paper, we propose a PRPG for LP BIST applications. The generator primarily aims at reducing the switching activity during scan loading due to its preselected toggling (PRESTO) levels. This architecture will allow to configure the scan chain to be driven either by a PRPG itself or by a constant value fixed for a given period of time. The PRESTO generator allows loading scan chains with patterns having low transition counts with significantly reduced power dissipation. It also enables fully automated selection of its controls such that the resultant test patterns feature desired, user-defined toggling rates. The PRESTO generator can also successfully act as a test data decompressor. This allows one to implement a hybrid test methodology that combines LBIST and ATPG-based embedded test compression.

This paper is organized as follows. Section II introduces the basic operational principles of the PRESTO generator, while Section III presents all architectural details of its structure with a brief discussion of the generator's abilities to produce patterns with various toggling rates. The performance of the PRESTO generator is dealt in section IV. A PRESTO-based LP test data decompressor is introduced in Section V, which is followed by the simulation and synthesis report using CAD tools in Section VI. Finally, conclusion is given.

II. BASIC PRESTO ARCHITECTURE

Figure 1 illustrates the basic hardware structure of a PRESTO generator. It circuit consists of an n-bit conventional PRPG connected with a phase shifter feeding scan chains forms a kernel of the generator producing the actual pseudorandom test patterns. The PRPG is implemented either Linear feedback shift register or a ring generator. The n bit hold latches are placed between phase shifter and PRPG. Each hold latch is individually controlled through a corresponding stage of an n-bit toggle control register. When the enable input is asserted, the given latch is transparent for data going from the PRPG to the phase shifter, and it is in the toggle mode. In the hold mode the latch is disabled, the system captures and saves the corresponding bit of PRPG, for a number of clock cycles, thus feeding the phase shifter (and possibly some scan chains) with a constant value. Each phase shifter output is obtained by XOR-ing outputs of three different hold registers. In this operation, every scan chain remains in a low-power mode which is provided by disabled hold latches drive the corresponding phase shifter output.

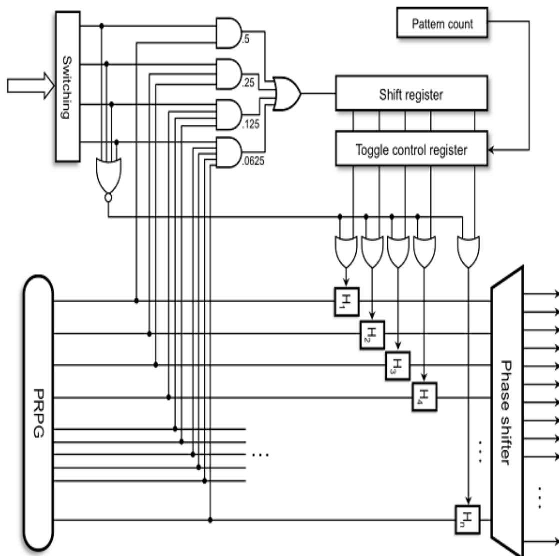

Figure 1. Basic architecture of a PRESTO generator

As mentioned above, the toggle control register supervises the hold latches. Its content values 0's and 1's, where 1's indicate latches in the toggle mode, thus transparent for data arriving from the PRPG. The switching activity is determined by their fraction. The control register is reloaded with the content of an additional shift register once per pattern. In order to enable the shift, register the enable signals injected and it produced in a probabilistic fashion by using the original PRPG with a programmable set of weights. Using four AND gates the weights are determined by producing 1s with the probability of 0.5, 0.25, 0.125, and 0.0625, respectively. The choice of probabilities is done by the OR gate. A 4-bit register Switching is employed to activate AND gates, and allows selecting a user-defined level of switching activity. For example, the switching code 0010 will set to 1, on the average, 12.5% of the control register stages, and thus 12.5% of hold latches will be enabled. Given the phase shifter structure, the amount of scan chains receiving constant values is assessed, and thus the expected toggling ratio.

The switching code 0000 is detected by using an additional 4-input NOR gate, which is used to switch the low power functionality off. The content of the shift register can also be selected in a deterministic manner due to a multiplexer placed in the front of the serial input of the register. It is worth noting that when working in the weighted random mode, the switching level selector ensures statistically stable content of the shift register in terms of the amount of 1s it carries. As a result, roughly the same fraction of scan chains will stay in the low power mode, though a set of actual low toggling chains will keep changing from one test pattern to another. It will correspond to a certain level of toggling in the scan chains. With only 15 different switching codes, however, the available toggling granularity may render this solution too coarse to be always acceptable. The next section presents additional features that make the PRESTO generator fully operational in a wide range of desired switching rates.

III. LOW POWER FULLY OPERATIONAL GENERATOR

Much higher flexibility in forming low-toggling test patterns can be achieved by deploying extra hardware which is shown in Fig. 2. In this approach, it splits up a shifting period of every test pattern into a sequence of alternating hold and toggle intervals. To move the generator backward and forward between these two states, we use a Toggle-type of flip-flop that switches whenever there is a 1 on its data input. If it is set to 0, the generator enters the hold period with all latches temporarily disabled regardless of the control register content. This is accomplished by placing AND gates on the control register outputs to allow freezing of all phase shifter inputs. This property can be crucial in SoC designs where only a single scan chain crosses a given core, and its abnormal toggling may cause locally unacceptable heat dissipation that can only be reduced due to temporary hold periods. If this T flip-flop is set to 1 (the toggle period), then the latches are enabled through the control register which can pass test data moving from the PRPG to the scan chains.

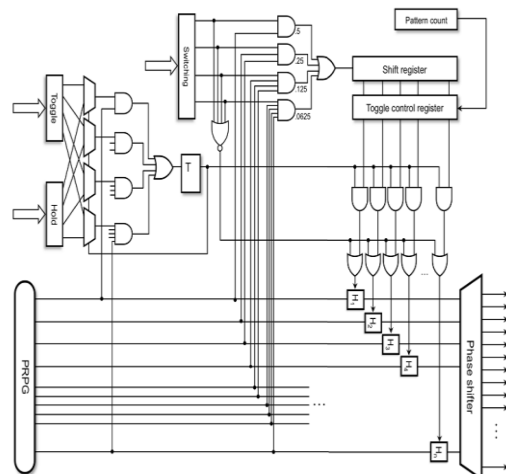

Figure 2. Fully operational Low power version of PRESTO

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Two additional parameters kept in 4-bit Hold and Toggle registers determine how long the entire generator remains either in the hold mode or in the toggle mode, respectively. To terminate either mode, a 1 must occur on the T flip-flop input. This weighted pseudorandom signal is produced in a similar manner to that of weighted logic used to feed the shift register. The T flip-flop controls also four 2-input multiplexers routing data from the Toggle and Hold registers. It allows selecting a source of control data that will be used in the next cycle to possibly change the operational mode of the generator. For example, when in the toggle mode, the input multiplexers observe the Toggle register. Once the weighted logic outputs 1, the flip-flop toggles, and as a result all hold latches freeze in the last recorded state. They will remain in this state until another 1 occurs on the weighted logic output. The random occurrence of this event is now related to the content of the Hold register, which determines when to terminate the hold mode.

Although the remaining registers are loaded once per test pattern (also at the scan shift speed), timing is not compromised because of shallow logic generating bits to be loaded serially into the registers. With the help of shadow registers, values remain unchanged during capture. Clearly, it suits LBIST applications, where the shift speeds are quite high. The LP registers are also added during embedded deterministic test (EDT) IP generation and insertion. The associated logic is integrated into the design along with the EDT logic. Since the EDT logic (including LP) is only added in the scan paths, there is no impact on the functional mode of operation.

IV. AUTOMATIC SELECTION OFCONTROLS

The performance of the PRESTO generator depends primarily on the following three factors:

1) the switching code (kept in the switching register).
2) the hold duty cycle (HC).
3) the toggle duty cycle (TC).

Given the size of PRPG, the number of scan chains and the corresponding phase shifter, can be selected automatically in such a way that the entire generator will produce pseudorandom test patterns having a desired level of toggling T provided the scan chains are balanced. The procedure of selecting these parameters consists of the following steps.

1) For each switching code k, k =1, 15, determine the corresponding probability pk of injecting a 1 into the shift register. These values are as follows: p1=0.5, ...,p14=0.38476563,and p15=0.69238281.

2) The values p_k obtained in step 1 determine as well the probability of asserting the T flipflop input for each hold (toggle) code k, and then the corresponding duration h_k (t_k)of the hold (toggle) duty cycle. Clearly, $h_k = t_k = 1/p_k$.

3) Given the size n of PRPG, determine, for each switching code k, the average number n_k of 1s occurring in the control register.

$$n_k = p_k \times n. \quad (1)$$

4) For each value of n_k (the number of enabled hold latches), find the average number a_k of active scan chains, i.e., scan chains that are not in the LP mode. This number is determined by the phase shifter architecture, and it also depends on the actual locations of 1s in the control register.

5) Given a desired level of toggling T (%), one can determine the resultant (hypothetical) number A of active scan chains:

$$A=(T\times S)/50 \quad (2)$$

Where S is the total number of scan chains.

6) For each switching code k, and thus the resulting number a_k of active scan chains, determine how many additional scan chains should be disabled. In each case, this quantity is given by $d_k = a_k - A$. If $d_k \leq 0$, then disregard the next steps, as the switching code k does not guarantee even the smallest (required) number of active scan chains.

7) Since disabling extra scan chains cannot be implemented through the control register. The value of dk is therefore converted into the number of corresponding cells in active scan chains

8) Ratio r is now evaluated for each value of h_k and t_k (in total $15 \times 15 = 225$ combinations) to find the best matching between the actual value of r and the theoretical value of the expression $(a_k/A)-1$.

9) Values of switching hold, and toggle codes that yield ratio r with the smallest deviation from the theoretical value are selected as the PRESTO setup parameters.

V. LP DECOMPRESSOR

In order to facilitate test data decompression while preserving its original functionality, the circuitry of Figure 2 has to be rearchitected and it is shown in Figure 3. The core principle of the decompressor is to disable both weighted logic blocks (V and H) and to deploy deterministic control data instead. In particular, the content of the toggle control register can now be selected in a deterministic manner due to a multiplexer placed in front of the shift register. Furthermore, the Toggle and Hold registers are employed to alternately preset a 4-bit binary down counter, and thus to determine durations of the hold and toggle phases. When this circuit reaches the value of zero, it causes a dedicated signal to go high in order to toggle the T flip-flop. The same signal allows the counter to have the input data kept in the Toggle or Hold register entered as the next state.

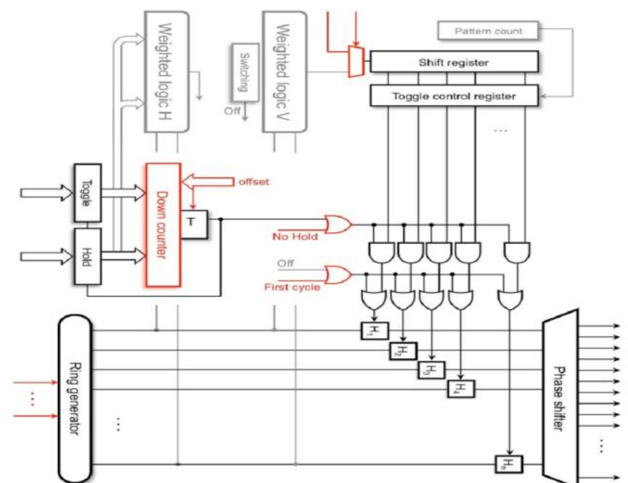

Figure 3. LP decompressor modules (gray are disabled and red items have been added)

Both the down counter and the T flip-flop need to be initialized every test pattern. The initial value of the T flip flop decides whether the decompressor will begin to operate either in the toggle or in the hold mode, while the initial value of the counter, further referred to as an offset, and determines that mode's duration. As can be seen, functionality of the T flip-flops remains the same as that of the LP PRPG but two cases. First of all, the encoding procedure may completely disable the hold phase by loading the Hold register with an appropriate code, for example, 0000. As a result, the entire test pattern is going to be encoded within the toggle mode exclusively. In addition, all hold latches have to be properly initialized.

VI. RESULTS AND DISCUSSION

The basic PRESTO pseudo random generator is coded using HDL and this simulated and verified. The simulation result is shown in figure 4

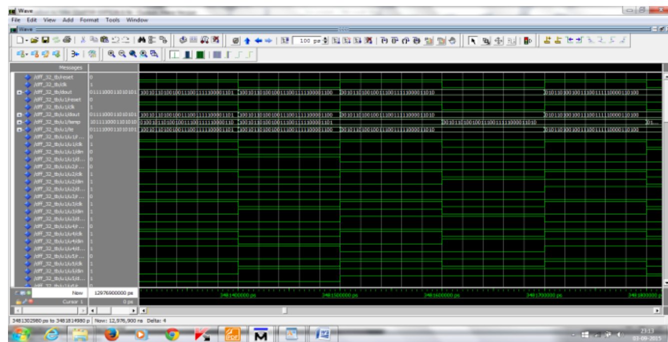

Figure 4. Pseudo random pattern generation simulation result

Low power fully operational generator circuit is coded using VHDL and this is simulated using CAD tool and the simulation result is shown in figure 5. This is verified using random input value.

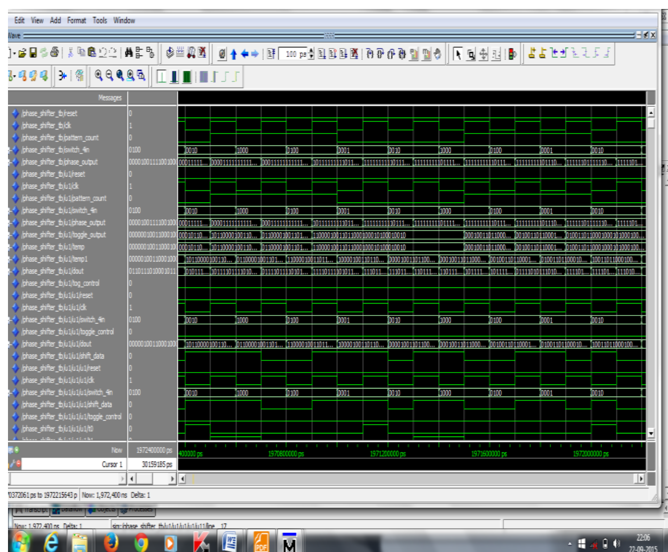

Figure 5. Low power fully operational generator simulation result

The proposed architecture is coded using HDL and the simulation is shown in figure 6.

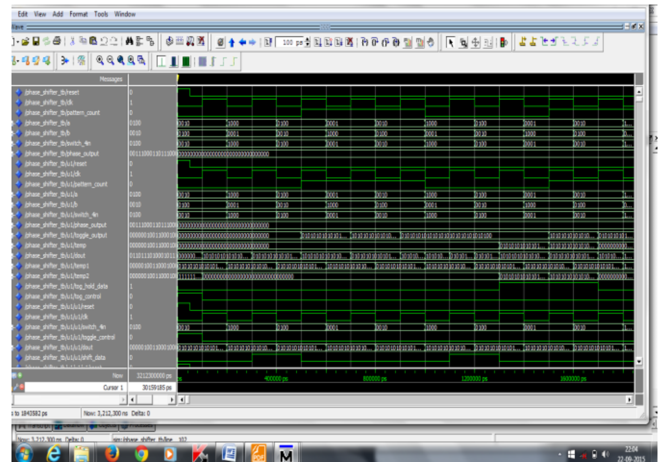

Figure 6. LP decompressor module simulation result

The synthesis report for the normal and modified is shown below

Table1. Device utilization summery for Basic PRESTO module

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	161	4656	3%
Number of Slice Flip Flops	286	9312	3%
Number of 4 input LUTs	42	9312	0%
Number of bonded IOBs	39	158	24%
Number of GCLKs	1	24	4%

Table 2. Device utilization summery for the proposed PRESTO module

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	204	4656	4%
Number of Slice Flip Flops	357	9312	3%
Number of 4 input LUTs	56	9312	0%
Number of bonded IOBs	47	158	29%
Number of GCLKs	1	24	4%

VII.CONCLUSION

This paper presents, PRESTO the LP generator can produce pseudorandom test patterns with scan shift-in switching activity precisely selected through automated programming. The features can be used to control the generator. The proposed architecture yield desired fault coverage faster than the conventional pseudorandom patterns. This is also capable of acting as a fully functional test data decompressor with the ability to control scan shift-in switching activity through the process of encoding. The proposed hybrid architecture allows one to efficiently combine test compression with logic BIST and these techniques can work synergistically to deliver high quality test. The above architecture is coded and synthesized using CAD tools. The simulation result and synthesized results are shown.

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