International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 2 Issue 11, November - 2013

Certain Investigations on NAND Based Flip Flops for Glitch Avoidance Using Tanner

T.Suganya[1]
PG scholar[1], Department of ECE,
Nandha College of Technology, Erode

Prof.S.P.Kesavan[2]
Professor[2] Department of ECE
Nandha College of Technology, Erode

Abstract

Glitching is a general design problem in systems employing DCDLs. An electronics glitch is an undesired transient that occurs before the signal settles to its planned value. Glitches occupy a large amount in the signal transitions of a circuit. Also glitches are extremely sensitive to delay characteristics. Hence glitch reduction by optimizing delay characteristics is a practical approach for power reduction. Usual approaches for power reduction optimize the sum of capacitive load and short-circuit current based on the transition activity information obtained in advance. In order to reduce the power consumption in circuit, the glitching of DCDLs have to be reduced. The previously proposed Glitch free NAND-Based DCDL circuit using three-state inverter based DCDLs and CMOS transistor logic was designed in a 90nm CMOS technology. The energy stored on the capacitor is degenerate as high temperature and also the delay and failure are more in CMOS transistor logic. In CMOS transistor logic, transistors leak power even when they are not activated and significant power dissipation takes place even during inactive state of circuits. A choice to CMOS transistor logic is the sleep transistor logic in which the operation is to disable entire blocks when not in use. This paper presents a NAND-Based flip flops for glitch avoidance which allows to reduce the peak-to-peak output delay of more than 42%, gate length and power will be reduced and also increase in the speed of operation compared to previously proposed Glitch free NAND-Based DCDL by using three-state inverter based DCDLs and sleep transistor logic have been designed in a 45nm CMOS technology.

1. Introduction

A development in the silicon technology has prepared it possible, the addition of millions of transistor in less area which enabled added functionality into same chip. This rising quantity of functionality finally causes switching operation of the transistor to increase which leads to additional power dissipation. Therefore it is very significant now to think on low power circuits slightly than only high performance circuits. In most recent few years there is extraordinary modify in the advance of the industry, researchers to arrive up with the power efficient devices beside with improved functionality and performance. Static power consumption is a major concern in nanometer technologies. Scaling improves transistor thickness and functionality on a chip. Scaling helps to increase speed and frequency of operation and therefore higher performance. Because voltages scale down by means of the geometries threshold voltages should also decrease to increase the performance advantages of the new technology, but leakage current increases exponentially. Thinner gate oxides have led to an increase in gate leakage current. Along with technology scaling down and higher operating speeds of CMOS VLSI circuits, the leakage power is getting enhanced. As process geometries are becoming smaller, device density increases and threshold voltage as well as oxide thickness decrease to keep pace with performance.

Difficulty for low power and low noise digital circuits has forced VLSI designers to search new approaches to the design of VLSI circuits and growing claim for low-power VLSI can be addressed at special design levels, such as the architectural, circuit, layout, and the process technology level. Power dissipation is an essential concern in the aim of CMOS VLSI circuits. High power consumption leads to go down in battery life in case of battery power applications and affects consistency packaging. If the power consumption is less, then the amount of power dissipation is also less.

In action reduced power consumption extremely reduce the packaging costs and highly increase in the circuit consistency. In order to reach high density and high performance, CMOS technology quality size and threshold voltage have been scaling down for decades. For the reason to facilitate of this trend, transistor leakage power has enhanced exponentially. The leakage power dissipation has grown to be a significant portion of total power consumption for present and upcoming silicon technologies. One of the most important causes of energy dissipation in CMOS circuits is due to the charging and discharging of the node capacitances of the circuits, nearby both as a load and as parasitic. Such part of the total power dissipated by means of a circuit is called dynamic power. In order to decrease the dynamic power, an additional approaches to the traditional technique of power consumption reduction, called sleep transistor logic.

The existing design values requires that activities taking place in various portions of a circuit be matched with respect to an overall signal. This overall signal is usually called the clock. Major between these synchronizing elements are latches and flip flops, which consider the previous input until new data is applied and the clock is asserted. Flip flops are edge triggered. They require a

positive or negative change of the clock to latch the input. A main use of flip flops is in the design of synchronous instruction and arithmetic pipelines. The main information of advantage is the number of transistors, the sum of the areas of all the transistors and the sum of the gate areas of all the clocked transistors.

One of many important factors affecting power consumption is the choice of circuit technique for logic, latches and flip flop. Flip flops largely reducing the power dissipation and increasing the performance, almost double the number of transistors. In modern deep-sub micrometer CMOS processes, time-domain resolution of a digital signal is attractive higher than voltage resolution of analog signals. These argue is nowadays nearly to a new circuit design model in which the conventional analog signal processing is expected to be slowly substituted by the processing of times in the digital domain. Within this new model, digitally controlled delay lines (DCDL) should play the role of digital-to-analog converters in conventional, analog-intensive, circuits. From a more practical point of view, nowadays, DCDLs are a key block in a number of applications, like all-digital PLL (ADPLL), all-digital DLL (ADDLL), all-digital spread-spectrum clock generators (SSCGs) and ultra-wide band (UWB) receivers with ranging feature.

The active power dissipation, which is the main source of power dissipation, is straight forwardly linked to the number of signal transitions in a circuit. A signal transition can be classified into two categories; a functional transition and a glitch. It is identified that glitches occupy a large amount in the signal transitions of a circuit. Also glitches are extremely sensitive to delay characteristics. Hence glitch reduction by optimizing delay characteristics is a practical approach for power reduction. Usual approaches for power reduction optimize the sum of capacitive load and short-circuit current based on the transition activity information obtained in advance.

Recent digital circuits consist of logic gates implemented in the complementary metal oxide semiconductor (CMOS) technology. Power consumption has two components: Dynamic Power and Leakage power. Dynamic and leakage power both are the major contributors to the total power consumption. Dynamic power includes both switching power and short circuit power. Spurious transitions (also called glitches) in combinational CMOS logic are a familiar source of needless power dissipation. Reducing glitch power is a highly desirable target. The dynamic power cannot be eliminated fully, since it is caused through the computing activity.

Static power refers to the power dissipation which results from the current leakage formed by CMOS transistor parasitic. Usually static power has been overshadowed by dynamic power consumption, but as transistor sizes continue to get smaller, static power may go beyond dynamic power consumption. To ease the rising consequence of static power in digital systems, static power reduction technique has been developed. Even with the rising consequence of static power in CMOS circuits, the dynamic power is still the major contributor to power consumption. Dynamic power is mostly consumed by glitches which are the unwanted transitions and need to be eliminated.

In order to reduce the power consumption in circuit, the glitching of DCDLs have to be reduced. Glitching is a general design problem in systems employing DCDLs. Glitch is a temporary fault in a system. It is frequently used to explain a temporary fault that corrects itself, and is so difficult to troubleshoot. The term is particularly common in the computing and electronics industries, and in circuit bending, as well as among players of video games, even though it is applied to all types of systems including human organizations and nature.

An electronics glitch is an undesired transient that occurs before the signal settles to its planned value. In other words, glitch is an electrical pulse of short duration that is usually the result of a fault or design error, particularly in a digital circuit. For example, many electronic components, such as flip flops, are triggered by a pulse that must not be shorter than a specified minimum duration; otherwise, the component may break down. A pulse shorter than the specified minimum is called a glitch. A glitch can occur in the presence of struggle condition in a poorly designed digital logic circuit.

In the most common applications, DCDLs are working to process clock signals; for that reason a glitch-free operation is required. A required condition to avoid glitching is designing a DCDL which have no-glitch in presence of a delay control-code switching. This is an issue at the DCDL-design level. The NAND-based DCDL topology presents a glitching problem. The errors that in some applications can create from DCDL glitching will be also discussed of the NAND-based DCDL. By way of reducing channel length for successive technology generations, threshold voltage and gate oxide thickness are also being scaled down. Leakage current as a result increases exponentially with reduction in threshold voltage. The leakage current is going to be a limiting issue for successive scaling down of transistors. Due to the smaller feature sizes in nanometer technologies, shorter channel lengths cause associate threshold current to increase when the transistor is in the off state.

The lower sub threshold voltage gives rise to increased sub threshold current as well, for the reason that transistors cannot be switched off completely. Because with each successive technology the number of transistors per given area is happening a rise, the leakage power in an integrated circuit for successive generations is increasing, since transistors leak even while they are not activated and large power dissipation takes place even during inactive state of circuits. For to reduce large power dissipation takes place during inactive state of circuits, the sleep transistor is used.

The newly proposed Glitch free NAND-Based DCDL circuit allows reducing the peak-to-peak output jitter of more than 40% with respect to a SSCG using three-state inverter based DCDLs and CMOS transistor. This paper presents a NAND-Based flip flops for glitch avoidance which allows to reduce the peak-to-peak output jitter of more than 42%,gate length and power will be reduced and also increase in the speed of operation compared to previously proposed Glitch free NAND-Based DCDL by using three-

state inverter based flip flops and sleep transistor have been designed in a 45nm CMOS technology.

2. Previously Proposed Glitch Free NAND-Based DCDL

This chapter reviews the previously proposed circuit level approach. In order to compare with the sleep transistor logic approach. Author Davide De Caro says that, the structure of previously proposed DCDL is shown in Fig. 1. In this figure "A" denotes the fast input of each NAND gate. Gates marked by "D", represents dummy cells added for load balancing. Two sets of control-bits, S_i and D_i, control the DCDL. The S_i bits encode the control-code by using a thermometric code:S_i-0 for i<c and S_i-1 for i>c. The bits T_i encode again c by using a one-cold code:T_{c+1}=0,T_i=1 for i ≠c+1. The Fig. 1 shows the state of all signals in the case In=1,c=1.According to the chosen control-bits encoding, each delay-element (DE) can be in one of three possible states. The DEs with i<c are in pass-state. In this state the NAND "3" output is equal to 1 and the NAND "4" allows the signal propagation in the lower NAND gates chain. The DE with i=c is in turn-state. In this state the upper input of the DE is passed to the output of NAND "3". The next DE is in post-turn-state. In this DE the output of the NAND "4" is stuck-at 1, by allowing the propagation, in the previous DE (which is in turn-state), of the output of NAND "3" through NAND "4". All remaining DEs (for i>c+1) are again in turn-state.

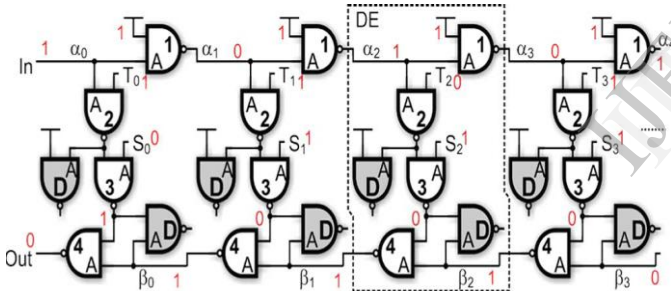

Fig.1.Previously Proposed Glitch-Free NAND-Based DCDLs (non-inverting topology)

TABLE I
Logic-states of each DE in previously proposed DCDLs

S_i	T_i	DE state
0	1	*Pass*
1	1	*Turn*
1	0	*Post-Turn*

In the existing DCDL the state of all α_i and β_i signals depends on the input (α_{2i}=β_{2i}=In and α_{2i+1}=β_{2i+1}=In) with the only exception of β_c, which is stuck-at 1. The glitch-free switching property of the proposed DCDL is conceptually simple to demonstrate. Let us assume a switching of the delay control-code from c=k to c=h. In the initial state of the line, α_{2i}=β_{2i}=In and α_{2i+1}=β_{2i+1}=In, with the exception of β_k, which is stuck-at 1. Let us suppose to first switch the k+1th DE from the post-turn-state to the turn-state. By looking to Fig. 2 it can be observed that, in these conditions, switches from 1 to α_k. The signal β_k is the input of the NAND "4" gate of kth DE. The switching of β_k is glitch-free since the other input of this gate is stuck-at α_k, therefore the NAND "4" output remains equal to α_k. After the k+1th DE switching, all cells are either in pass-state or in turn-state. In these conditions it is possible to freely change the state of DEs from pass-state to turn-state, since this change does not affect the logic state of signals α_i and β_i. After this phase the h+1th DE can be switched from turn-state to post-turn-state. This switching is again glitch free, since only β_h signal switches from α_h to 1.

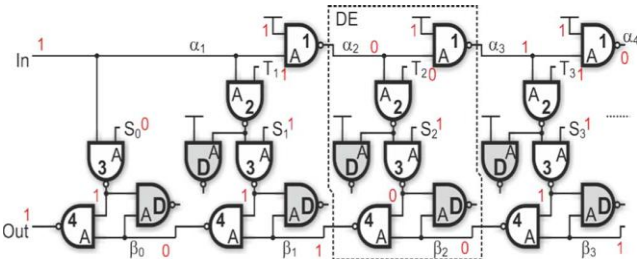

Fig.2.Previouly proposed glitch-free NAND-based DCDLs (non-inverting topology).

This procedure has the drawback to require a three-step switching of the DCDL.The following section provides a more detailed analysis of the glitching of proposed circuit in order to show that a glitch-free operation can also be achieved by using a properly designed two-step switching mechanism.

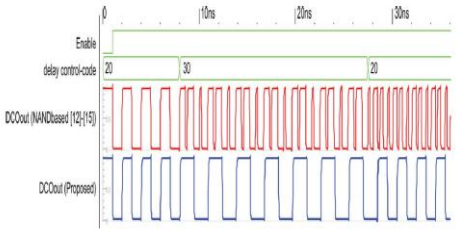

Fig.1 (a).Transient simulation of two ring oscillator DCO designed by using previously proposed NAND based DCDLs

The signal plotted in Fig.1 (a) is the output of previously proposed DCDLs of Fig.1, simulated by using the above described three steps switching mechanism. Note that, in Fig. 1, by increasing the control code by one, two NAND gates are inserted in the signal propagation path between *In* and *Out*. Therefore, the resolution can be written as $t_{NAND\ LH}$+$t_{NAND\ HL}$=2* t_{NAND}.The minimum delay of proposed inverting solution is higher than that of the NAND-based DCDL of existing approach. The circuit of Fig. 1 is an inverting DCDL. In this circuit it is interesting to observe that the first DE is never in post-turn state, therefore is T_0 always 1 (see Table I). This observation allows constructing a non-inverting DCDL by modifying only the first "2" of the first DE have been deleted, together with signal T_0.

The signal α_1 of the second DE is now equal to *In*, therefore the whole behavior of the DCDL is non-inverting. This topology maintains the same of previous solution, while it can easily verified that the minimum delay t_{min} is now $2*t_{NAND.}$ The non-inverting DCDL of Fig. 2, therefore, maintains the same t_R of the NAND-based flip flops of existing approaches, while avoiding its glitching problem.

The glitch-free operation of the previously proposed DCDLs can be obtained with a three-step switching mechanism: for a switching from a delay control code c=k to a delay control code c=h, first, the k+1th DE is switched from post-turn-state to the turn-state; next all DE are switched from pass to turn-state (or vice versa) and finally the DE is switched to post-turn-state. This switching mechanism presents the drawback of being slow and can result in a not simple driving circuit for the flip flop control-bits. Sufficient condition to achieve a glitch-free operation in NAND based DCDL is imposing the following two timing constraints:

$$t_{S\,HL} - t_{T\,LH} > t_{NAND} \quad (2)$$

$$t_{T\,HL} - t_{S\,LH} > -3t_{NAND} \quad (3)$$

Where $t_{S\ LH}$, $t_{T\ HL}$and $t_{T\ LH}$ represents the arrival times of HL and LH switching of and signals, respectively. In order to show how these timing constraints can be, in practice, realized let us define two times, Δs and Δt, as follows:

$$\Delta_s = t_{S\,HL} - t_{T\,LH} \quad \Delta_t = t_{S\,LH} - t_{T\,HL}. \quad (4)$$

By using the above definitions, the two timing constraints becomes

$$\Delta_s > t_{NAND} \quad (5)$$

$$\Delta_t < 3t_{NAND}. \quad (6)$$

Figure 3.Shows the powerful circuits for the control-bits of previously proposed DCDL in that S_i delayed with different LH/HL delays by using clock tree delay and double clock flip flops. This circuit is simpler than NAND based circuit and clock tree delay based circuits.

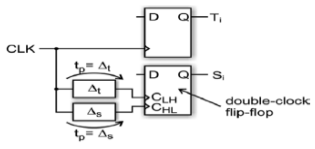

Fig.3.Driving circuits for the control-bits of previously proposed DCDLs using clock tree delay and double clock flip flops.

This solution gives a low circuit complexity. It is possible to achieve a timing margin as high as desired. But this glitch free NAND based DCDL circuit allows reducing the peak-to-peak absolute output jitter of more than the 40% with respect to a SSCG using three-state inverter based DCDLs and CMOS transistor logic.

3. Proposed NAND Based Flip Flops for Glitch Avoidance

In the previous section we have seen that the glitch-free operation of the previously proposed DCDL. This can be reducing the glitches of more than the 40% using CMOS transistor logic. The proposed NAND based flip flops can reduce the glitches of more than the 42% using sleep transistor. The figure (4) shows that structure of NAND gate used in proposed NAND Based flip flops. This circuit can use sleep transistor logic. This logic will reduce glitches, power consumption and gate length more than that of CMOS transistor logic used in previously proposed DCDL.Timing constraints used in proposed are same as used in previously proposed NAND based DCDLs. High power dissipation is one of the major challenges of integrated circuit design in deep submicron and nano scale technologies. The existing method was designed in a 90nm CMOS technology and the proposed method has been designed in a 45nm CMOS technology. The demand for higher functions with higher performance and lower power dissipation initiates the scaling of MOS transistors in every technology generations.

Low power has emerged as a most important topic in today's electronics industry. Require for low power has caused a main usual change, where power dissipation has happen to as important a concern as performance and area. Two components find out the power consumption in a CMOS circuit: Static and Dynamic Power. Static (Leakage) power: includes sub-threshold leakage, drain junction leakage and gate leakage due to tunneling. Among these, sub threshold leakage is the most important one. Dynamic power: Includes charging and discharging (switching) power and short circuit power. In Dynamic power, power consumption due to switching activity is more important. It can be fulfilled from the over discussion so future that glitch and leakage power both are the main contributors to the power consumption.

3.1. Operation of sleep transistor logic

By way of reducing channel length in support of succeeding technology generations, threshold voltage and gate oxide thickness be moreover organism scaled down. Leakage current as a result increases exponentially with decrease in threshold voltage. The leakage current is going to be a limiting factor for successive scaling down of transistors. Owing to the smaller feature sizes in nanometer technologies, shorter channel lengths cause sub threshold current to increase while the transistor is in the off state.

The lower sub threshold voltage gives rise to increased sub threshold current as well, for the reason that transistors cannot be switched off totally. Since by way of every successive technology the amount of transistors per specified area is on a rise, the leakage power in an integrated

circuit for successive generations is increasing, because transistors leak even when they are not activated and large power dissipation takes place even during inactive state of circuits. Therefore it is necessary to decrease static power for the period of the idle or standby mode of operation of the circuits.

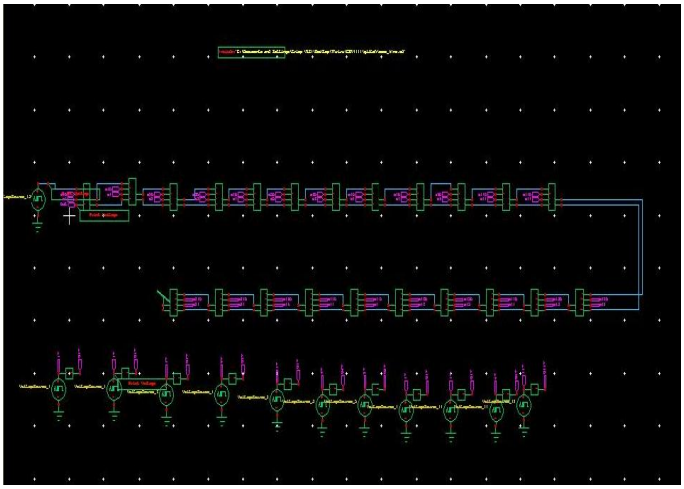

Fig.4.DCDL Structure of Proposed NAND Based Flip Flops

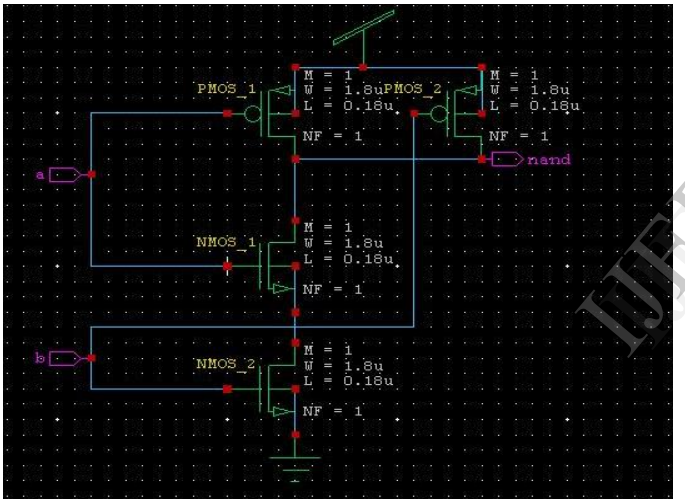

Fig.4.Internal Structure of NAND Gate of Proposed Flip Flop Using Sleep Transistor Logic

There are a number of VLSI techniques to reduce leakage power. Every method provides a well-organized method to reduce leakage power; although disadvantages of every method limit the application of each technique. The new approach is proposed in this work which also reduces total power consumption, accordingly provided that an innovative option to low-leakage power VLSI designers.

The proposed method used to reduce static power consumption is power gating, the use of sleep transistors to disable entire blocks when not in use. Systems which are sleeping for long periods of time and "wake up" to perform a periodic activity are frequently in a remote location monitoring an activity. These systems are usually battery or solar-powered. Power consumption is a key design issue. By shutting down a functional but absorbent block until it is used, leakage current can be reduced extensively. Reducing the total power consumption is essential because it is wanted to make best use of the run time with smallest amount necessities on size, battery life and weight allocated to batteries.

Sleep transistors are essential element in any low leakage power design. In this paper, the sleep transistors can be implemented as Header switch type which achieves the power gating. The header switch is implemented by PMOS transistors to control Vdd supply. PMOS transistor is less leaky than NMOS transistor of a similar size. The NBTI effect increases V_{th} over time and makes PMOS transistor even less leaky. Header switches turn off VDD and maintain VSS on. As the result, it allows a easy design of a pull-down transistor to separate power-off cells and clamp output signals in “0” state. The “0” state isolation is complied with reset state condition in most designs.

The source of one of the sleep transistor is connected to the body of new PMOS sleep transistor for having body biasing effect. So, leakage reduction in this technique occurs in two ways. Firstly, the sleep transistor effect and secondly, the variable body biasing effect. This technique uses aspect ratio W/L=3 for NMOS transistor and W/L=6 for PMOS transistor. Due to the minimum aspect ratio the sub-threshold current reduces. Since the sources of the NMOS sleep transistor is connected to the body of PMOS transistor as shown in Fig. 4, the threshold voltage of the sleep transistors increases due to the body biasing cause during sleep mode. This increase of threshold voltage of the transistors reduces the leakage current. That’s why the static power consumption also lowers.

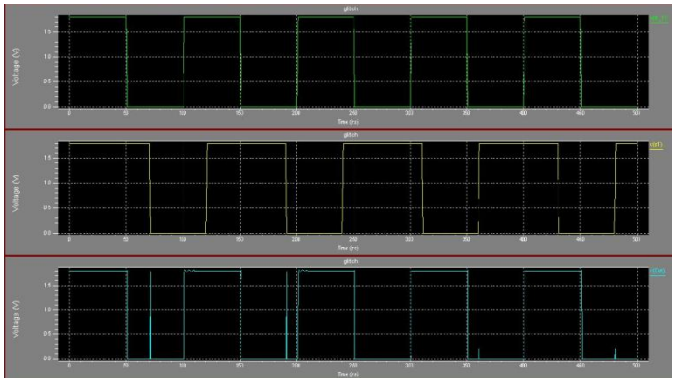

Fig.5. Output of DCDLs of Proposed NAND Based Flip Flop Using Sleep Transistor Logic

The Sleep transistor resistance should be large enough in sleep mode to produce a considerable voltage drop, almost equal to VDD, between GND and Virtual GND. Also the on resistance should be as small as possible as it will have the least effect on discharge path delay and hence on the speed of the circuit. But these requirements always contradict each other because a smaller resistance means wider area of transistor which causes more power consumption so there is always a tradeoff between leakage power saving and speed of the circuit.

4. Results and Discussion

Simulations are obtained in TANNER Tool. First step in obtaining the simulations is to compile the Verilog file in TANNER Tool. Verilog file is created from the circuit diagram, which is designed in the schematic. The Verilog file is now compiled in TANNER Tool. After the compilation of Verilog file, the layout for the circuit diagram drawn in schematic will be generated in TANNER Tool. After that simulations are performed on the layout generated using Verilog files. The results are simulated at room temperature. Glitches present in the O/P and leakage current are main reason now for power consumption.

Since the reduction in leakage current and glitches, there is a extensive reduction in power consumption. The results of proposed method will be Power consumption is reduced, speed in the operation of method is high compared to existing method and delay will be reduced 2% more than that of the existing method and also Gate length will be reduced compared to existing method. Before to evaluate the performances of the flip flop DCDLs, a sequence of simulations to verify the glitching behavior have been performed. The simulation result shows sleep transistor approach is having the least power dissipation as compared to normal CMOS transistor approach. The power Dissipation is decreasing as the process technology scaled down. Owing to scaling of technology, the leakage current as well present. Power consumption is owing to both the leakage current and unwanted transitions. The reduction in power consumption and glitches are observed from the output of DCDLs of proposed NAND based flip flop using sleep transistor logic.

5. Conclusion

During nanometer scale CMOS technology, sub-threshold leakage power consumption is an enormous test. Even though previous approaches are efficient in a number of ways, no great result for reducing power consumption in upcoming nanometer scale CMOS technology. Therefore, designers select techniques based upon technology and design criteria. Scaling down of device dimensions, supply voltage and threshold voltage for achieving high performance and low dynamic power dissipation has basically contributed to the raise in leakage power dissipation. Scaling along of the technology has led to increase in leakage current. Currently, a leakage power has happen to additional dominant as compared to Dynamic power. But, Dynamic Power consumption due to glitches can't be neglected.

Therefore, in this paper, the efficient technique has been proposed for reducing glitch and leakage power reduction in CMOS VLSI Circuits. This paper presented an efficient design methodology for reducing the power dissipation in NAND based flip flop design. The proposed technique is more effective in reducing power consumption. The result is simulated with TANNER software in 45nm CMOS technology. This paper proposes a sleep transistor logic used in NAND gate for low power consumption. The results show that the proposed techniques has less power dissipation compared to conventional CMOS design with less transistor count. These advantages made these logics more convenient for energy efficient digital applications.

The basic concept of sleep transistor logic circuit design process is described. Utilizing the basic sleep transistor logic of header type inverter/buffer, the D flip flop is implemented and analyzed. From the simulations, the functionality of the implemented flip flop set up to be reasonable**.** The simulation results confirm the suitability of developed model and shows that proposed solutions improve the resolution with respect to previous approaches. The use of proposed NAND based flip flop allowed to reduce the peak-to-peak output delay of more than 42%, gate length and power will be reduced and also increase in the speed of operation compared to previously proposed Glitch free NAND-Based DCDL by using inverter-based DCDLs and sleep transistor logic.

6. References

[1] Pushpa Saini and Rajesh Mehra, "A Novel Technique for Glitch and Leakage Power Reduction in CMOS VLSI Circuits," International Journal of Advanced Computer Science and Applications, Vol. 3, No. 10, 2012

[2] Kaijian Shi and David Howard, "Sleep Transistor Design and Implementation – Simple Concepts yet Challenges To Be Optimum," Kaijian.Shi@synopsys.com, David.Howard@arm.com

[3] Hina malviya,Sudha Nayar and C.M Roy, "A new approach for Leakage Power Reduction Techniques in Deep Submicron Technologies in CMOS CIRCUIT for VLSI Applications," International Journal of Advanced Research in Computer Science and Software Engineering, Volume 3, ISSN: 2277 128X, Issue 5, May 2013

[4] H.P. Rajani, Srimannarayan Kulkarni and M.S. Ramaiah, "Novel Sleep Transistor Techniques for Low Leakage Power Peripheral Circuits," International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.4, August 2012

[5] B. Dilli Kumar, 2A. Chandra Babu, 2V. Prasad, "A Comparative Analysis of Low Power and Area Efficient Digital Circuit Design," International Journal Computer Technology & Applications, Vol 4 (5), 764-768, ISSN: 2229-6093

[6] L.Wang , L. Liu, and H. Chen, "An implementation of fast-locking and wide-range 11-bit reversible SAR DLL," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 6, pp. 421–425, Jun. 2010.

[7] R. J. Yang and S. I. Liu, "A 40–550 MHz harmonic-free all digital delay locked loop using a variable SAR algorithm," IEEE J.Solid-State Circuits, vol. 42, no. 2, pp. 361–373, Feb. 2007.

[8] R. J. Yang and S. I. Liu, "A 2.5 GHz all digital delay locked loop in 0.13mm CMOS technology," IEEE J.Solid-State Circuits,vol.42,no. 11, pp. 2338–2347, Nov. 2007.

[9] S. Kao, B. Chen, and S. Liu, "A 62.5–625-MHz anti reset all digital delay locked loop," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 54, no. 7, pp. 566–570, Jul. 2007.

[10] A. G. M. Strollo, D. De Caro, E. Napoli, and N. Petra, "A novel high speed sense amplifier based flip-flop," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 11, pp. 1266–1274, Nov. 2005.

[11] B. S. Kong, S. S. Kim, and Y. H. Jun, "Conditional-capture flip-flop for statistical power reduction," IEEE J. Solid-State Circuits, vol. 36, no. 8, pp. 1263–1271, Aug. 2001.