Class-C Inverter Power Optimization Technique For Second Order Sigma Delta Modulator

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Abstract

This paper presents a complete implementation of second order sigma delta modulator with power optimization technique namely offset cancelled integrator using Class-C inverter in popular Tanner tool. The second order sigma delta modulator is implemented with two stage CMOS op-amp followed by offset cancelled integrator using Class-C inverter, comparator, D-flip flop and digital to analog converter (DAC). In this case the power spectral density and average power consumption has been found out for the circuit. Average power consumption with offset cancelled integrator using Class-C inverter technique is 0.14037pW for simulation time from 0 to 1ms which is very less. The circuit is designed with 0.18µm CMOS process technology with supply voltage of 1 volt and signal frequency of 3 KHz. Such a circuit with low power requirement can be used for biomedical and other applications.

1. Introduction

With the scaling down of modern VLSI technologies, more complicate digital circuits have been implemented with a higher clock rate and lower supply voltage, which introduces more constraints for the analog circuits. Therefore, the design of low-voltage, low-power analog circuitries has become more important. Because of powered by batteries, the supply voltage is often limited, and the life time of the battery is of great importance for these devices, and all these factors address the requirements of low-power system building blocks. However, the decreased supply voltage restricts the signal swing in circuits and brings difficulties for analog circuit design. In low-voltage environments, the transistor characteristics degrade and some circuit techniques can no longer be used, thus the low-voltage design is different from the traditional circuit design technique.

In the sigma−delta modulator, the difference between the analog input signal and the output of the DAC is the output of the summer. This difference is given as an input to the integrator. The integrator integrates over each clock period. The clock is at a much higher frequency than the input sinusoid, causing the sine wave to be approximately flat over the clock period. The integration of the pulse difference is linear over one clock period. The output of the integrator represents an accumulation of the error term between the input and the DAC output.

This integral then digitized by a clocked quantizer, and the quantizer output is the output of the sigma−delta modulator. In the feedback path, the DAC shifts the logic level so that the feedback term matches the logic level of the input; making the difference equally weighted. The transient output of the sigma−delta modulator is a pulse density modulated signal that represents the input sine wave. This waveform is more dense with digital ones when the signal represented is high and less dense when the waveform is low. The three main performance measures of an ADC are its resolution (usually number of bits), its speed (how many conversions it does per second), and its power consumption, where customarily it is desired that the first two of these be maximized and the third minimized.

A second order sigma-delta modulator can be derived by placing two integrators in series as shown in Figure 1.

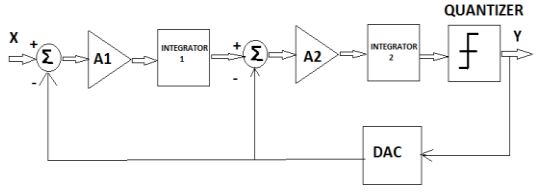

Figure 1: Block diagram of second order sigma delta modulator

Among different ADC topologies, the Sigma-Delta ADCs efficiently trade speed for accuracy, providing an efficient way to implement high-resolution ADCs without stringent matching requirements compared to other types of ADCs (ex: flash ADC, pipeline ADC) in audio band applications. Therefore, the sigma-delta ADCs are more power-effective and robust compared to other architectures.

There are many power optimization techniques for second order sigma delta modulator. One of the efficient technique is offset cancelled integrator using Class-C inverter technique which is described in detail in section 2. Other building blocks of sigma delta modulator are described in section 3. Circuit simulation details and experimental parameters are described in sections 4 and 5 respectively. Finally the conclusion is given in section 6.

2. Class-C Inverter Power Optimization Technique

A traditional cascaded class-C inverter is shown in Figure 2. The supply voltage (*V*DD) is chosen to be slightly lower than the sum of the threshold voltage (*V*TH) of the input transistors M1 and M2, and the two input transistors both operate in a sub-threshold region when the common mode voltage *V*CM = *V*DD/2 is inputted. Hence the circuit consumes very less power [1].

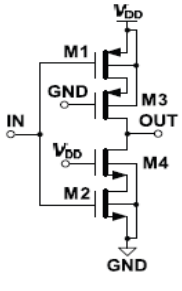

Figure 2: Schematic of Class-C Inverter

In inverters, the virtual ground voltage can be defined by the offset voltage of inverters which is determined by the size of the MOS transistors in inverters. However, the unknown offset of the inverter impairs modulator performances. Thus, the offset has to be cancelled by the offset cancellation techniques. The offset cancelled integrator using inverter is shown in Figure 3.

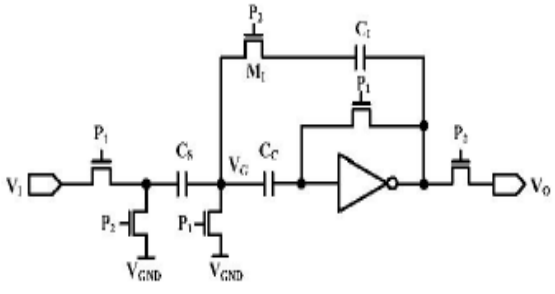

Figure 3: Offset Cancelled Integrator Using Inverter

It is common to use the inverter with transistors operating in the strong inversion region. However, the static short circuit current from VDD to VSS consumes large amount of power. If the power supply voltage (VDD) is chosen to be lower than the sum of the threshold voltages VTH of NMOS and PMOS, then the inverter behaves as a class-C amplifier that minimizes static current. Here, the supply voltage of the modulator is chosen to 1.2V, because the VTH of transistors is 0.662V and -0.7V respectively for the NMOS and PMOS of the inverter [6].

During P1 phase, sampling capacitor Cs is charged to input voltage VI. The offset cancellation capacitor Cc is charged to the offset voltage VOFF of the inverter but the integration charge in CI is not lost because the transistor Ml is open. At this phase, both transistors in inverter are turns off. Actually, the all transistors operate in weak inversion region. At the beginning of P2 phase, the inverter input voltage is increased or decreased to VI+VOFF. One of transistors is turned on while the other transistor is completely off at this moment. Since the input voltage of inverter should return to VOFF due to the negative feedback loop, the charge in Cs is transferred into Cl. Then the inverter input voltage goes back to VOFF and the both transistors are turned off again. Since only one transistor is turned on and operates in the strong inversion region during transition, high slew is obtained with a minimal amount of the short circuit current. On

the other hand, both transistors are operating in the weak inversion region during P1 phase with the minimum static current. This operation allows for high slew rate during the transition period and maintains the minimum static power consumption. The proposed integrator cell presents only a half delay to the signal. The transfer function of this integrator is:

$$H(z) = \frac{z^{-1/2}}{1-z^{-1}}$$

3. Other Building Blocks

A. Two Stage CMOS Op-Amp

To avoid closed-loop instability, frequency compensation is necessary in op-amp design. For two-stage CMOS op-amp, the simplest compensation technique is to connect a capacitor across the high gain stage. This results in the pole splitting phenomena which improves the closed-loop stability significantly. However, due to the feed-forward path through the Miller capacitor, a right-half-plane (RHP) zero is also created. In theory, such a zero can be nullified if the compensation capacitor is connected in conjunction with either a nullifying resistor or a common-gate current buffer as shown in Figure 4 [14].

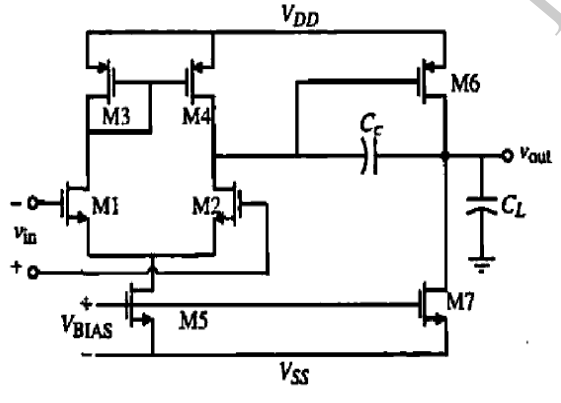

Figure 4: Two Stage CMOS Op-Amp Circuit

B. Comparator

A comparator acts as the quantizer in the sigma delta modulator. Since the comparator is of 1-bit it has only two levels either a '1' or a '0'. A '1' implies that VDD = + 2.5V and a '0' implies that VSS = - 2.5V. If the output of the integrator is greater than the reference voltage (Vref) is has to give an output of '1' and if the integrator output is less than reference voltage then the output of the comparator should be '0'. A simple comparator performs the required function efficiently. Given a reference level, a comparator gives an output of VDD when the signal is greater than the reference level and an output of VSS when signal is less than reference level. In this design the Vref = 0V. The operational amplifier can be used as a comparator. The only change needed is that the comparator doesn't require the compensation capacitor which is required by the operational amplifier. The comparator circuit is shown in Figure 5. The comparator in the modulator will be driving the 1-bit DAC and also any buffer present at the output of the modulator.

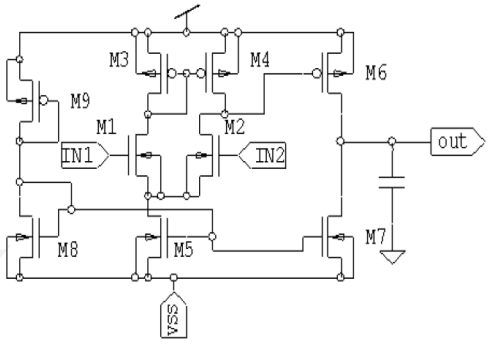

Figure 5: Comparator Circuit

C. D-Flip Flop

The circuit level design D flip-flop used in the sigma delta modulator design is as shown in Figure 6. D flip-flop acts as a sampler which latched the input for one clock period. Here we apply the output of comparator to the d input of the circuit, and takes the output from q & qbar. It is generally an edge-triggered flip-flop which gives output for the positive transition of the clock and operated with oversampling clock.

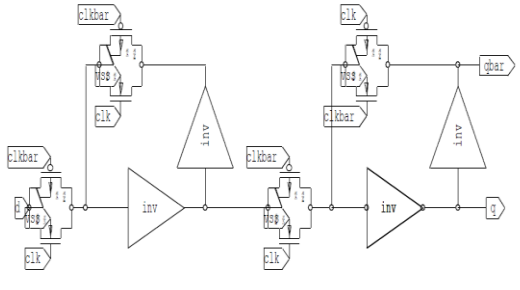

Figure 6: D Flip-Flop Circuit

D. Digital to Analog Converter (DAC)

The digital to analog converter is necessary to convert the digital signal into analog signal at the output and is to be subtracted from the input. The DAC must reference the feedback signal in the modulator so that the difference at the amplifier does not saturate the amplifier. The DAC consists of two transmission gates and two pairs of resistors as shown in Figure 7. The gate of the NMOS transmission gate 1 is tied to the gate of the PMOS on transmission gate 2. Likewise, the gate of the PMOS on transmission gate 1 is tied to the gate of the NMOS on transmission gate 2. The first pair of gate is driven by q from the output of D flip-flop. The second pair of gates is driven by qbar from the output of the D flip-flop. qbar is the inverse of q, so this design turns only one transmission gate ON at a time. The input to each transmission gate is a voltage divided down from the positive and negative rails. This voltage division is accomplished using resistor tied to ground and a resistor connected to the respective rail.

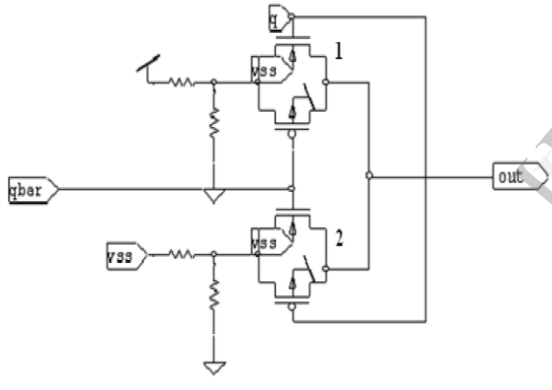

Figure 7: DAC Circuit

4. Circuit Simulation

The second order sigma delta modulator using Class-C inverter is implemented in popular Tanner software. Block diagram of second order sigma delta modulator using Class-C inverter is shown in Figure 8. It consists of Op-amp with Class-C inverter, Comparator, D Flip-Flop and DAC. Supply voltage of 1 Volt with frequency of 3 KHz is applied at the input. Each block has its circuit designed individually on Tanner and then called the instances for making the total circuit block.

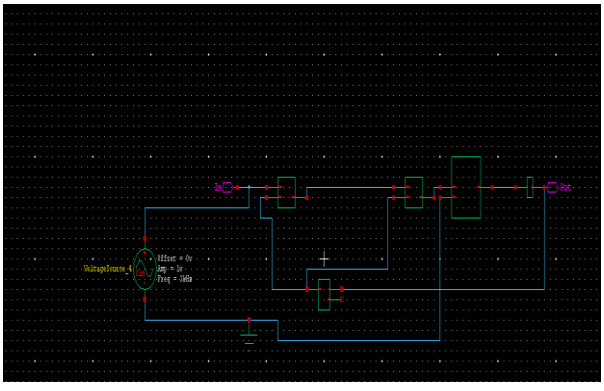

Figure 8: Snapshot of second order sigma delta modulator using Class-C inverter in Tanner

After simulation of the second order sigma delta modulator using Class-C inverter circuit in Tanner, the analog signal is converted into digital with low power consumption of the circuit. Simulation result of second order sigma delta modulator using Class-C inverter circuit is shown in Figure 9.

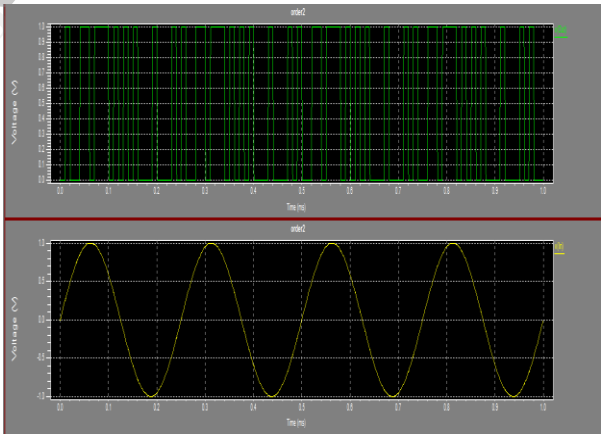

Figure 9: Simulation result of second order sigma delta modulator using Class-C inverter in Tanner

Power Spectral Density of second order sigma delta modulator using Class-C inverter is also plotted using Tanner which is shown in Figure 10.

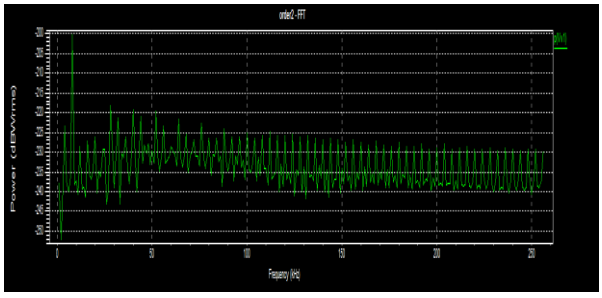

Figure 10 Power Spectral Density of second order sigma delta modulator using Class-C inverter in Tanner

5. Experimental Parameters

The second order sigma delta modulator using Class-C inverter is designed by using 0.18um CMOS process. All main parameters of the described modulator are summed up in Table I along with comparison with previous work.

TABLE I

Parameters	Value	Previous Work
Technology	0.18µm CMOS	0.35µm CMOS
Order Of Modulator	2	2
Supply Voltage	1 V	1.2 V
Signal Frequency	3 KHz	2KHz
Average Power Consumption	0.14037 pW	5.6 µW
Quantizer Resolution	1-Bit	1-Bit

6. Conclusion

In battery operated systems used for bio-medical and other applications, it is of utmost importance that the power consumption is kept to a minimum and this is generally achieved by running the IC's at the lowest possible supply voltage required for the necessary frequency. In this paper a low power second order sigma delta modulator using Class-C inverter is implemented in Tanner tool with 0.18um CMOS process technology which operates with 1 volt supply voltage and consumes 0.14037 pW average power for simulation time from 0 to 1ms.

7. References

[1] Hao Luo, Yan Han, Xiaopeng Liu, Guo Liang, and Lu Liao "An Audio Cascaded ∑Δ Modulator Using Gain-boost Class-C Inverter", 978-1-4577 1997-4/11, 2011 IEEE.
[2] H. Luo, Y. Han, et al. "Bulk-compensated technique and its application to subthreshold ICs," Electronics Letters, vol. 46, no. 16, pp.1105-1106, Aug., 2010.
[3] Y. Chae and G. Han, "Low voltage, low power, inverter based switched-capacitor delta-sigma modulator," IEEE J. Solid-State Circuits, vol. 44, no. 2, pp.458-472, Feb., 2009.
[4] Chen Yueyang, Zhong Shun'an, Dang Hua "Design of A low-power consumption and high-performance sigma-delta Modulator", in 2008 World Congress on Computer Science and Information Engineering, 978-0-7695-3507-4/08, 2008 IEEE.
[5] Guo-Ming Sung, Chih-Ping Yu, Dong-An Yao "A Comparison of Second-Order Sigma-Delta Modulator Between Switched-Capacitor and Switched-Current Techniques", in 978-1-4244-2342-2/08, 2008 IEEE.
[6] Youngcheol Chae and Gunhee Han "A Low Power Sigma Delta Modulator Using Class-C Inverter", in 2007 Symposium on VLSI circuits Digest of Technical Papers.
[7] Adnan GuLndel, William N. Carr "A Micro Power Sigma-delta A/D Converter In 0.35-gm Cmos For A Low Frequency Applications", in IEEE 2007.
[8] J. Goes, B. Vaz, R. Monteiro and N. Paulino, "A 0.9V ΔΣ Modulator with 80dB SNDR and 83dB DR Using a Single-Phase Technique," ISSCC Dig. Tech. Papers, pp.74-75, Feb. 2006.
[9] K.-P. Pun, S. Chatterjee and P. Kinget, "A 0.5V 74dB SNDR 25kHz CT ΔΣ Modulator with Return-to-Open DAC," ISSCC Dig. Tech. Papers, pp.72-73, Feb. 2006.
[10] E.Lopez-Morillo, R.G.bCarvajal, H. ElGimili "A Very Low Power Class AB/AB Op-Amp Based Sigma Delta Modulator for Biomedical Applications" , in 2006 IEEE.
[11] K. Nam, S.-M. Lee, D. K. Su, and B. A. Wooley, "A Low-Voltage Low- Power Sigma-Delta Modulator for Broadband Analog-to-Digital Conversion," IEEE J. Solid-State Circuits, vol. 40, no. 9, pp.1855-1864, Sep. 2005.
[12] Youngcheol Chae, Minho Kwon and Gunhee Han "A 0.8-µW Switched Capacitor Sigma-Delta Modulator Using A Class-C Inverter", ISCAS 2004, 0-7803-8251-X/04, 2004 IEEE.
[13] L. Yao, M. Steyaert and W. Sansen, "A 1V 88dB 20kHz Sigma-Delta Modulator in 90nm CMOS," ISSCC Dig. Tech. Papers, pp.80-81, Feb. 2004.
[14] Phillip E. Allen, Douglas R. Holberg "A Text Book on CMOS Analog Circuit Design", Second Edition, Oxford Press University, Page 269,273.