Comparative Review of 5T, 4+2T, 7T and 8T SRAM Cell Designs

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Abstract—The study provides a comprehensive analysis of different configurations of Static RAM, with a specific emphasis on the 4+2T, 5T, 7T, and 8T architectures. By doing thorough analysis, we carefully study the specifications and performance metrics of each configuration, which allows us to gain useful insights into their unique qualities. The parameters of cell area scaling, array size, array efficiency, and read/write characteristics are thoroughly assessed, enabling a detailed comprehension of the advantages and disadvantages inherent in each design. This concentrated analysis not only improves our comprehension of memory design but also establishes the foundation for future progress in computer systems. This research makes a substantial contribution to the continuous development of memory technologies and their incorporation into modern computing architectures by enhancing our understanding of SRAM configurations and their consequences.

Keywords—SRAM, 5T, 4+2T, 7T, 8T, comparative analysis, specifications, performance metrics, area efficiency

I. Introduction

The Static RAM (SRAM) is a fundamental component of contemporary computer systems, functioning as the main storage for important data in a wide range of applications, including personal computing devices and complex data centers. Among the several types of SRAM, the 5T, 4+2T, 7T, and 8T configurations are popular choices due to their distinct advantages and trade-offs in important areas such as size efficiency, speed, power usage, and stability. This study aims to do a thorough comparison of these configurations, highlighting their individual specifications and performance indicators.

The 5T SRAM architecture emphasizes compactness and low power consumption, making it an appealing choice for applications that demand great density and energy economy. In contrast, the 4+2T, 7T, and 8T variants incorporate extra transistors to improve stability and read/write capabilities. Understanding the complexity of these setups is crucial for designers and engineers attempting to optimize memory subsystems for varied computing environments.

Through a comprehensive evaluation of critical metrics like access time, leakage current, read and write stability, and area efficiency, this paper tries to highlight the strengths and limitations of each SRAM arrangement. By giving insights into the intricacies of the 5T, 4+2T, 7T, and 8T SRAM designs,

this work contributes to the current discourse on memory design, aiding breakthroughs in future computing systems.

II. Literature Survey

The face recognition accelerator in [1] uses a mostly-read 5T memory design to minimize bitcell area, increase voltage scalability, and improve read reliability. This hybrid search technique allows for efficient face detection. At 100MHz and 0.6V, it finds 93% detection accuracy and 81% classification accuracy with a power consumption of 23mW. The system can be difficult to scale for larger datasets or real-time applications, and it has disadvantages such as intermittent memory updates and limited adaptation to changing databases. The accelerator uses SVM and cascaded classifiers to identify and classify faces. By 7.2% less bitcell area than 6T designs, the memory design allows for large voltage scaling and low power operation. At 100MHz and 0.6V, read energy consumption is 0.103pJ/bit.

In parallel, the realm of SRAM cell innovation witnesses the emergence of novel designs such as the 4+2T SRAM cell, as discussed by [2]. This design paradigm strategically divides the VDD terminals, fostering enhanced energy efficiency, while ingeniously leveraging N-well as the word-line. Empirical findings presented by [2] demonstrate tangible improvements in energy and frequency performance, a testament to the viability of such innovative approaches. These include novel topologies like loadless and driverless SRAM cells, strategically crafted to augment both performance and stability in demanding operational environments. However, as highlighted by [3], the intricacies of optimizing SRAM cell design become evident upon delving into essential parameters and the delicate balance of trade-offs between stability, power

consumption, access time, and area.

To decrease AxVDDmin, the proposed L-shaped 7T SRAM architecture depicted in [4] uses novel strategies such as offset cell VDD biasing, boosted BL, and asymmetric-VTH read-port. This yields an impressive 260mV VDDmin, a noteworthy 9x greater read-BL swing than earlier devices. The accomplishment shows significant improvements in SRAM design with 50% lower AxVDDmin than traditional 8T cells. Certain suggested approaches, like as the offset cell VDD biasing technique, have significant power and area overheads that could affect overall efficiency even though they preserve a compact cell layout topology with less than a 15% increase in cell size. Even though the L7T design reduces AxVDDmin and improves sensing capabilities, more research is necessary to resolve any potential trade-offs or implementation difficulties. All things considered, the L-shaped 7T Array, with its improved performance and efficiency, marks a major advancement in SRAM technology.

The suggested SRAM design described in [5] incorporates a number of modifications to improve effectiveness and performance. Buffered read operations remove SNM limitations and peripheral hardware reduces bitline leakage. For write operations, sub-threshold processes are optimized, and sense amplifier redundancy reduces mistakes by increasing error probability, decreasing offset, and mitigating the effects of global variation. Read buffer optimization requires sharing foot-drivers amongst cells in order to efficiently drain read current in order to sense at low voltages. An 8T SRAM bit-cell has sense amplifier redundancy for sub-threshold operation to reduce mistakes. It is possible to operate at low voltages (350 mV) with less power usage. But there are disadvantages as well, like higher overhead from redundant sensing amplifiers and difficulties choosing and maintaining redundant sense amplifiers, which limits scalability when increasing redundancy for error reduction.

III. Analysis of SRAM

Understanding the functionality of Static Random-Access Memory (SRAM) entails analyzing the intricate interactions among its essential components, each indispensable for its proper operation. The core of this analysis is the basic design of SRAM cells, which are often made up of bistable flip-flop circuits made from cross-coupled inverters. In the absence of power, these flip-flops act as the fundamental storage devices, resolutely holding binary data as electrical charges. In this architecture, consideration is given to the critical functions and roles of necessary parts such as Bit Lines, Word Lines, Storage Nodes, Access Transistors, and Sense Amplifiers.

The significance of Bit Lines as channels for data transfer is acknowledged, as is their importance in enabling the smooth passage of electrical impulses into and out of the SRAM cell. Similarly, it is mentioned how crucial Word Lines are to controlling access to certain SRAM cells and acting as gatekeepers to allow read and write operations. The functionality made possible by Access Transistors—gateways that control data flow between Bit Lines and Storage Nodes—is painstakingly dissected in this examination.

Moreover, the complex function of Sense Amplifiers during read operations is discussed, clarifying how they detect and amplify the voltage differential across the Bit Lines. The process's output is the proper categorization of recorded data as logic high or logic low. Also, the analysis of write operations exposes the intricate procedure by which data is written on Bit Lines and subsequently transferred into Storage Nodes upon activation of the corresponding Word Line.

This thorough investigation reveals the intricate workings that support SRAM's operation and illuminates the varied functions and relationships of its essential components. With this thorough understanding, the field of memory technology will be further advanced through the research and investigation of SRAMs with different transistor counts and creative design paradigms.

IV. Study of Various SRAM Configurations

A. 5T SRAM

Often used in integrated circuits, 5T SRAM, also known as 5-Transistor SRAM, shown in Fig.1 is a memory cell architecture that incorporates components from both 4T and 6T SRAM architectures. It has five transistors in total and provides a number of important functions. By adding more transistors, the stability is improved and it becomes less vulnerable to noise and process fluctuations than 4T SRAM. Extra transistors also aid in reducing leakage currents, which improves overall dependability and energy efficiency. Between the stability and performance of 6T SRAM [6] and the compact layout of 4T SRAM, 5T SRAM offers a well-balanced compromise. Nevertheless, compared to 4T SRAM, it has more complexity and area overhead, which could affect manufacturing yield and cost. Despite being smaller than 6T SRAM, 5T SRAM's additional transistors still need more silicon area, which restricts its use in applications with limited space. 5T SRAM is frequently used in high-performance computing systems, such as CPU caches and on-chip memories, where speed and stability are critical requirements. Its capacity to regulate leakage currents also makes it appropriate for power-efficient designs, such as those seen in IoT and mobile devices.

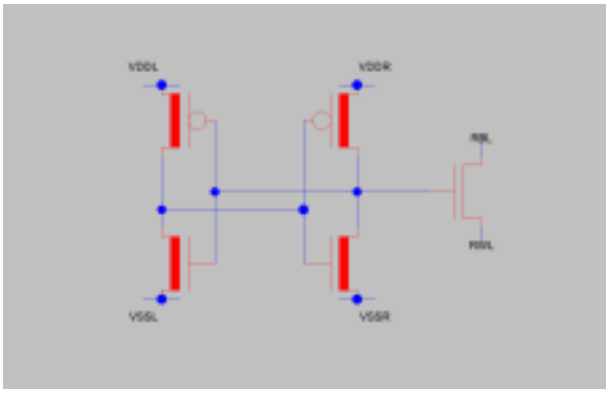

Fig. 1. A schematic of 5T SRAM cell.

B. 4+2T SRAM

For improved performance and efficiency, the 4T+2T SRAM cell incorporates features from both 4T and 6T SRAM cells. It is composed of two access transistors and two cross-coupled inverters in a 4T component, and more access transistors in a 2T portion. The 2T part increases the read signal while the 4T section maintains stability during read operations. In a similar vein, the 2T section improves stability and reliability during write operations while the 4T portion saves data. In comparison to 4T cells, this design offers better read stability and reliability. It also has less area overhead than 6T cells, which could result in lower power usage. Fig.2 shows the schematic of the 4+2T SRAM. It does, however, also come with drawbacks, such as heightened design complexity and susceptibility to changes in the process. Applications for the 4T+2T SRAM cell include IoT devices and mobile devices, which call for a balance of performance, power, and space. In order to improve performance and efficiency, future advancements might concentrate on integrating cutting-edge techniques and performing additional optimization for certain applications. All things considered, the 4T+2T SRAM cell holds out hope for effective memory solutions that have better qualities than conventional architectures.

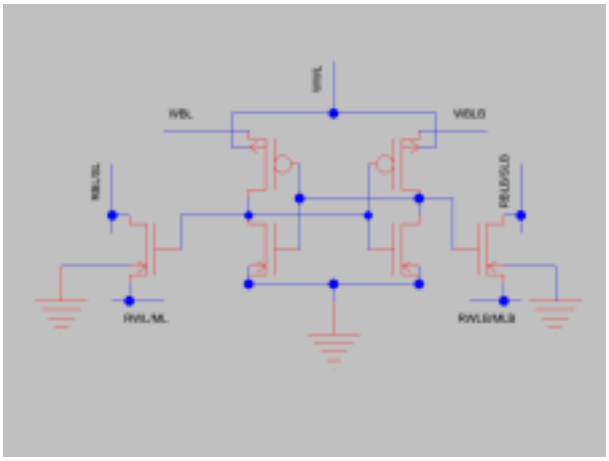

Fig. 2. 4+2T SRAM

C. 7T SRAM

Seven transistors make up the memory cell design known as 7T SRAM, or 7-Transistor SRAM, which is frequently used in integrated circuits. It provides a harmony between power efficiency, performance, and stability. Enhanced stability and dependability are attained by adding more transistors, which strengthen the cross-coupled feedback loop and lessen the device's vulnerability to noise and process fluctuations. Adding more transistors also helps to reduce leakage currents, which improves dependability and energy efficiency. When compared to more intricate memory cell designs, 7T SRAM still offers a comparatively high density even though it is larger than 6T SRAM as seen in Fig.3. The supplementary transistors result in greater area overhead, which limits its usability in applications with limited space. Other challenges include the added complexity that may affect manufacturing yield and cost. High-performance computer systems, where speed and stability are critical, including register files and cache memory in CPUs, are common uses for 7T SRAM. Furthermore, because of its capacity to control leakage currents, it is appropriate for low-power and energy-efficient designs, such as those seen in mobile and Internet of Things applications.

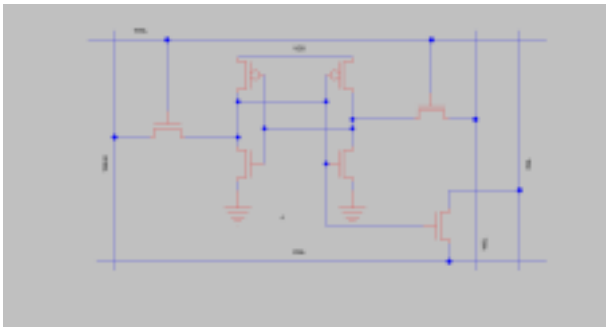

Fig. 3. A schematic of 7T SRAM cell.

D. 8T SRAM

Eight transistors make up the memory cell design known as 8T SRAM, or 8-Transistor SRAM, which is widely used in integrated circuits. It provides more stability and adaptability than devices with a lower transistor count. The cross-coupled feedback loop is strengthened with additional transistors, which improves stability and reliability. Additional control transistors further minimize leakage current, and the additional transistors enable better read and write capabilities. Fig.4 shows a schematic design of 8T SRAM cell. The complexity of manufacturing and the higher silicon area needed for 8T SRAM are challenges that can affect yield and cost. High-performance computer systems where speed, stability, and reliability are crucial, including CPU caches and register files, are common uses for 8T SRAM. It is also appropriate for low-power and energy-efficient designs, such as mobile devices and Internet of Things applications, due to its capacity to control leakage currents.

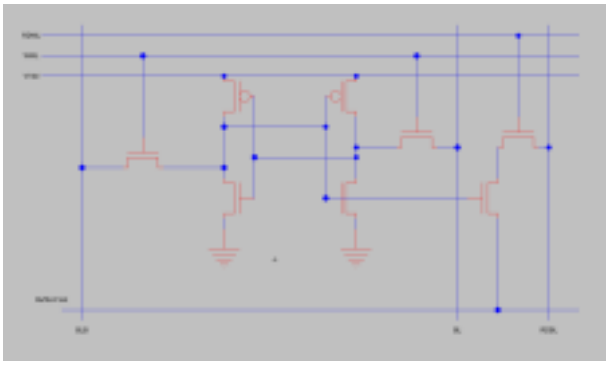

Fig. 4. A schematic of 8T SRAM cell.

V. Results And Discussion

A. Technology Employed

The performance, power consumption, and efficiency of SRAM cells are inextricably connected to the semiconductor technology employed in their manufacturing. As technology

TABLE I. Comparison of SRAM configurations

SRAM Variant		5T	4+2T	7T	8T
Technology		40nm	55nm	65nm	65nm
Operational Mode		SRAM	SRAM/CAM	SRAM	SRAM
Memory Capacity		4Mb	16 Kb	32 Kb	256 Kb
Area Efficiency		1.08	0.89	0.87	0.77
Array Efficiency		0.56	0.64	0.45	NA
VDD_{min} (Read/Write) in mV		380	250	260	350
Read	Energy in fJ/bit	NA	5.5 (0.25V)	NA	1240 (0.35 V)
	Frequency in MHz	NA	6 (0.25V)	NA	0.025 (0.35 V)
Write	Energy in fJ/bit	103 (0.6 V)	4.9 (0.25V)	44 (0.26 V)	880 (0.35 V)
	Frequency in MHz	100 (0.6 V)	4 (0.25V)	1.8 (0.25 V)	0.025 (0.35 V)

nodes shrink, transistors within these cells similarly reduce in size, enabling larger integration densities and the promise of increased performance. This downsizing holds the potential to augment the speed and efficiency of SRAM operations. However, the journey to smaller transistors isn't without its obstacles. One prominent concern is the increase of leakage currents [7], which can compromise power efficiency and worsen heat dissipation issues. Additionally, the manufacturing process becomes more intricate with smaller features, demanding better precision and introducing complexity that can effect yield rates and production costs. Thus, while developments in semiconductor technology offer exciting potential for SRAM development, they also demand careful consideration of these associated issues to assure optimal performance and reliability.

B. Cell Area Scaling

Cell area scaling serves as a critical criterion for analyzing the efficiency of different SRAM layouts. By comparing the area of each configuration to a standard reference, often the 6T SRAM cell, this scaling provides useful insights into the relative compactness of each architecture. A scaling factor greater than 1 suggests a bigger area demand, whereas a value below 1 denotes a more space-efficient design.

In this perspective, the 5T configuration stands out for its amazing efficiency, since it exhibits the smallest cell area when scaled to the standard 6T cell. This means that the 5T arrangement occupies less physical space compared to other configurations, making it an appealing alternative for situations where area minimization is critical. This better area efficiency means that the 5T arrangement could potentially give advantages in terms of overall chip size, manufacturing cost, and power consumption. Therefore, in the arena of SRAM design, careful consideration of cell area scaling is vital for selecting the most space-efficient and cost-effective solutions.

C. Pushed - Rule Cell

The metric discussed here offers insights into whether a given SRAM configuration has been maximized according to fabrication criteria. When a configuration is pushed to its limitations, it means that designers have pushed the boundaries of what is technically viable within the confines of manufacturing regulations. However, this ambitious approach can also pose possible issues in layout design, fabrication yield, and general manufacturability.

In the instance of the 4+2T configuration being pushed to its boundaries, it shows that designers have optimized the arrangement to its utmost extent, potentially leveraging every available opportunity to boost performance or minimize area. While this method may offer benefits in terms of functionality or efficiency, it also presents difficulties regarding the practical implementation of such a design. Challenges in layout design may develop because to the intricate arrangement of components, while issues in fabrication yield could result from the intricacy of manufacturing techniques necessary to obtain the desired configuration. Pushing a setup to its boundaries represents a difficult balance between innovation and practicality. While it may result in breakthroughs in SRAM technology, it also underlines the significance of resolving potential issues in layout, fabrication, and manufacturability to assure the viability and durability of the final product.

D. Memory Array Size

The size of the memory array is crucial in determining the overall capacity for storage of an SRAM chip. In general, larger memory arrays possess the potential to store a greater amount of data, hence augmenting the total storage capacity of the SRAM. Nevertheless, this advantage is accompanied by the drawback of increased chip surface area and potentially elevated power consumption.

In the presented Table I, each SRAM configuration is coupled with a specific memory array size, typically ranging from kilobits to megabits. Configurations with larger memory array capacities can accommodate more data, making them suitable for applications requiring extensive storage capacities. For instance, the 8T configuration stands out for its potential to deliver up to 256 Kb (kilobits) of memory, making it well-suited for applications demanding a considerable quantity of memory.

While larger memory arrays offer advantages in terms of storage capacity, they also come with some trade-offs [8]. The increased chip area necessary to handle larger memory arrays might contribute to greater production costs and potentially limit the scalability of the design. Additionally, larger memory arrays may require more power, reducing the overall energy efficiency of the SRAM chip.

Basically, choosing an SRAM configuration requires careful consideration of the application's requirements

and a thorough assessment of variables including power consumption, storage capacity, and area use in order to provide the best possible outcome.

E. Array Efficiency

Array efficiency estimates the proportion of the memory array that is successfully utilized for storing data, eliminating any overhead or redundant elements. Various elements, including circuit overhead, redundancy systems, and peripheral circuits, might influence the total array efficiency. A greater array efficiency rating indicates superior utilization of the memory array for storing relevant data, maximizing the effective storage capacity of the SRAM chip.

In the circumstances provided, the 5T architecture emerges as a standout performer in terms of array efficiency. This shows that the 5T configuration employs a bigger share of its memory array for storing data compared to other arrangements. By decreasing circuit overhead and optimizing peripheral circuits, the 5T architecture delivers a better level of efficiency in utilizing memory resources.

The increased array efficiency displayed by the 5T architecture suggests that it allows better exploitation of memory resources, potentially leading to enhanced storage capacity and improved overall performance in applications demanding efficient data storage. Therefore, while selecting an SRAM design, consideration of array efficiency alongside other performance parameters is vital for attaining optimal usage of memory resources and increasing the efficacy of the memory subsystem.

F. Read/Write Characteristics

The Table I offers a detailed summary of critical properties linked with the read and write operations of different SRAM architectures, including minimum operating voltages, operating frequencies, and energy consumption per bit. These characteristics play crucial roles in influencing the performance, power consumption, and reliability of SRAM chips under diverse operating circumstances.

Lower voltage needs for read/write operations often translate to reduced power consumption, a trend shown by the 4+2T and 7T designs in the Table I. By running successfully at lower voltages, these topologies indicate a capacity to cut energy usage, boosting overall power efficiency. This property is particularly helpful in and reduce manufacturing costs, ultimately advancing the scalability and viability of SRAM technologies. Furthermore, as the demand for memory-intensive applications grows, there is a need to explore alternative memory technologies and architectures that can complement or augment traditional SRAM designs. Thus, research directions in SRAM design going forward are wide-ranging and include improving existing configurations for new technologies and exploring novel battery-powered devices or energy-constrained contexts where power consumption is a vital factor.

On the other hand, the 8T design stands out for delivering the lowest read and write frequencies among the configurations given in the chart. Despite running at slower frequencies, the 8T design compensates by requiring the least energy per bit during read and write operations. This means that while it may not reach the fastest data transmission speeds, it excels in terms of energy economy, making it an interesting choice for applications emphasizing power optimization.

Overall, the characteristics listed in the Table I provide insightful viewpoints on how different SRAM designs strike a compromise between power consumption, energy efficiency, and performance. After carefully analyzing these factors, designers are better equipped to choose an SRAM configuration that best fits the unique requirements and limitations of their application.

VI. Conclusion

The selection of an appropriate SRAM configuration is a multifaceted decision that hinges on the specific requirements of the application at hand. Designers must carefully balance various factors such as area efficiency, power consumption, performance, and array size to meet the desired objectives effectively. However, the landscape of SRAM design continues to evolve, presenting opportunities for future research and development endeavors.

One avenue for future exploration involves optimizing SRAM configurations to align with emerging technologies. As new fabrication processes and materials emerge, there is potential to enhance the performance and efficiency of SRAM cells through innovative design approaches. Additionally, exploring novel transistor architectures, such as non-traditional gate structures or advanced materials, could lead to breakthroughs in SRAM design, unlocking new levels of performance and energy efficiency.

Addressing challenges related to manufacturing and integration represents another crucial area for future research. As technology nodes continue to shrink, manufacturers face increasingly complex manufacturing processes and integration challenges. Future research efforts may focus on developing techniques to improve yield rates, enhance reliability,

transistor architectures while overcoming challenges related to manufacturing. Scholars can significantly contribute to the development of memory solutions that are not only more dependable and efficient but also flexible enough to meet the ever-changing demands of modern computing systems by pushing the limits of SRAM architecture.

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