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Comparative Study Of Different Hysteresis Modulation Methods Of Multilevel Inverters

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Abstract

The hysteresis modulation for power electronic converters is attractive in many different applications because of its unmatched dynamic response and wide command-tracking bandwidth. Its application and benefits for two-level converters are well understood, but the extension of this strategy to multilevel converters is still under development. This paper summarizes and reviews the various hysteresis modulation approaches available in the literature for multilevel converters. The pros and cons of various techniques are described and compared for tracking the reference signal in order to attain an adequate switching optimization, excellent dynamic responses and high accuracy in steady-state operation. By using the recently developed multilevel hysteresis modulation approaches, the advantages of using several accessible dc potentials in a multilevel inverter have been fully exploited. All of these hysteresis modulation approaches are tested for tracking a current reference when applied to a five-level inverter. The relevant simulation and experimental results are also presented. This study will provide a useful framework and point of reference for the future development of hysteresis modulation for multilevel converters.

***Key words*—Hysteresis modulation, multiband (MB), multioffsetband (MOB), multilevel converter, time-based (TB).**

1. Introduction

The hysteresis modulation for power electronic converters are preferred for applications, where performance requirements are more demanding such as to achieve good dynamic response, unconditional stability, and wide command-tracking bandwidth. In this approach, the controlled system variable is compared against hysteresis band(s) to create the switching commands for the converter. This control has been widely used to control the conventional two-level converter, showing its robustness and simplicity in a lot of applications. A brief description of the standard two-level hysteresis control for output current regulation is presented in the following. The objective of standard two-level hysteresis current control is to switch the converter transistors in such a manner that the converter load current tracks a reference within a specified hysteresis band. Consider a single-phase half-bridge inverter, as shown in Fig.1.(a) for two-level hysteresis current control. In Fig.1(a) two dc sources of magnitudes *V*dc/2 are considered at the dc link of inverter and their common point (*n*, neutral point) is grounded. The net controllable output voltage of the inverter is *uV*dc/2, where *u* is defined as the control input and represents the switching logic of inverter. It assumes the values +1 and −1 for the two-level inverter of Fig.1(a). The inverter output voltage *v*an can be represented as follows:

$$v_{\mathrm{an}} = \frac{uV_{\mathrm{dc}}}{2} = Ri_a + L\frac{di_a}{dt} + v_{\mathrm{back}} \quad \text{.....(1)}$$

where i_a is the load current, V_{back} is the back EMF voltage, and *L* and *R* are the load inductance and resistance, respectively [see Fig.1(a)]. As V_{back} increases or as larger reference current slopes are required, larger average values of *v*an need to be used. Since the voltage across the load resistance is often small, this value can often be neglected. Introducing a term d_{iref}/dt, where *i*ref is the current reference to be tracked, (1.1) becomes as follow

$$\frac{d(i_a - i_{\mathrm{ref}})}{dt} \approx \frac{uV_{\mathrm{dc}}/2 - v_{\mathrm{back}}}{L} - \frac{di_{\mathrm{ref}}}{dt}. \quad \text{.....(2)}$$

It is evident from (2) that the current error (*ce* = *ia* − *i*ref) can be reduced by increasing or decreasing *v*an, depending on the polarity of *ce*.Fig.1(b) represents the implementation logic for this correct voltage-level selection for a two-level inverter using hysteresis control. It can be seen that as the measured current (*ia*) becomes greater than its reference (*i*ref) by the hysteresis band "*h*," the inverter output voltage (*uV*dc/2) is switched to its lowest level (−*V*dc/2, *u* = −1) in order to decrease the current. Likewise, when *ia* becomes less than *i*ref by "*h*", *uV*dc/2 is switched to its highest level (*V*dc/2, *u* = +1) in order to increase the current. For the inverter of Fig.1.1(a),*u* assumes the value +1 for the switching logic *S*1 = 1, *S*2 = 0 and −1 for *S*1 = 0 and *S*2 = 1. A three-phase system can also be simply implemented using three independent single-phase hysteresis current regulators. Based on the two-level hysteresis control logic described earlier, the control input *u* can be defined as follows:

if (*ce* (*t*) ≥ +*h*) , then *u*(*t*) = −1

else if ($ce\ (t) \leq -h$) , then $u(t) = +1$.

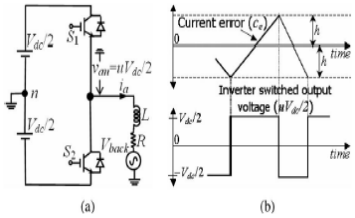


Fig.1. (a) Two-level half-bridge inverter.(b) Two-level hysteresis control

However, this new converter voltage level may not be adequate to return *uc* to the specified limits. When this happens, the converter should switch to the next higher (or lower as appropriate) voltage level, and the process should cease only when the correct voltage level is selected that reverses the direction of *uc* . To exemplify it further, one of the standard multilevel inverter topologies, the single-phaseleg five-level configurations of which are shown in Fig.2 can be considered. For a five-level inverter, *v*an in (1) may be defined as *v*an = *n*Vdc, where *n* = 1/2, 1/4, 0, −1/4, and −1/2, as a five-level inverter may select between voltage levels *V*dc/2, *V*dc/4, 0, −*V*dc/4, and −*V*dc/2 for the net dc-link voltage of *V*dc. Then, in a similar manner as described earlier, *ce* can be kept limited to a specified band by selecting a higher or lower voltage level than its present output depending on the polarity of *ce*.

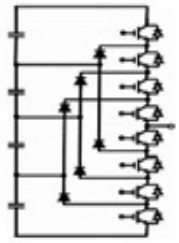


Fig.2.Five-level diode-clamped inverter.

2.MB Hysteresis Modulation

The MB hysteresis modulation scheme for the multilevel converters uses symmetrical hysteresis bands to control the switching so that the inner band causes switching between adjacent levels, while the outer band causes an additional switching level change whenever necessary. The process, first proposed in and later used is shown in Fig.3.(a) in the form of current regulation. Whenever the current error Fig.3.(a) crosses the inner boundary *B*, the inverter output is decreased or increased by one level (depending on which hysteresis boundary has just been crossed). Generally, this voltage change Fig.3.(b) will cause the current error to reverse its direction without reaching the next outer band. However, if the error does not reverse, it will continue through the boundary of *B* to the next outer boundary (placed atΔB out of*B*). At this point, next higher or lower level voltage will be switched. This process continues as discussed earlier until the current error direction reverses.

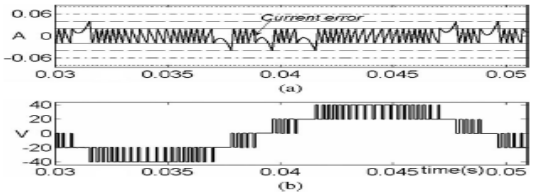


Fig.3..MB five-level hysteresis modulation.
(a) Current error and hysteresis band plots.
(b) Inverter output voltage.

It is important to note that if the voltage level applied at a boundary crossing of the current error Fig.3.(a) is insufficient to force the error back, no next voltage level is applied as the error againFig.3.(b) crosses this boundary next time after the previous voltage level change with the same slope. The error in that case is allowed to go until the next voltage level change at next higher or lower boundary crossing of the error to force it back as is evident from Fig.3.(a).

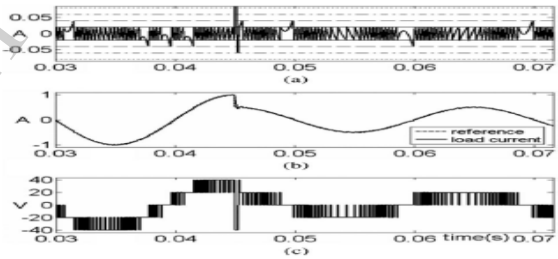


Fig.4. Transient performance of MB scheme.
(a) Current error and hysteresis band plots.
(b) Reference and measured load current.
(c) Inverter output voltage.

3.Experimental Setup

An experimental setup is used to test the MHM schemes discussed in this paper. A prototype of a single-phase five-level IGBT-based diode-clamped inverter is built in the laboratory. The overall structure of the experimental setup is shown in Fig.5. The main power circuits consist of a single-phase five-level voltage source diode clamped inverter, load, and dc-link circuit. The inverter dc bus is supported by a separately controllable dc supply obtained from a single-phase transformer and diode rectifier circuit. The dc link voltage and load parameters of the inverter are kept same as considered earlier in the simulation studies, i.e., *V*dc = 80V and *R* = 35 Ω, *L* = 30 mH, respectively. HV2–HV5 denotes the Hall effect voltage transducers for sensing the dc-link capacitor voltages and HC1 represents the Hall effect current transducer

sensing the inverter load current (*ia*). Each semiconductor switch shown in Fig.4.3 explain as follows, it consists of an IGBT with an anti parallel diode. The IGBT modules used is Mitsubishi CM75DY-24 H. This is a 1200 V/75 A IGBT with two IGBTs/ diodes in each module. For simplicity, the same IGBT modules are also used as clamping diodes with a shorted gate in the inverter, as shown in Fig.4.3 The presence of back EMF would serve to create more variation in switching frequency, but without affecting the nature of the current error trajectory. Therefore, for simplicity, back EMF voltage source has not been used. In the experimental setup, a chopper circuit for the dc capacitor voltages equalization has also been used, as shown in Fig.5. Its working principles and operational features can be referred from .Without any dedicated control or additional hardware, the dc-link capacitor voltages tend to unbalance under most of the operating conditions in a diode-clamped inverter . This chopper circuit of Fig.5 keeps the dc-link capacitor voltages balanced so that the inverter is able to generate five different and correct voltage levels.

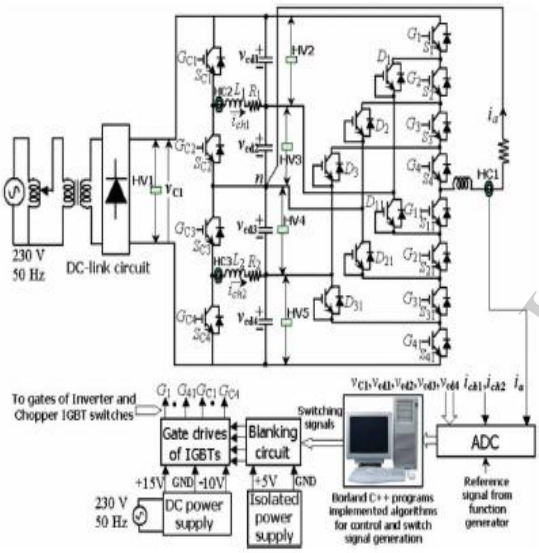


Fig.5. Overall structure of the experimental setup

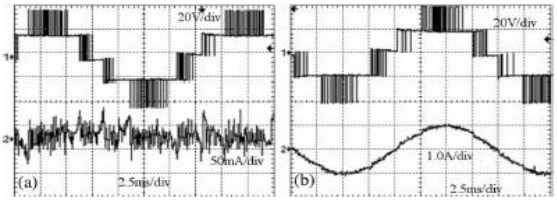


Fig.6.Experimental results showing the MB hysteresis modulation performance
(a) Inverter output voltage and current error.
(b) Inverter output voltage and controlled load current.

4.MOB Hysteresis Modulation

As opposed to the MB scheme, which uses symmetrically placed hysteresis bands for current error regulation, the MOB scheme uses the bands placed with an offset around the zero current error line. The advantage of using the offsets is that different bands can be easily implemented. Also, the corresponding logic can also be easily programmed /implemented in a way that if the voltage appearing at the boundary of a band is insufficient to force the error back, it is allowed to move to the other band. As opposed to the previously presented scheme, fixed voltage levels are applied in MOB scheme as the current error crosses a boundary of the band with a certain slope. In this section, first the conventional MOB scheme is presented, and then, its modified version is presented, which offers improved performances.

5.Conventional MOB Hysteresis Modulation

A MOB scheme was proposed in previous section on the basis of a three-level inverter. In this scheme, the current can be controlled using $n-1$ offset bands for an n-level inverter. Fixed voltage levels are switched at each of the offset boundaries when the current error crosses the boundary of an offset band in a direction, away from the zero error line. A possible two-offset band arrangement ($B1$, $B2$) for controlling a three-level inverters shown in Fig.7. It is shown in the figure that as the error (Ce) touches the corresponding boundaries of $B1$ and $B2$, fixed output voltage levels are switched. The switching takes place when sign of the error and its slope at the boundary of a band are same, and the previous switching had not taken place at the same boundary of the same band.

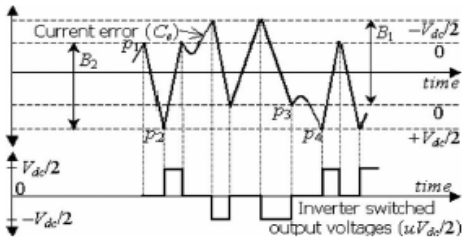


Fig.7.Three-level MOB hysteresis modulation

To exemplify it, let us consider a five-level multi offset hysteresis current regulation with Fig.8 showing a possible current error trajectory along with the offset-band arrangements and corresponding switched output voltage levels. By following the scheme of , it requires four bands ($B1-B4$) and as the current error touches the corresponding boundaries of $B1-B4$, fixed output voltage levels are switched. It can be followed that 0 V is switched at the lower limits

of$B1$,$B3$ and upper limits of$B2$,$B4$,$-V$dc/4 at the upper limit of $B1$,+Vdc/4 at the lower limit of $B2$, $-V$dc/2 at the upper limit of $B3$ and +Vdc/2 at the lower limit of $B4$.

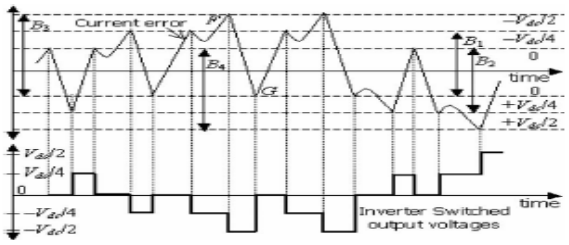


Fig.8. Five-level MOB hysteresis modulation.

The limitation, when using this scheme for a higher level inverter can be seen by looking at the current error path from F to G. It is evident that a voltage-level transition from $-V$dc/2 to 0 V occurs at G, thereby, skipping the level $-V$dc/4. This results in inverter output voltage with large steps and large voltage stress across the devices at the switching instants Fig.9.

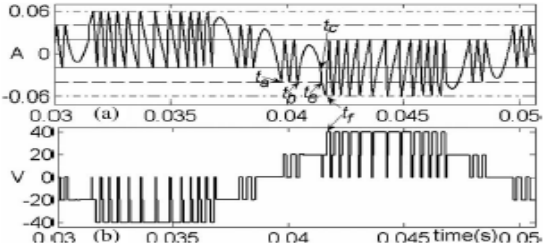


Fig.9..MOB five-level hysteresis current control with fixed voltage applied at the band crossings of the current error. (a) Current error trajectory along with the allotted bands.(b) Inverter switched output voltage.

It is evident that in this process, the intermediate level +Vdc/4 is skipped as the current error travels from *tf* to the upper boundary of $B2$. It should be noted that since the current error remains in the allotted bands, the controlled current follows its reference. It is the voltage waveform, which is degraded. However, as is evident from Fig.4.7,the error is bounded within a smaller band ($B1$ or $B2$) in the region when switching the voltage levels 0 and Vdc/4, while due to the control actions of this scheme, the error is bounded within a larger band ($B3$ or $B4$) in the region when it is required to output one of the two extreme voltage levels Vdc/2. This results in variable-tracking performance in a single cycle of the current waveform itself.

6.Modified MOB Hysteresis Modulation

To overcome the drawbacks of the multilevel control of MOB, MMOB hysteresis control is presented. The band placement and functioning of MMOB scheme for a five-level inverter is shown in Fig.10.

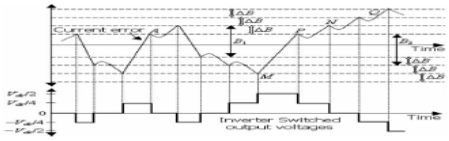


Fig.10..MMOB five-level hysteresis modulation

In this scheme, the current error is required to be bounded mainly between the bands $B1$ and $B2$, which are displaced by a small offset ΔB. Further, two additional offsets of the same width ΔB are placed out of $B1$ and$B2$ to provide a reliable and robust control. In general, a total number of $n-2$ offsets are required for an n-level inverter in both the positive- and negative-current-error regions. It differs from the MOB method in the decision logic of output voltage levels at the crossing points of current error and corresponding boundaries of the hysteresis bands and also in the total number of bands required. In the MMOB approach, the applied output voltage at the band crossing points of current error is not fixed, but depends on the previous voltage level, i.e., just before the crossing point. .

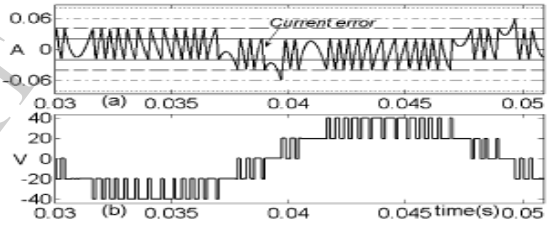


Fig.11.MMOB five-level hysteresis modulations.
(a) Current error and the hysteresis band plots.
(b) Inverter output voltage.

Fig.11 shows the results, the switching always occurs between adjacent levels and no voltage level is skipped. Also, as opposed to MOB scheme, the current Fig.4.9(a) tracking performance remains uniform throughout a complete load current cycle in MMOB scheme, as the current error is mostly bounded within the hysteresis bands of same width. It should be noted that the controller acts as desired when switching between +Vdc/4, 0, and $-V$dc/4 and degrades when higher voltage levels (Vdc/2) are needed to be switched. This indicates that fixed voltage-level Fig.11(b) switching as in works fine for the three-level inverter and needs modification for higher level inverters.

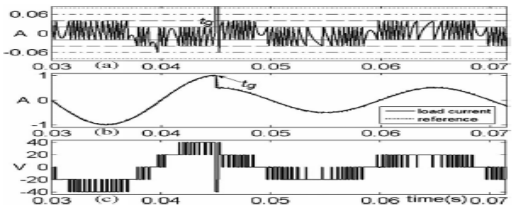


Fig.12.Transient performance of MMOB modulation. (a) Current error and hysteresis band plots. (b) Reference and measured current.(c) Inverter output voltage

Transient performance of MMOB modulation, Fig.12.shows the simulation results, obtained under the same transient condition, as considered in the previous sections. the current Fig.12(a) tracking performance remains uniform throughout a complete load current cycle in MMOB scheme, as the current error is mostly bounded within the hysteresis bands of same width.The reference and measured current are shown in Fig.12.(b),

7. TB Hysteresis Modulation

As discussed earlier, although the MOB schemes are easy to implement , it requires offset compensation signals to be added to the controlled system variable, since the bands are not symmetric about zero. The MB scheme, presented does not suffer from this steady-state-tracking error problem, but may still not have evenly symmetric current error waveform, especially for non sinusoidal current references. In the following, a TB MHM is first described, which works on the principle of controlling the system variable within a single band so that any type of current offset can be avoided. Then, a modified TB approach for MHM is discussed, which shows much better performances in terms of tracking as well as can be used with a limit on the maximum allowable switching frequency.

8.TB Multilevel Hysteresis Modulation

A TB multilevel hysteresis control scheme was proposed is to use only one hysteresis band to detect an out-of bounds current error. Digital logic is used to select the "correct" voltage level in response. Upon detecting the error exceeding the upper (or lower) hysteresis limit, the inverter output is switched down (or up) one voltage level so as to return the error back to zero, as earlier. But if the new inverter switched state is inadequate to reverse the error back to zero, the output is switched further down (or up) until the current-error direction reverses. A possible current error trajectory and inverter switched output for a five-level inverter are shown in Fig.13.

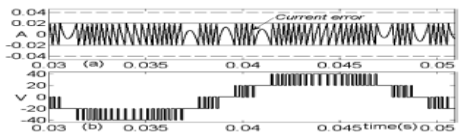


Fig.13.TB five-level hysteresis modulation
(a) Current error and the hysteresis band plots.
(b) Inverter output voltage.

9.Modified TB Hysteresis Modulation

To counter the limitations of the aforementioned TB scheme, an efficient method is modified TB multilevel hysteresis control scheme. This approach requires $(n-2)$ outer bands at ΔB from their inner ones for an n-level inverter. Further, the current error slope-detection-based control is replaced by the algorithm of detection of only sign of the current error slope. The use of extra bands in the modified scheme implies that, for example, if the current error crosses B with a certain voltage switched at the boundary of B, the next voltage level will not be switched until the error touches the outer band at ΔB from B. By doing so, the situation like that discussed in the earlier paragraph can be clearly avoided for a sufficient width of ΔB. A total number of $(n-1)$ bands required for an n-level inverter in this scheme can be justified by following the current error trajectory in control details of modified TB scheme and the discussions presented in the earlier presented schemes. It is also clear that it can efficiently work under varying load conditions as well. Based on the earlier discussion, the switching decisions under this scheme can be defined with respect to TB scheme for an n-level inverter as follows:

$$\text{if } \left\{C_e \geq 0 \text{ and } \frac{dC_e}{dt} > 0\right\}, \text{then } u(t_k) = u(t_{k-1}) + \frac{1}{n-1}$$

$$\text{else if } \left\{C_e < 0 \text{ and } \frac{dC_e}{dt} < 0\right\}, \text{then } u(t_k) = u(t_{k-1}) - \frac{1}{n-1}.$$

$u(tk)$ is the current value of the switching decision, while $u(tk-1)$ is its immediate past value. This can be justified from Fig.14(a) in which, $tk-1$, tk , etc., shown on the horizontal axis are the time instants at which Ce crosses the earlier defined boundaries of the bands. It can be seen that depending on the sign of Ce and dCe/dt, the output voltage level is either increased or decreased by Vdc/4, at the crossing points Fig.14(b). Note that, the inverter holds its output voltage level until tk , which it attained at $tk-1$.

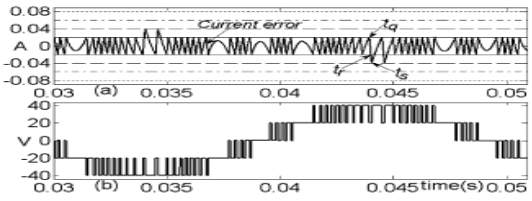


Fig.14.Modified TB five-level hysteresis current control. (a) Current error and hysteresis band plots. (b) Inverter switched output voltage.

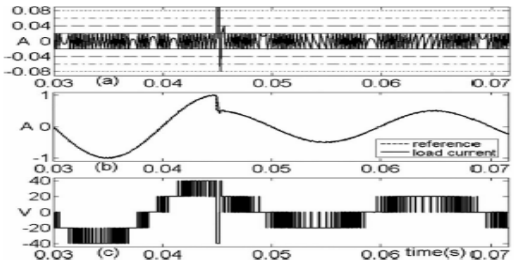


Fig.15.Transient performance of modified TB scheme. (a) Current error and the hysteresis band plots.(b) Reference and measured load current. (c) Inverter output voltage.

10. MATLAB Design and Results

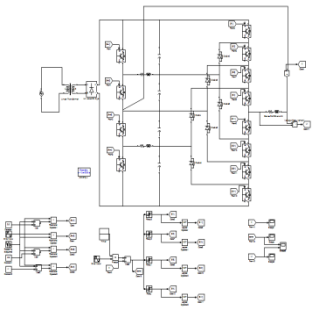


Fig.15.Simulink model of MOB Modulation

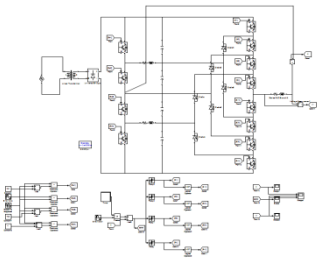


Fig.16.Simulink model of MMOB Modulation

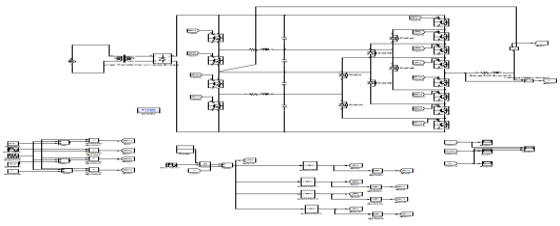


Fig.17.Simulink model of TB Modulation

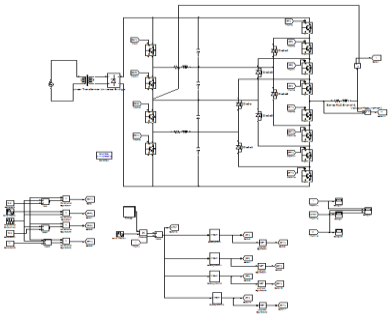
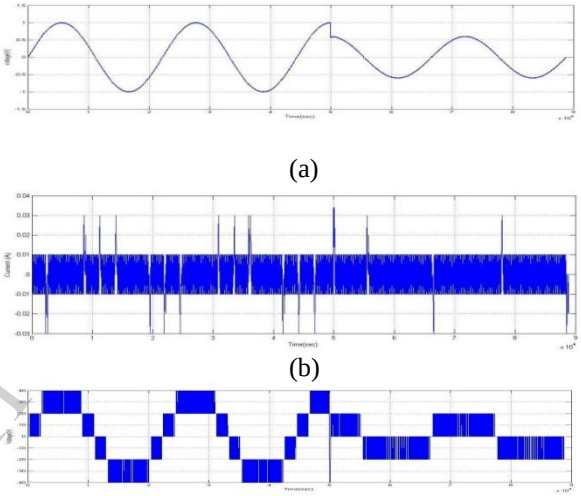


Fig.18.Simulink model of MTB Modulation

11.Simulation results

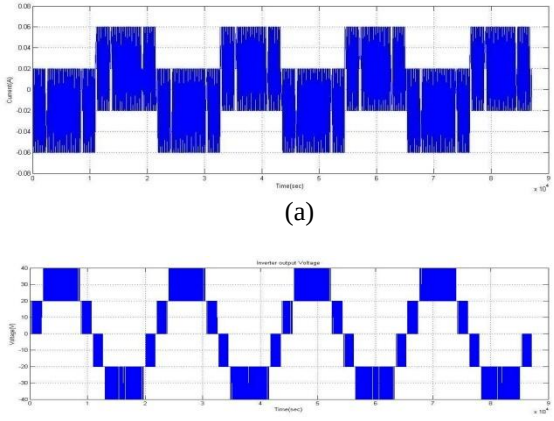


(a)

(b)

(c)

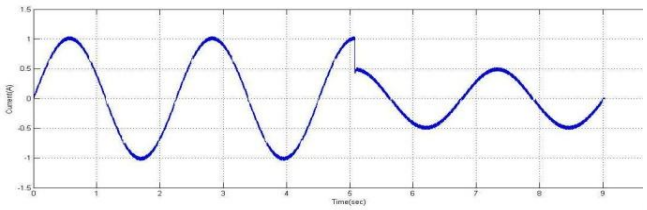
Fig.19.Transient performance of MB scheme.
(a) Current error and hysteresis band plots.
(b) Reference and measured load current.
(c) Inverter output voltage



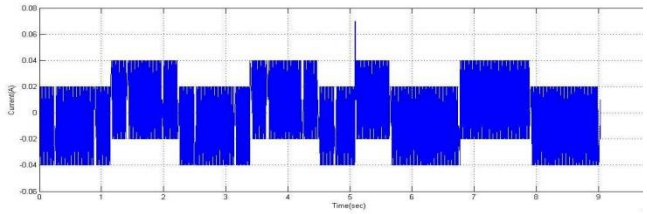
(a)

(b)

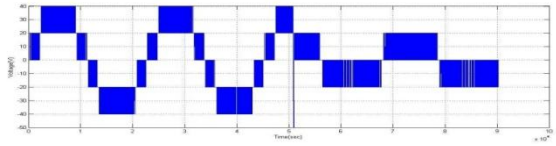
Fig.20.MOB five-level hysteresis current control with fixed voltage applied at the band crossings of the current error.
(a) Current error trajectory along with the allotted bands.
(b) Inverter switched output voltage



(a)

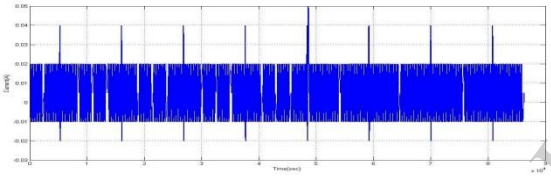


(b)

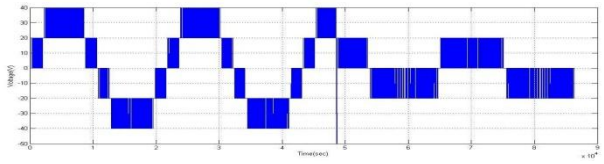


(c)

Fig.21.Transient performance of MMOB scheme.
(a) Current error and hysteresis band plots.
(b) Reference and measured load current.
(c) Inverter output voltage

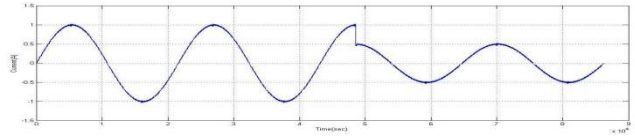


(a)

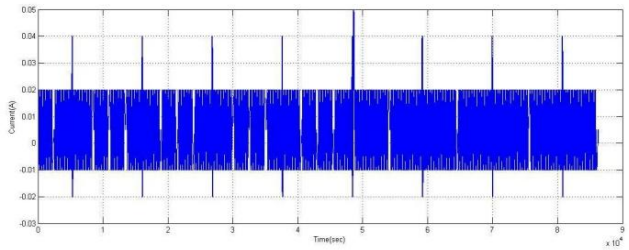


(b)

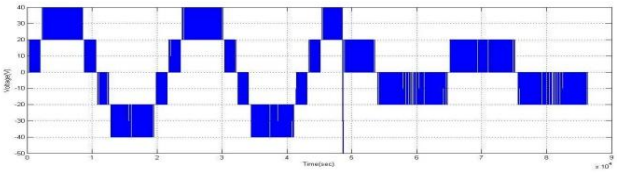
Fig.21.TB five level hysteresis modulation
(a) Current error .(b) Inverter output voltage



(a)



(b)



(c)

Fig.22.Modified TB five level hysteresis modulation.(a)Current error .(b)Hysteresis band plots
(c)Inverter switched output voltage

Conclusion

In this paper summarizes and reviews the various hysteresis modulation techniques available in the literature for the multilevel converters. This includes, in general, the MB, MOB, and TB hysteresis modulation techniques. To generalize the existing MHM techniques for higher level inverters, their modified versions have been also discussed. The basic principle of operation and logical sequence of the design choices has been described for each of these schemes. The advantages of using various accessible dc voltage levels have been fully exploited by using these schemes. The various schemes considered in this paper have been further investigated using simulation and experimental studies for a five-level inverter system. However, these strategies can easily be extended to any multilevel inverter structure, even in the case of *n*-level voltage waveforms and three-phase systems. This paper also presents a comparative analysis of the various MHM schemes. Among these schemes, the modified TB scheme offers a number of advantages in terms of better tracking performance, extra control over maximum allowable switching frequency, etc. It can be expected that with further investigation of the MHM methods and the development of modern technology, the hysteresis modulation will gain more popularity for controlling the multilevel converters in different applications.

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