Comparative study of Synchronous High Resolution DPWM techniques on FPGA

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Abstract: **-Digital Pulse Width Modulation (DPWM) technique has a great influence on power controlled application due to its better stability, controllability and ability to work in high frequencies. These techniques are widely used in power converters and recent developments in semiconductor field have pushed the switching frequency limits of power devices. In order to meet the frequency requirement it needs an efficient Pulse Width Modulating (PWM) Technique. In this paper we have compare two Synchronous High Resolution DPWM techniques on FPGA based on conventional DPWM counter based design.**

Keywords—DPWM, high resolution, power converters

I. INTRODUCTION

Energy harvesting is now one of the leading research fields in the modern world in order to deal with the need of the day by day rising of energy demand with more eco-friendly and natural way. Now a days we mainly depend on renewable energy harvesting techniques like sun, wind etc. as a solution to meet this problem. But the main drawbacks of these techniques are that the output cannot be predicted. So in-order to deal with the variations in the output we depend on power converters[6]-[10]to get the desired output which we can work on.

The recent development in semiconductor like GaS and SiC[11] power devices as pushed the limits of operating frequency further and to handle the switching frequency we need high resolution Pulse Width modulators[1] to drive it. Traditional designs of DPWM techniques was basically designed by using counters and comparators, which is mainly used to generate the gating signals for the depending on the thresholds. In these type of designs the main factor is number of bits(η_{DPWM}) used to generate a PWM signal and the counter clock period which determines the minimum on-time step.

$$\eta_{DPWM} = log_2\left(\frac{f_{clk}}{f_{sw}}\right) \qquad (1)$$

- f_{SW}:- DPWMfrequency
- f_{CLK}:-counter clock frequency

Nowadays, the effort of evolution in the field of power converter designs with higher switching frequencies is increasing which ultimately aims to reduce the size of inductors and capacitors. The another need of high resolution is that in the case of digital implementation, the number of bits η_{DPWM}should be higher than the A/D converter resolution in order to avoid the limit cycling[3]-[5]. As a result, here will be unfeasibly of high clock frequency which can result in theincrease of the complexity and therefore increasing the cost of final implementation.

Another advantage of PWM signal is that it gives control over the signal both logically in digital applications and over voltage in power control applications like motor control. The control over voltage can be attained by changing the duty cycle of the PWM signal as shown in Fig 2.
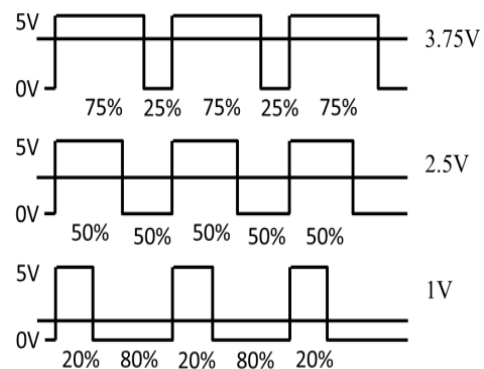

Fig.1. waveform showing control over voltage

$$voltage = 5v * \frac{duty\ cycle}{100} \qquad (2)$$

5v is the peak voltage of the given PWM signal

FPGA's are one of the efficient technology or solution which has been provided by the engineers to easily test and see the outcome at each scenario by implementing each design in it and to come up with an efficient solution. Most of the new FPGA's have on board processors to handle computing more easily. The simplicity and features of FPGA has bought it a long way and FPAA and FPAADD has proven promising development in this field. FPGA can be used in even harsh environment and the ease of upgrading has made it more efficient and has a solution for our needs. It can also work with high frequency and power control application which makes it an ideal solution in power electronic systems. It also reduces the cost and size of the controlling section in a design which attracts design

engineers to choose FPGA's in many power electronic devices.

In this paper we are comparing two designs of high resolution DPWM technique based on the conventional design using counters and comparators[2]. The first design is based on Digital clock manager and multiplexers as add-on to the conventional design and it is designed on Spartan series FPGA and the second design uses Mixed-Mode Clock Manager(MMCM) and IODELAY1 block in virtex 6 series.

II. HIGH-RESOLUTION SYNCHORONOUS DPWM ARCHITECTURES USING DCM BLOCK
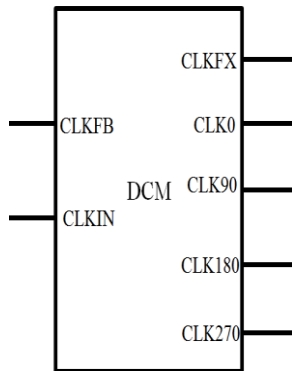
A. DCM BLOCK

Fig: 2 DCM block in Spartan series

Digital clock managers are the block which is present in Spartan series FPGA's to handle the clock signals. DCM blocks reduce the jittering caused by the clock signals in the design by using a feedback signal to determine the jitter in the clock signals. It also can generate different clock signals with reference to the input clock signals by its phase shifting and frequency synthesising features.

The fine phase shifting can be fixed (specified at design time and set during the FPGA configuration process) or variable. It is set by means of the DCM attributePHASE_SHIFT [12], an integer in the range [-255, +255][13]. Fig. 2 shows the fine phase shift effects in the fixed mode of operation. A phase-shifted output with a resolution of (1/256)th of the input clock period can be obtained.
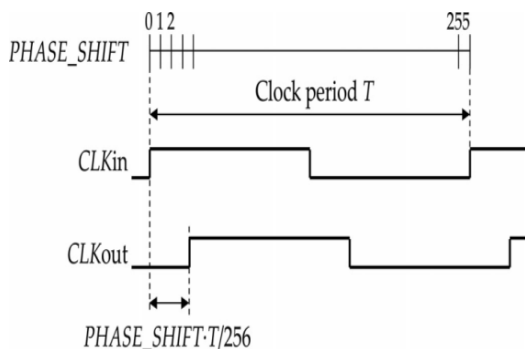
Fig:3 waveform showing phase shifting effect

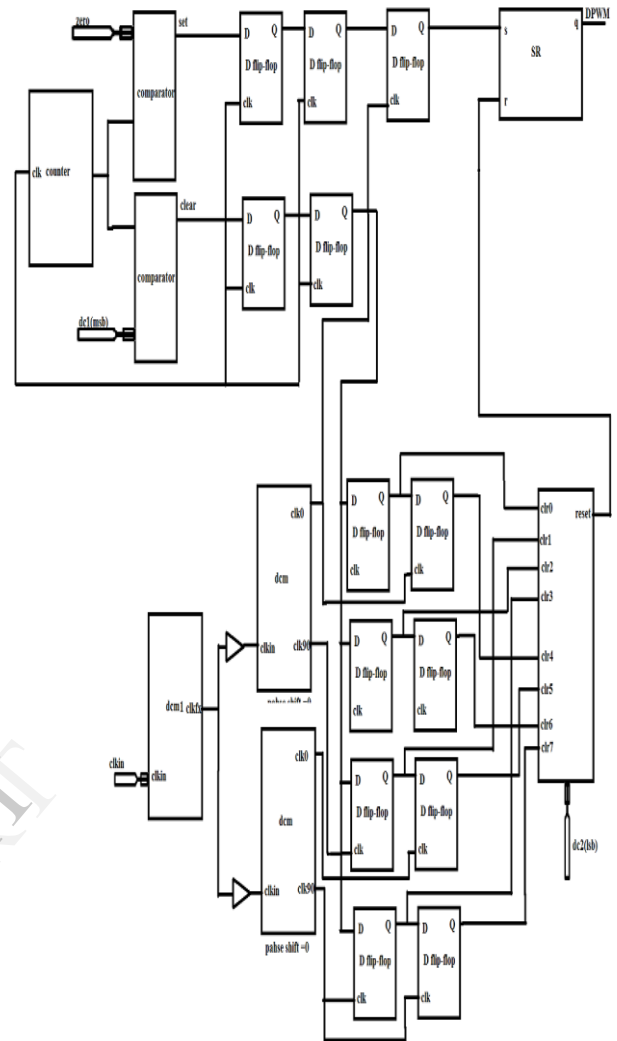### B. High resolution DCM based DPWM design

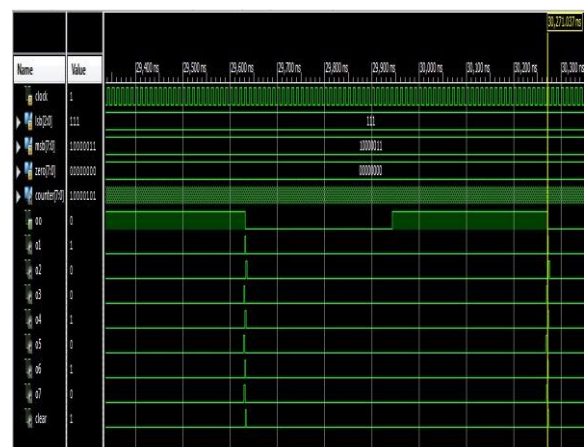Fig:4 high resolution DPWM architecture based on DCM module

Fig:5 output waveform of DCM based DPWM technique

In this design the clock signal is phase shifted and synthesized with the help of DCM modules to generate clock signals with different frequency and phase shift needed for the PWM signal generation. The input bits are divided into msb(dc1) and lsb(dc2). When the counter gets

the clock signal its startscounting and when the output of the counter matches the input of the 1st comparator (zeros) a set signal is given to the SR latch. And when the output of the counter matches with the input of the 2nd comparator (dc1)a clear signal is activated and this output signal is given to the D flip-flops and depending on the multiplexer input(dc2) the output of a D flip-flop is send as a reset. Since the phase shift and frequency of the clock signals given for the flip-flops are different we will get a proper reset signal depending on the input given to the multiplexer.The design is simulated on Spartan XCS400-4tq144 series.

TABLE 1: SYNTHESIS REPORT OF DCM BASED DPWM

DEVICE UTILIZATION SUMMARY(ESTIMATED VALUES)			
LOGIC UTILIZATION	USED	AVAILABLE	UTILIZATION
NUMBER OF SLICES	23	3584	0%
NUMBER OF SLICES FLIP FLOPS	19	7168	0%
NUMBER OF 4 INPUT LUTS	41	7168	0%
NUMBER OF BONDED IOBS	21	97	21%
NUMBER OF GCLKS	10	8	125%
NUMBER OF DCMS	3	4	75%

III.   IODELAYE1 HIGH RESOLUTION DPWM
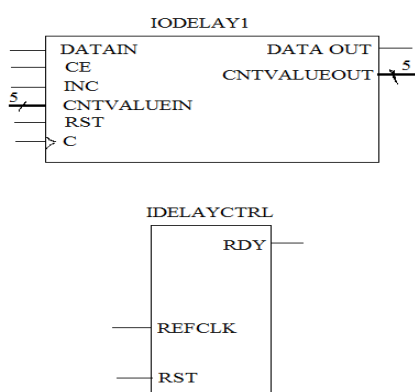
A. *IODELAY1 block*

Fig.6. pin out description of IODELAY1 and IDELAYCTRL

In the second approach we make use of the I/O delay block (IODELAYE1) which is present in Virtex-6[14] series FPGAs or as IODELAY2 present in Virtex-7 FPGAs. The IODELAYE1 block provides a certain delay for the input signals according to the parameters and mode we use the block thus by allowing us to generate

the signals which has been delayed by a certain number of tap delays with respect to the input. The factor which calculate the resolution is the tap resolution and for IODELAYE1 the tap resolution is given by,

$$t_{tap} = 1/(32 \cdot 2 \cdot f_{CK\_REF}) \qquad (3)$$

byproviding a fine delay-time t_d adjustment. The range of the IODELAY1 Block is determined by the reference clock frequency which is the main attribute in this design. The range of clock frequency range is from 200 ± 10. The IODELAY1 block can run on different modes depending on the inputie, the attributes which we set.In increment/decrement mode (CE), increment/decrement delay (INC), and reset (RST), are the attributes which determines the mode of operation of the IODELAY1 to control the desiring delay as needed. One of the advantages of the block is that it uses a clock signal C which makes the design synchronous which ultimately helps us to determine the delay and predict the output precisely. The IDELAYCTRL block should be instantiated with the IODELAY1 block since IDELAYCTRL is responsible for the continuous calibration of the delay elements which helps to reduce the influence of process, voltage, and temperature on the output signal with the help of supplied reference clock frequency (REFCLK). Fig. 6 shows the pin outdescription of the IODELAYE1 and IDELAYCTRL blocks in vertex 6 series. The different modes of operation of IODEALY1 when operating in the unidirectional input delay configuration, depending on the mechanism used to select the number of delay taps.

1) Fixed: The delay is fixed in this mode at the time of design and the delay cannot be changes in between an operation.

2) Variable: In this mode the delay factor depends on the input control signals CE and INC. Increment/decrement signal (CE) determines the delay by incrementing or decrementing the number of delay taps depending on the INC signal is activated or not. The RESET input when activated resets the delay block to a predefined delay value

3) Loadable variable: This mode is similar to the variable mode operation except the delay factor is determined by a 5 bit input value provided to the CNTVALUEIN in port. The delay time is, therefore, calculated as $t_d = t_{tap}$. Similar to the variable operation the reset signal is activated to reset the delay value ie, the 5 bit data given to CNTVALUEIN. The delay value when updated can be read from CNTVALUEOUT port.

B. *DPWM architecture using IODELAY1*

Fig. 7 shows the proposed implementation for an m+1-bit HRPWM using the IODELAY1 block. The

design comprises of a counter and comparators as thr traditional DPWM technique. Similar to the DCM DPWM technique this design uses MMCM block to handle the clock signals of this design. The difference of this design is that it replaces multiplexers from the traditional designs and uses IODELAYE1 block for increasing the resolution and to make the implementation easier. Signals SETD and CLRD are generated comparing the counter output with zeros for SETD and the most significant bits (dc(m:5) in the figure) for CLR. The CLR signal then is given to the IODALAY1 block for setting up the reset signal for the SR latch.
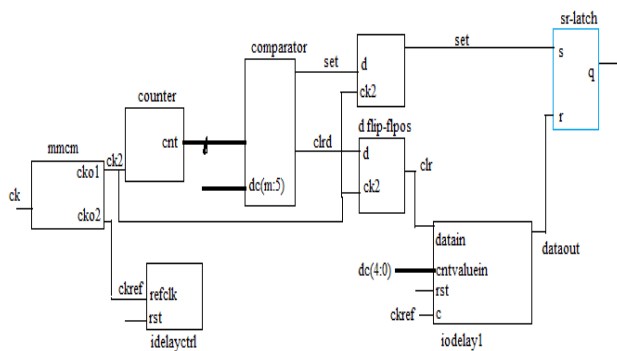

Fig.7.DPWM design using IODELAY1

In this design we use the IODELAY1 block in variable mode so that we can use the CNTVALUEIN port to set up the delay using 5 bit input data. The CNTVALUEIN sets up the delay using the 5 bit data and is delay factor can be updated using the reset signal (RST). Since the design is synchronous it provides more precision in providing and predicting the output. The clock signal provided in the input port C. the maximum delay which can be provided by the IODELAY1 block is 32- tap delay. The same delay factor demand the counter clock frequency to be the double of the IODELAY1 clock frequency. This demand is met by MMCM which does the same function as DCM block in the first design.

As mentioned above when ewe use IODELAY1 block we have use IDELAYCTRL block also with it whose main function is to auto calibrate the tap delay efficiently.MMCM is responsible for providing different output clock frequency and this is done by using the attributes like M, D, and O since

$$f_{CKO} = M/(D \cdot O) \qquad (4)$$

The basic operation of the proposed IODELAYE1-based HRPWM architecture with dc ="10110100." The CLRD signal is activated when dc(7:5) =CNT(7:5) = "101" = 4. The resulting pulse is captured in the next clock cycle by D flip-flop, which generates the input signal for the IODELAYE1 block to the input DATAIN. The IODELAYE1 block then will generate the RESET

signal by delaying the CLR signal according to the CNTVALUEIN inputwhich is the tap cyclesdc(4:0) = "10100" = 20. This signal clears the SR latch to generate the desired PWM signal.
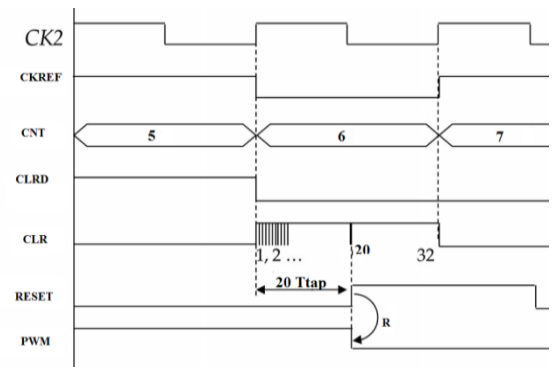

Fig.8. IODELAY1 operation for 10110100

The proposed IODELAYE1-based High Resolution Pulse Width Modulation architecture has been simulated for Xilinx Virtex-6 XC6VCX75T- FF484. The clock frequency used as input clock is 200-MHz and for counter frequency 400MHZ. The REF_CK clock frequency for the IODELAYE1 block has been set to 200 MHz, achieving a resolution

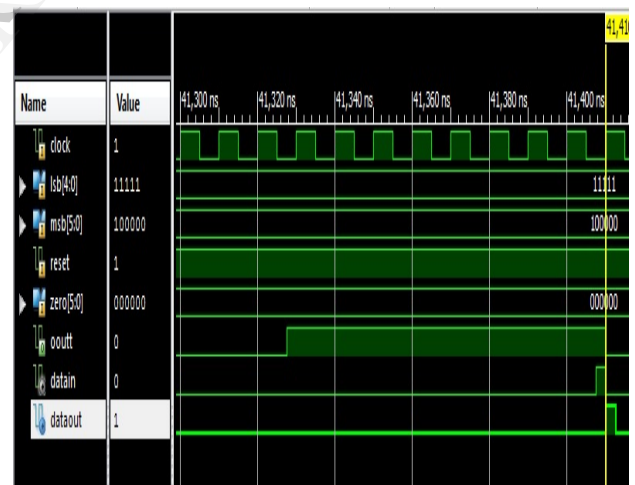$$t_{tap} = \Delta ton = (1/ (32 \cdot 2 \cdot f_{CKREF})) = 78 \text{ ps.}$$

Fig: 9.Output waveform of IODELAYE1 based design for 10000001111

TABLE 2: SYNTHESIS REPORT OF DCM BASED DPWM

DEVICE UTILIZATION SUMMARY(ESTIMATED VALUES)			
LOGIC UTILIZATION	USED	AVAILABLE	UTILIZATION
NUMBER OF SLICE REGISTERS	8	93120	0%
NUMBER OF SLICELUTS	13	46560	0%
NUMBER OF FULLY USED LUT-FF PAIRS	0	21	0%
NUMBER OF BONDED	25	240	10%

IOBS			
NUMBER OF BUFG/BUFGCTRLS	3	32	9%

IV. CONCLUSION

It is clear from the synthesis report and output generated, that the IODELAY1 DPWM architecture is more compact and provides better resolution than the DCM based design. But the IODELAY1 DPWM architecture is dependable on the operating clock signal frequency. The frequency of operation is restricted to 200Mhz – 300Mhz depending on the virtex series which we use. The variations in the clock frequency outside the operational frequency can cause the IODELAY1 block to subject errors in the PWM signal where in the 1st design DCM block can work up to 200Mhz frequency and is more prone to errors and readjusts itself under that frequency.
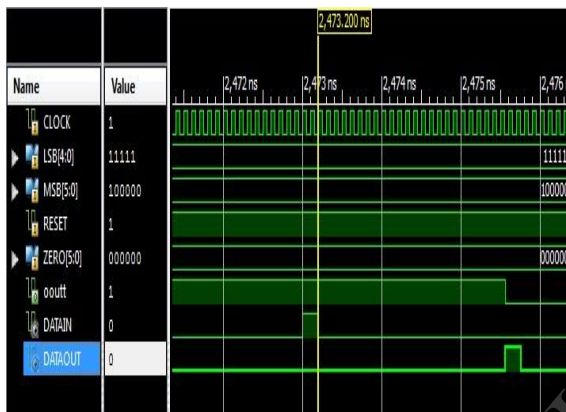

Fig:10. Waveform showing error due to clock frequency of IODELAY1 block

Fig10 shows the error subjected in the IODELAY1 DPWM architecture when clock variation (when the design operates outside the operating frequency of the IODELAY1 block) is subjected in the design. The DATAIN and DATAOUT signals will not follow the cntvaluein or tap delay which we provide. The other advantage of the designs is that they are synchronous which makes the designs more efficient and predictable to errors.

REFERENCE

[1] S.C. Huerta,A.de Castro,O.Garcia, andJ.A.Cobos,"FPGA-based digital pulse-widthmodulatorwithtime resolutionunder2 ns,"IEEE Trans.Power Electron.,vol.23,no.6, pp. 3135–3141,Nov.2008

[2] Synchronous FPGA-Based High-Resolution Implementations of Digital Pulse-Width Modulators Denis Navarro, O´ scar Luc´ıa, Member, IEEE, Luis Angel Barraga´n, Jose´ Ignacio Artigas, Isidro Urriza, and O´ scar Jime´nez, Student Member, IEEE. IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 27, NO. 5, MAY 2012

[3] A. Mohammed, "Digital control of power converters," IEEE Applied Power Electronics Conference and Exposition, Professional Education Seminars Workbook, Austin, TX, 2008.

[4] A. Prodic, D. Maksimovic, and R. W. Erickson, "Design and implementation of digital PWM controller for a high-frequency switching dc–dc power converter," in *Proc. IEEE Annu. Conf. Ind. Electron. Soc.*, 2001, pp. 893–898.

[5] A. V. Peterchev and S. R. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 301–308, Jan. 2003.

[6] L. Corradini, A. Bjeletic, R. Zane, and D. Maksimovic, "Fully digital hysteretic modulator for dc–dc switching converters," IEEE Trans. Power Electron., vol. 26, no. 10, pp. 2969–2979, 2011.

[7] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Sievaluation of potentials for performance improvement of inverter and dc–dc converter systems by SiC power semiconductors," IEEE Trans. Ind. Electron., vol. 58, no. 7, pp. 2872–2882, Jul. 2011.

[8] T. Nomura, M. Masuda, N. Ikeda, and S. Yoshida, "Switching characteristics of GaN HFETs in a half bridge package for high temperature applications," IEEE Trans. Power Electron., vol. 23, no. 2, pp. 692–697, Mar. 2008.

[9] A. Simon-Muela, Y. Elbasri, C. Alonso, V. Boitier, and J. L. Chaptal, "Modeling digital control laws for high-frequency VRM applications," in Proc. IEEE Power Electron. Spec. Conf., 2008, pp. 1560–1565.

[10] W. Yu, J. S. Lai, H. Ma, and C. Zheng, "High efficiency dc–dc converter with twin-bus for dimmable LED lighting," IEEE Trans. Power Electron., vol. 26, no. 8, pp. 2095–2100, Jul. 2011.

[11] S. Ajram and G. Salmer, "Ultrahigh frequency dc-to-dc converters using GaAs power switches," IEEE Trans. Power Electron., vol. 16, no. 5, pp. 594–602, May 2001.

[12] M. G. Batarseh, W. Al-Hoor, L. Huang, C. Iannello, and I. Batarseh, "Window-masked segmented digital clock manager-FPGA-based digital pulse-width modulator technique," IEEE Trans. Power Electron., vol. 24, no. 11, pp. 2649–2660, Nov. 2009.

[13] Spartan-3 Generation FPGA User Guide, UG331 (v 1.5), Xilinx, San Jose, CA, 2009, ch. 3.

[14] Virtex-6 FPGA SelectIO Resources User Guide, UG361 (v 1.3), Xilinx, San Jose, CA. 2009, ch. 2.