

Comparative Study on New COPWM Techniques for Three Phase Cascaded Z-Source Inverter

V. Arun^{#1}, B. Shanthi^{*2}, S. P. Natarajan^{\$3}

[#]Department of EEE, Arunai Engineering College, Thiruvannamalai, Tamilnadu, India

^{*}Centralised Instrumentation and Service Laboratory, Annamalai University, Chidambaram Tamilnadu, India

^{\$}Department of EIE, Annamalai University, Chidambaram, Tamilnadu, India

Abstract

This paper presents the comparison of the different Carrier Overlapping Pulse Width Modulation (COPWM) techniques for three phase seven level Z source cascaded inverter. Due to switch combination redundancies, there are certain degrees of freedom to generate the multi level AC output voltage. This work presents the use of CFD combination. The Z-source based CMLI is triggered by the different COPWM techniques having sinusoidal and Third Harmonic Injection (THI) reference with triangular carriers. It is observed that the COPWM-3 technique with sine reference provides reduced harmonics and COPWM-1 technique with THI reference provide improved RMS value at its output voltage. The effectiveness of the PWM techniques developed using CFD are demonstrated by simulation using MATLAB / SIMULINK.

1. Introduction

Multilevel inverters are a viable solution to increase the power with a relatively low stress on the components and with simple control systems. Multilevel inverter presents several other advantages. Multilevel inverter generates better output waveforms with a lower dv/dt than the standard inverter. Then, multilevel inverter can increase the power quality due to the great number of levels of the output voltage: in this way, the AC side

filter can be reduced, decreasing its costs and losses. Furthermore multilevel inverter can operate with a lower switching frequency than conventional inverter, so the electromagnetic emissions they generate are weaker, making less severe to comply with the standards. Multilevel inverter can be directly connected to high voltage sources without using transformers; this means a reduction of implementation and costs. Gajanayake et al [1] developed the closed-loop controller for a Z source inverter. Gao et al [2] developed five level diode clamped Z source inverter. Kanimozhi and Senthil Kumar [3] proposed cascaded Z source multilevel inverters for uninterruptible power supply application Mohamad and Ali [4] introduced DVR based cascaded inverter with Z source. Shafie Bakar et al [5] described the various PWM techniques. Yousuf et al [6] introduced multi carrier PWM technique for five level inverter. Poh Chiang Loh et al [7] introduced three-level Z source NPC inverter. Various pulse width modulation strategies for Z source NPC inverter were discussed in [8]. Shajith and Kamaraj [9] developed double carrier pulse width modulation control for Z source inverter. Sumedha and Lakumana [10] have designed impedance network of three level Inverter. Dual input and dual output Z source three level inverter was proposed by Seyed et al in [11]. Shanthi and Natarajan [12] developed carrier overlapping PWM methods for five level cascaded inverter. Shen and Peng [13] introduced Z source inverter with small inductor value. Urmila and Subbarayudu [14] discussed various PWM techniques for multilevel inverter. Yang et al [15] developed unified control technique for Z source inverter. This paper presents a three phase cascaded Z source inverter

topology for investigation with COPWM-1, COPWM-2 and COPWM-3 using sinusoidal and third harmonic injection reference switching techniques. Simulations were performed using MATLAB-SIMULINK. Harmonics analysis and evaluation of different performance measures for various modulation indices have been carried out and presented.

2. Z source seven level cascaded inverter

Figure 1 shows the two-port network that consists of an inductors (L_1 , L_2) and capacitors (C_1 , C_2) and connected in X shape is employed to provide an impedance source (Z Source) coupling the inverter to the dc source. The Z source multilevel inverter utilizes shoot-through state to boost the input dc voltage of inverter switches when both switches in the same phase leg are on.

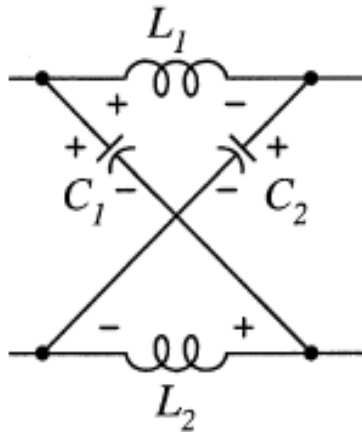


Figure 1. Impedance network

Figure 2 shows the seven level Z source cascaded inverter. The inverter topology is based on the series connection of single-phase inverters with separate impedance DC sources. The resulting phase voltage is synthesized by the addition of the voltages generated by the different cells. The number of output voltage levels are $2n+1$, where n is the number of cells. The AC output of each H-bridge is connected in series such that the synthesized output voltage waveform is the sum of all the individual H-bridge outputs. As the number of levels increase the harmonic distortion decreases and efficiency of the inverter increases because of the reduced switching losses.

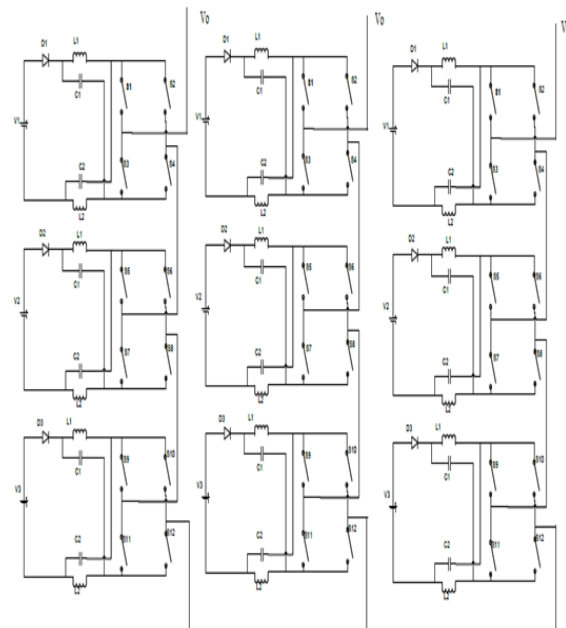


Figure 2. Seven level Z source cascaded inverter

3. Multicarrier overlapping PWM techniques

Carrier overlapping PWM technique is the widely adopted modulation technique for MLI. It is similar to that of the sinusoidal PWM technique except for the fact that several carriers are used. Multicarrier PWM is one in which several triangular carrier signals are compared with one sinusoidal modulating signal. $(m-1)$ carriers are required to produce m -level output. All carriers are having same frequency f_c and same peak-to-peak amplitude A_c are disposed such that the bands they occupy overlap each other; the overlapping vertical distance between each carrier is $A_c/2$. As far as the particular carrier signals are concerned, there are multiple CFD including Frequency, amplitude, phase of each carrier and offsets between carriers. The reference wave of multilevel carrier based PWM method can be sinusoidal and third harmonic injection. As far as the particular reference wave is concerned there is also multiple CFD including frequency, amplitude, phase angle of the reference wave and as in three phase circuits, the injected zero sequence signal to the reference wave. Therefore multilevel carrier based PWM methods can offer multiple CFD. These CFD combinations combined with the basic topology of multilevel inverters can produce many multilevel carrier based PWM methods. This paper focuses on three COPWM techniques that utilize the CFD of vertical offsets among carriers. They are: COPWM-1, COPWM-2 and COPWM-3.

The amplitude modulation index m_a and the frequency ratio m_f are defined in the carrier overlapping method as follows:

$$m_a = A_m / 2A_c$$

$$m_f = f_c / f_m$$

THI reference is developed by superimposing a third harmonic component on fundamental. The addition of third harmonic makes it possible to increase the maximum amplitude of fundamental in the reference. Harmonic elimination techniques, which are suitable for fixed output voltage, increase the order of harmonics and reduce the size of output filter. But these advantages should be weighed against increase in switching losses of power devices and iron losses in transformer due to high harmonic frequencies. It is not always necessary to eliminate triplen harmonics which are not normally present in three phase connections.

3.1. COPWM-1 Technique

The vertical offset of carriers for seven level inverter with COPWM-1 technique having Sine reference and THI are illustrated in figures 3 & 4 respectively. It can be seen that the three carriers are overlapped in positive group and three are overlapped in the negative group and the reference wave is placed at the middle of the four carriers. In this technique all the carrier waveforms are in phase.

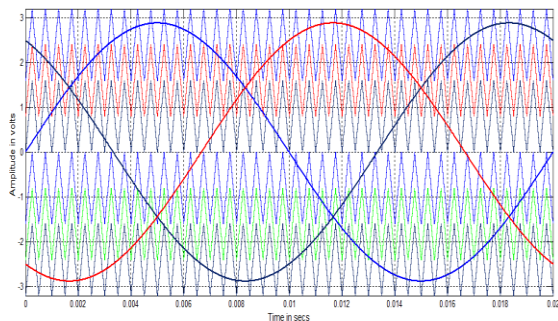


Figure 3. Carrier arrangement for COPWM-1 Technique with sine reference ($m_a=0.9$, $A_c=1.6$, $A_m=2.88$, $m_f=40$)

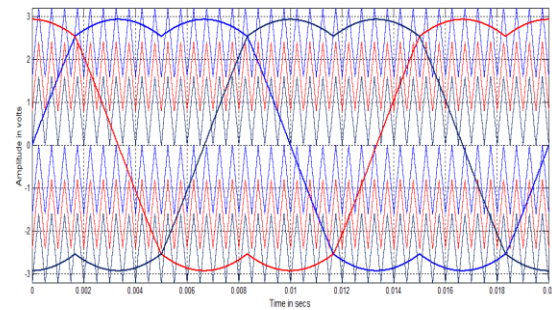


Figure 4. Carrier arrangement for COPWM-1 Technique with THI reference ($m_a=0.9$, $A_c=1.6$, $A_m=2.88$, $m_f=40$)

3.2. COPWM-2 Technique

Carriers for seven level inverter with COPWM-2 technique having Sine reference and THI are illustrated in figures 5 & 6 respectively. It can be seen that the carriers are divided equally into two groups according to the positive/negative average levels. In this technique the two groups are opposite in phase with each other while keeping in phase within the group [12].

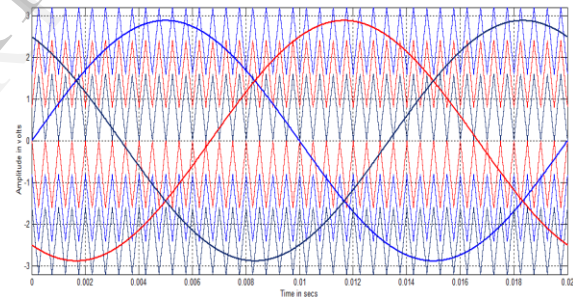


Figure 5. Carrier arrangement for COPWM-2 Technique with sine reference ($m_a=0.9$, $A_c=1.6$, $A_m=2.88$, $m_f=40$)

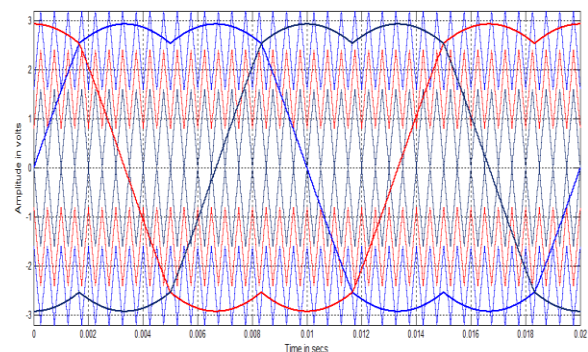


Figure 6. Carrier arrangement for COPWM-2 Technique with THI reference ($m_a=0.9$, $A_c=1.6$, $A_m=2.88$, $m_f=40$)

3.3. COPWM-3 Technique

Carriers for seven level inverter with COPWM-3 technique having Sine reference and THI are illustrated in figures 7 & 8 respectively. In this technique carriers invert their phase in turns from the previous one. It may be identified as PWM with amplitude-overlapped and neighbouring-phase-interleaved carriers. COPWM-2 and COPWM-3 have second control freedom change with the carriers horizontally phase shifted from COPWM-1 besides the offsets in vertical [12].

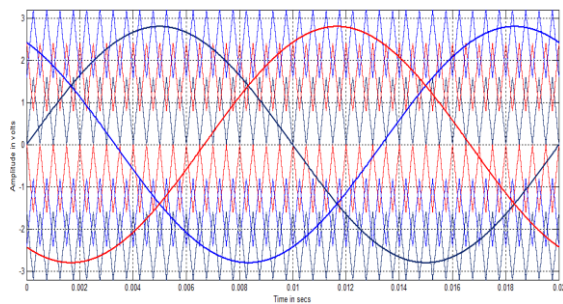


Figure 7. Carrier arrangement for COPWM-3 Technique with sine reference ($m_a=0.9$, $A_c=1.6$, $A_m=2.88$, $m_f=40$)

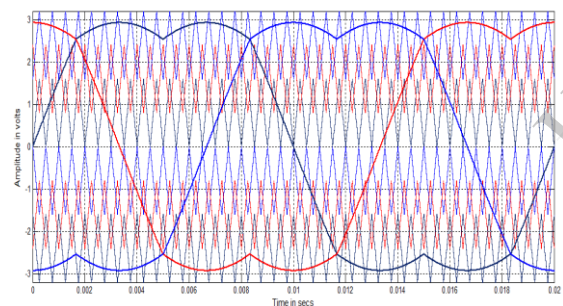


Figure 8. Carrier arrangement for COPWM-2 Technique with THI reference ($m_a=0.9$, $A_c=1.6$, $A_m=2.88$, $m_f=40$)

4. Simulation results

The Z-source cascaded seven level inverter is modelled in SIMULINK using power system block set. Switching signals for cascaded multilevel inverter using COPWM techniques are simulated. Simulations are performed for different values of m_a ranging from 0.8 to 1 and the corresponding %THD for both sinusoidal and THI references are measured using the FFT block and their values are shown in Table I & II and the corresponding graphical representations are found in figure 21 and figure 22 respectively. Figure 9-20 show the simulated output voltage of Z-source CMLI and their harmonic spectrum. Figure 9 displays

the seven level output voltage generated by COPWM-1 switching technique with sine reference and its FFT plot is shown in Figure 10. Figure 11 shows the seven level output voltage generated by COPWM-2 switching technique with sine reference and its FFT plot is shown in Figure 12. Figure 13 shows the seven level output voltage generated by COPWM-3 switching technique with sine reference and its FFT plot is shown in Figure 14. Figure 15 displays the seven level output voltage generated by COPWM-1 switching technique with THI reference and its FFT plot is shown in Figure 16. Figure 17 shows the seven level output voltage generated by COPWM-2 switching technique with THI reference and its FFT plot is shown in Figure 18. Figure 19 shows the seven level output voltage generated by COPWM-3 switching technique with THI reference and its FFT plot is shown in Figure 20. Tables III & IV show the VRMS (fundamental) of the output voltage of the proposed inverter. The Crest factor of the output voltage listed in Table V & VI. The following parameter values are used for simulation: $V_{DC} = 50V$, R (load) = 10 ohms, $f_c = 2000$ Hz and $f_m = 50$ Hz.

4.1. Simulation result for sinusoidal reference

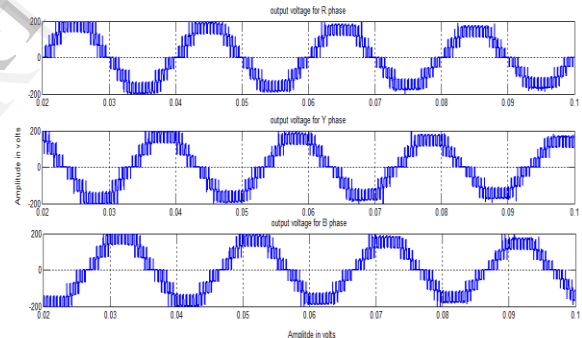


Figure 9. Output voltage generated by COPWM-1 Technique with sine reference

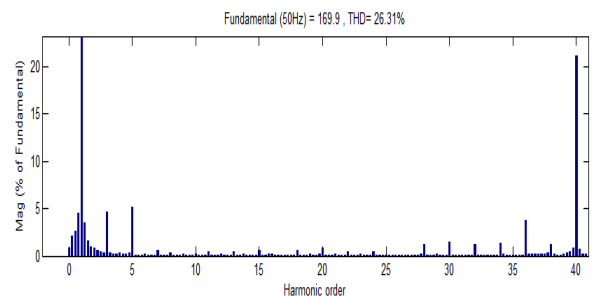


Figure 10. FFT plot of COPWM-1 Technique with sine reference

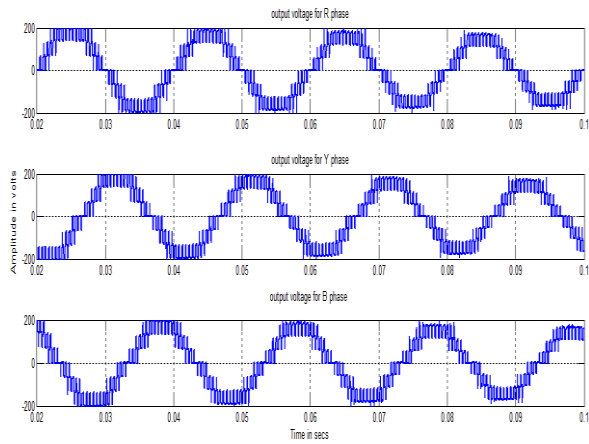


Figure 11. Output voltage generated by COPWM-2 Technique with sine reference

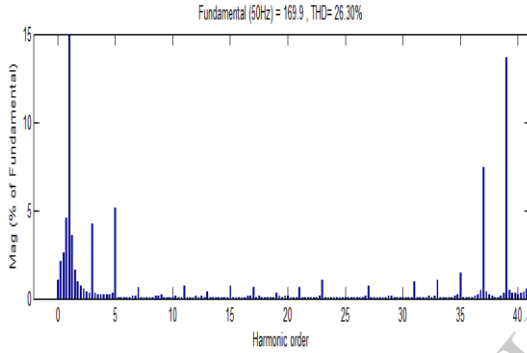


Figure 12. FFT plot of COPWM-2 Technique with sine reference

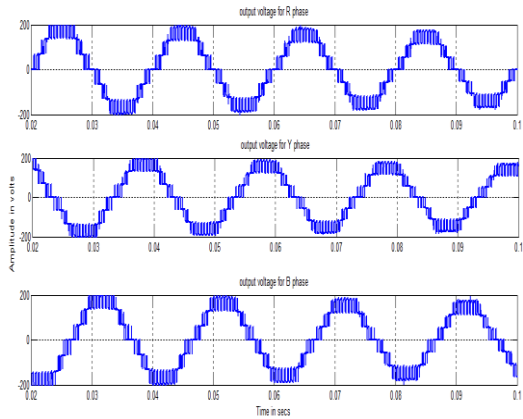


Figure 13. Output voltage generated by COPWM-3 Technique with sine reference

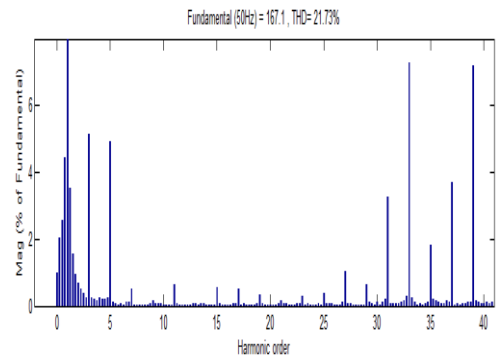


Figure 14. FFT plot of COPWM-3 Technique with sine reference

4.2. Simulation result for THI reference

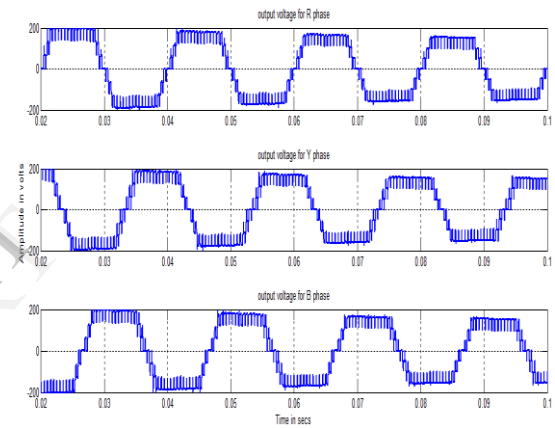


Figure 15. Output voltage generated by COPWM-1 Technique with THI reference

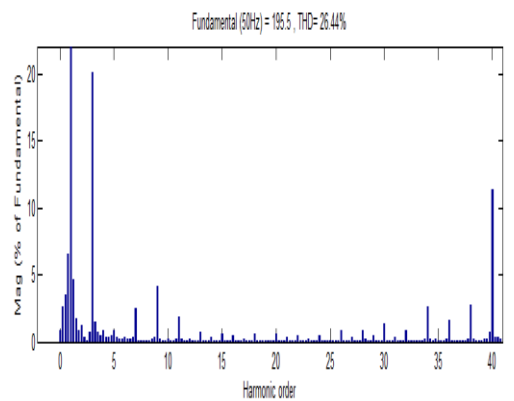


Figure 16. FFT plot of COPWM-1 Technique with THI reference

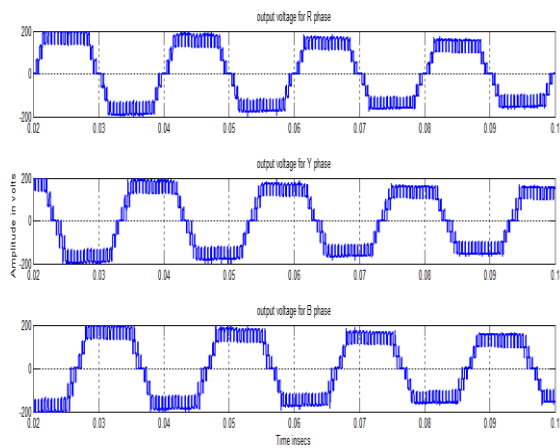


Figure 17. Output voltage generated by COPWM-2 Technique with THI reference

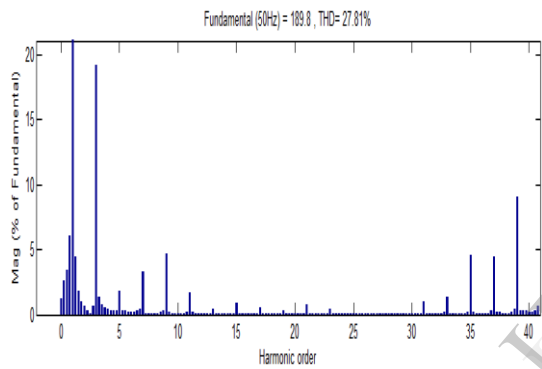


Figure 18. FFT plot of COPWM-2 Technique with THI reference

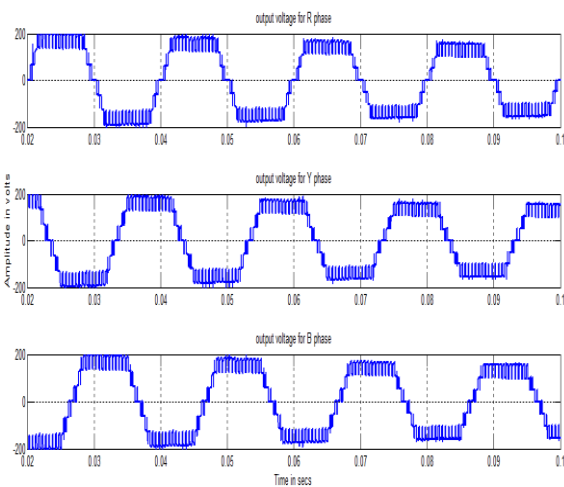


Figure 19. Output voltage generated by COPWM-3 Technique with THI reference

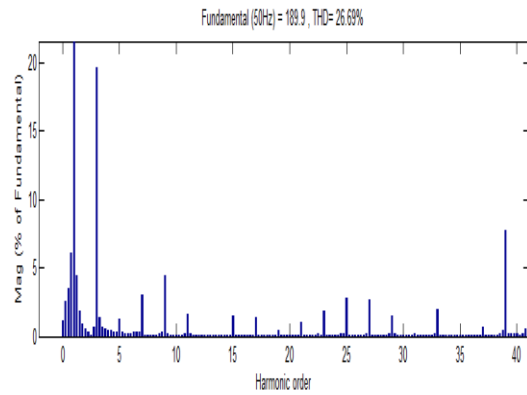


Figure 20. FFT plot of COPWM-3 Technique with THI reference

Table 1.

% THD for different modulation indices for sinusoidal reference

m_a	COPWM-1	COPWM-2	COPWM-3
1	21.43	21.31	16.85
0.9	26.31	26.30	21.73
0.8	31.11	30.92	23.74

Table 2.

% THD For Different Modulation Indices For THI Reference

m_a	COPWM-1	COPWM-2	COPWM-3
1	25.62	25.53	24.06
0.9	26.44	27.81	26.69
0.8	20.14	29.91	27.68

Table 3.

V_{RMS} for different modulation indices with sinusoidal reference

m_a	COPWM-1	COPWM-2	COPWM-3
1	128.5	128.8	128.8
0.9	120.1	120.1	118.2
0.8	110.4	110.4	110.8

Table 4.
V_{RMS} for different modulation indices with THI reference

m _a	COPWM-1	COPWM-2	COPWM-3
1	140.4	140.4	140.5
0.9	138.2	134.1	134.3
0.8	127.6	127.2	127.6

Table 5.
% CF for different modulation indices for sinusoidal reference

m _a	COPWM-1	COPWM-2	COPWM-3
1	1.4140	1.4138	1.4138
0.9	1.41465	1.4146	1.4137
0.8	1.4139	1.2327	1.4142

Table 6.
% CF for different modulation indices with THI reference

m _a	COPWM-1	COPWM-2	COPWM-3
1	1.4138	1.4138	1.4142
0.9	1.4146	1.4153	1.4139
0.8	1.4137	1.4143	1.4145

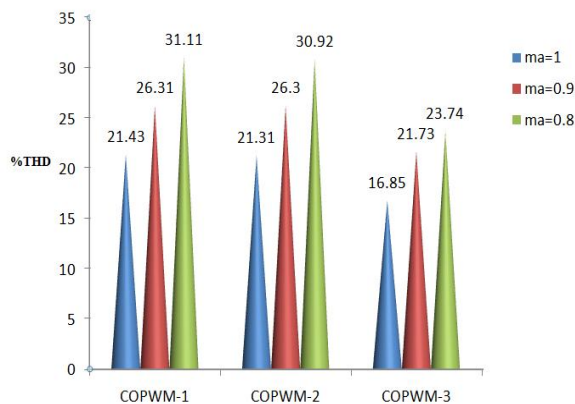


Figure 21. %THD Vs m_a (Sine reference PWM)

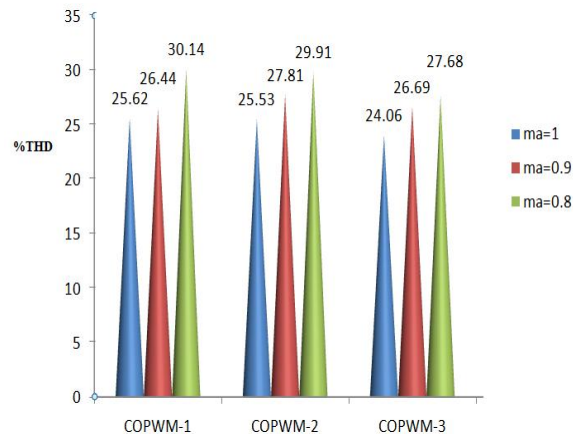


Figure 22. %THD Vs m_a (THI reference PWM)

It is observed that harmonic output voltage is least with COPWM-3 with sine reference technique. The CF is relatively equal for all the strategies. From the FFT spectrum the following are observed, lower order harmonics are relatively equal for all the three strategies and 3rd order harmonic is dominant in all the strategies. From Table III & IV it is observed that V_{rms} value is high in COPWM-1 technique with THI reference.

5. Conclusion

In this paper, COPWM techniques for Z- source seven level cascaded inverter have been presented. Z-source multilevel inverter gives higher output voltage through its Z network. Performance factors like %THD, V_{rms} and CF have been evaluated, presented and analyzed. It is found that the COPWM-3 with sine reference technique provides lower %THD. COPWM-1 with THI reference technique provide higher V_{RMS}. The result indicate that appropriate PWM strategies have to be employed depending on the performance measure required in a particular application of MLI based on the criteria of output voltage quality (Peak value of the fundamental, THD and dominant harmonic components).

6. References

- [1] Chandana Jayampathi Gajanayake, D. Mahinda Vilathgamuwa and Poh Chiang Loh, "Development of a Comprehensive Model and a Multiloop Controller for Z Source Inverter DG Systems," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 4, pp-1295-1308, 2007.
- [2] Gao, F.Loh, P.C.Blaabjerg, F.Teodorescu, R.Vilathgamuwa, "Five-level Z-source diode-clamped

- inverter,” *IEEE Transaction on Power Electronics*, vol. 3, no. 4, July 2010.
- [3] S.Kanimozhi, R.Senthil Kumar “Z Source Multilevel Inverter for Uninterruptible Power Supply Application,” *International Journal of Power Systems and Integrated Circuits*, vol. 2, Special Issue 1, pp-29-31, 2012.
- [4] Mohamad Reza Banaei and Ali Reza Dehghanzadeh, “DVR Based Cascaded Multilevel Z-Source Inverter,” *IEEE International Conference on Power and Energy*, December 2010.
- [5] Mohd. Shafie Bakar, Nasrudin Abd. Rahim and Kamarul Hawari GhaZali, “Analysis of various PWM Controls on Single-Phase Z Source Inverter,” in *Proc. IEEE Con. Rec.: 978-1-4244-8648-9/10 (SCORE2010)*, 2010.
- [6] S.Mohamed Yousuf, P.Vijayadeepan and Dr.S.Latha, “The Comparative THD Analysis of Neutral Clamped Multilevel Z Source Inverter using Novel PWM Control Techniques,” *International Journal of Modern Engineering Research*, vol.2, Issue.3, pp-1086-1091, 2012.
- [7] Poh Chiang Loh, Feng Gao and Frede Blaabjerg, “Topological and Modulation Design of Three-Level Z Source Inverters,” *IEEE Transactions on Power Electronics*, vol. 23, No. 5, pp-2268-2277, 2008.
- [8] Poh Chiang Loh, Frede Blaabjerg and Chow Pang Wong, “Comparative Evaluation of Pulse Width Modulation Strategies for Z Source Neutral-Point-Clamped Inverter,” *IEEE Transactions on Power Electronics*, vol. 22, no. 3, pp-1005-1013, 2007.
- [9] U.Shajith Ali and V.Kamaraj, “Double Carrier Pulse Width Modulation Control of ZSource Inverter,” *European Journal of Scientific Research*, vol.49, no.2, pp.168-176, 2011.
- [10] Sumedha Rajakaruna and Laksumana Jayawickrama, “Steady-State Analysis and Designing Impedance Network of Z Source Inverters,” *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp-2483-2491, 2010.
- [11] Seyed Mohammad Dehghan, Mustafa Mohamadian, Ali YaZdian and Farhad AshrafZadeh, “A Dual-Input–Dual-Output Z Source Inverter,” *IEEE Transactions on Power Electronics*, vol. 25, no. 2, pp360-368, 2010.
- [12] B. Shanthi and S.P. Natarajan, “Carrier Overlapping PWM Methods for Single Phase Cascaded Five Level Inverter,” *International Journal of Sciences and Techniques of Automatic Control and Computer Engineering*, special issue, pp.590-601, 2008.
- [13] M. Shen and F. Z. Peng, “Operation modes and characteristics of the Z-source inverter with small inductance or low power factor,” *IEEE Transactions on Industrial Electronics*, vol. 55, no. 1, pp. 89–96, Jan. 2008.
- [14] B.Urmila, and D.Subbarayudu, “Multilevel Inverters: A Comparative Study of Pulse Width Modulation Techniques,” *Journal of Scientific and Engineering Research*, pp.1-5, 2010.
- [15] S. Yang, X. Ding, F. Zhang, F. Z. Peng, and Z. Qian, “Unified control technique for Z-source inverter,” in *Proc. IEEE Power Electron. Spec.Conf.*, pp. 3236-3242, 2008.